# Generalized Analytical Design Equations for Variable Slope Class-E Power Amplifiers

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***Abstract*— The Class-E power amplifier is widely used because of its high efficiency, resulting from switching at zero voltage and zero slope of the switch voltage. In this paper, we extend our general analytical solutions for the Class-E power amplifier to the ideal single-ended Variable Slope Class-E (Class-E$_{VS}$) power amplifier which is switching at zero voltage but not necessarily at zero slope. It is shown that a Class-E$_{VS}$ power amplifier can have higher tolerance to switch (transistor) output capacitance compared to the normal Class-E power amplifier; this higher tolerance can be exchanged for higher drain efficiency. The presented design equations for Class-E$_{VS}$ power amplifiers give more degrees of freedom in the design and optimization of switching RF power amplifiers.**

## I. Introduction

Many different aspects of the Class-E power amplifier (PA) have been extensively studied in the last three decades [1]-[5]. The ideal Class-E PA features zero-level and zero-slope switching which results in high efficiency. The reportedly "sub-optimum operation" with non-zero slope switching [2] is hardly used because of its believed inferior performance [1]. In this paper, the non-zero slope switching Class E PA will be referred to as Variable Slope Class-E (Class-E$_{VS}$) PA.

Analyses of the Class-E$_{VS}$ PA are presented in [1] and in [3]. In [1], it is shown that an RF-choke Class-E$_{VS}$ PA has a slightly larger tolerance to switch (transistor) output capacitance ($\approx$ 10% more) compared to the conventional Class-E PA with an RF-choke. In [3], an iterative design procedure is presented to design a Class-E$_{VS}$ PA.

It is well-known that using a finite dc feed inductance instead of an RF-choke in Class-E has benefits [3], [4] including:

- a reduction in overall size and cost
- a higher load resistance for the same supply voltage and output power; this typically yields more efficient output matching networks
- larger switch parallel capacitor $C$ (Fig. 1a) for the same supply voltage, output power and load. This enables higher drain efficiency or higher frequency of operation.

This paper presents an analysis and some discussions on Class-E$_{VS}$ PAs with *finite dc-feed inductance* to combine the increased tolerance to e.g. capacitances of Class-E$_{VS}$ with the advantages of using finite dc-feed inductances. The analysis in this paper is based on closed form expressions like the ones presented in [4]. As a result of the analysis, analytical design equations are presented showing the relation between the design parameters. It is shown in this paper that Class-E$_{VS}$ with *finite dc-feed inductance* can have very high tolerance to switch (transistor) output capacitance ($\approx$ 110% more than Class-E with *finite-dc feed inductance* and $\approx$ 680% more than Class-E with *RF-choke*); which allows using large transistors hence yields higher drain efficiency than conventional Class-E PAs. Besides, the switch voltage of the Class-E$_{VS}$ PA for negative turn-on slopes resembles to a half-sinusoid having less higher harmonics and lower peak value than that in a conventional Class-E PA which is beneficial for e.g. filtering, reliability.

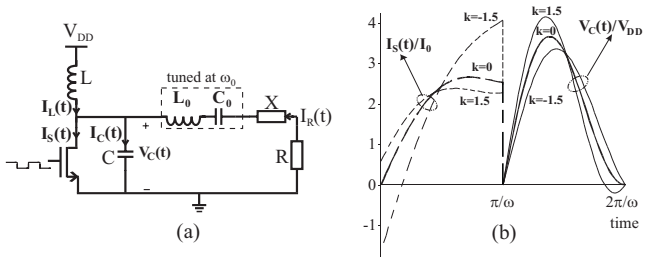


Fig. 1. (a) Single-ended Class-E$_{VS}$ PA (b) Normalized switch voltage and switch current of Class-E$_{VS}$ PA with finite dc-feed inductance with the turn-on slope of $k = -1.5$, $k = 0$(Class-E) and $k = 1.5$

## II. Analysis of Class-E$_{VS}$ Power Amplifier

A single ended switching PA topology is given in Fig. 1. If the correct input parameters and the circuit element values are chosen, the circuit properly operates as a Class-E PA by satisfying the following conditions (1) and (2) [2], [1]:

$$V_C(2\pi/\omega) = 0 \tag{1}$$

$$\left.\frac{dV_C(t)}{dt}\right|_{t=2\pi/\omega} = \omega V_{DD} k \tag{2}$$

where $\omega V_{DD} k$ is the slope of $V_C(t)$ at the moment the switch is closed; for conventional Class-E operation $k = 0$. However, in Class-E$_{VS}$ operation $k$ is a real value that can be selected freely and therefore gives a degree of freedom in the design of a Class-E$_{VS}$ PA[1].

For the switching PA in Fig. 1a a design set $K = \{K_L, K_C, K_P, K_X\}$ can be derived that relates circuit element values and operating conditions such as supply voltage, operating frequency and output power. In [4], an analytical solution is given that enables infinitely many ideal Class-E realizations, to be selected by one parameter $q = 1/(\omega\sqrt{LC})$. The expressions for the elements in the design set $K$ are given in Table 1; the values of the elements (as a function of $q$) are presented in [4] for conventional Class-E operation.

[1]For $k = 0$, (1) and (2) are the well-known conventional Class-E conditions from which it follows that conventional Class-E operation is a special case of general Class-E$_{VS}$ operation.

| $K_L = \frac{\omega L}{R}$, $K_C = \omega CR$, $K_P = \frac{P_{OUT}R}{V_{DD}^2}$, $K_X = \frac{X}{R}$ |
|---|

Table 1: Design Set $K$ for Class-E$_{VS}$ PA[2]

In this paper, the analytical solution in [4] is extended to cover Class-E$_{VS}$ PAs as well. Therefore, an analytical solution for the design set $K$ is derived which also allows a non-zero slope of the switch voltage at the turn-on moment of the switch; the slope is here defined by the value for $k$. This section presents the derivation of the design set $K$ for Class-E$_{VS}$ PAs.

### A. Circuit Description and Assumptions

The circuit schematic of the Class-E$_{VS}$ PA is given in Fig. 1a. For the analysis and derivations in this paper a number of assumptions are made:

- the only real power loss in the circuit occurs on load R
- the switch (transistor) is loss-less, operating instantly with zero on-resistance and infinite off-resistance
- the loaded quality factor ($Q_L$) of the series resonant circuit ($L_0$ and $C_0$) is high enough in order for the output current to be sinusoidal at the switching frequency
- the duty cycle is 50%

Fig. 1b illustrates the switching behavior and the switch definition used here: in the time interval $0 \leq t < \pi/\omega$ the switch is closed and in the time interval $\pi/\omega \leq t < 2\pi/\omega$ it is opened. This switching action repeats itself with a period of $2\pi/\omega$.

### B. Circuit Analysis

In the analysis, the current into the load, $I_R(t)$, is assumed to be sinusoidal. Note that theoretically this occurs only for infinite $Q_L$ of the series resonant network consisting of $L_0$ and $C_0$. It is however a widely used assumption [1] - [6] that simplifies analysis considerably:

$$I_R(t) = I_R \sin(\omega t + \varphi) \tag{3}$$

*In the time interval* $0 < t < \pi/\omega$, the switch is closed and hence the capacitance voltage $V_C(t) = 0$ and the current through the capacitance $I_C(t) = C\frac{dV_C(t)}{dt} = 0$. In this time interval, the switch current $I_S(t)$ is

$$\begin{aligned} I_S(t) &= I_L(t) + I_R(t) \\ &= \frac{V_{DD}}{L}t - I_L(0) + I_R \sin(\omega t + \varphi) \quad (4) \\ \text{where} \quad I_L(0) &= C \cdot \omega V_{DD} k - I_R \sin(\varphi) \end{aligned}$$

*In the time interval* $\pi/\omega < t < 2\pi/\omega$, the switch is opened. Then, in the Class-E PA the current through capacitance $C$ is

$$I_C(t) = \frac{1}{L}\int_{\pi/\omega}^{t} (V_{DD} - V_C(t))\, dt + I_L\left(\frac{\pi}{\omega}\right) + I_R(t) \tag{5}$$

Relation (5) can be re-arranged in the form of a linear, nonhomogeneous, second-order differential equation

$$LC\frac{d^2V_C(t)}{dt^2} + V_C(t) - V_{DD} - \omega L I_R \cos(\omega t + \varphi) = 0 \tag{6}$$

[2] $L_0$ and $C_0$ seen in Figure 1 can be determined from the chosen loaded quality factor ($Q_L = \omega_0 L_0/R$) where $\omega_0 = 1/\sqrt{L_0 C_0}$.

which has as solution

$$\begin{aligned} V_C(t) = \quad & C_1 \cos(q\omega t) + C_2 \sin(q\omega t) + V_{DD} - \quad (7) \\ & \frac{q^2}{1-q^2} p V_{DD} \cos(\omega t + \varphi) \end{aligned}$$

where $q = 1/(\omega\sqrt{LC})$ and $p = \omega L I_R / V_{DD}$. The coefficients $C_1$ and $C_2$ follow from the initial off state conditions, $V_C(\pi/\omega) = 0$ and $I_L(\pi/\omega) = \frac{V_{DD}}{\omega L}(\pi - p\sin(\varphi) + \frac{k}{q^2})$.

It follows from (4) and (7) that $V_C(t)$ and $I_S(t)$ can be expressed in terms of $V_{DD}$ and $\omega$ only if $\varphi$, $q$, $p$ and $k$ are known. The variable $k$ is already defined as a free variable that can take real numbers. The derivation of the three parameters $\varphi$, $q$ and $p$ is the next step in the derivation.

To derive expressions for the three unknowns so far, $\varphi$, $q$ and $p$, three independent equations are required. For this, the two basic Class-E$_{VS}$ equations (1) and (2) can be used, together with some other equation. A suitable extra equation can be based on stationary behavior of Class-E$_{VS}$ PA: $\overline{V_L(t)} = |\text{constant}|$ and $\overline{V_C(t)} = |\text{constant}|$. Working out the latter for stationary behavior yields

$$V_{DD} \quad = \quad \frac{\omega}{2\pi}\int_0^{2\pi/\omega} V_C(t)\, dt \tag{8}$$

With (8), (1) and (2) three non-linear equations with unknowns $\varphi$, $q$, $p$ and the free variable $k$ are obtained. These three equations can be arranged in the same form:

$f_i(p, q, \varphi, k) \quad = \quad p\Big(a_i(q,k)\cos(\varphi) \; + \; b_i(q,k) sin(\varphi)\Big) \; + \; c_i(q,k) = 0$, where $i = 1, 2, 3$.

Solving the non-linear set of the equations for $\varphi$, $q$ and $p$ is now more or less straightforward. For example, $f_1(p, q, \varphi, k)$ and $f_2(p, q, \varphi, k)$ can be used to solve $p$ and $\varphi$ in terms of $q$ and $k$. If the obtained expressions for $p(q, k)$ and $\varphi(q, k)$ are substituted in $f_3(p, q, \varphi, k)$ it can be seen that $f_3(q, k) = 0$ independent of $q$ and $k$; which proves that the obtained expressions for $p(q, k)$ and $\varphi(q, k)$ are the analytical solution of the system of equations. For every *real* value $q$ and $k$ there is a solution for $p$ and $\varphi$.

$$(p(q,k), \varphi(q,k)) = \quad \left\{ \begin{array}{ll} (p_1(q,k), \varphi_1(q,k)) & \text{if } q > 1 \\ (p_2(q,k), \varphi_2(q,k)) & \text{if } q < 1 \end{array} \right\}$$

where,

$$\begin{aligned} \varphi_1(q,k) = \quad & \arctan(\varphi_a(q,k), \varphi_b(q,k)) \\ \varphi_2(q,k) = \quad & -\arctan(\varphi_a(q,k), -\varphi_b(q,k)) \\ \varphi_a(q,k) = \quad & (q\pi \, \sin(q\pi) + 2 - 2\, \cos(q\pi))\, q \sin(q\pi) \\ \varphi_b(q,k) = \quad & \Big(4 - 2\, \sin(q\pi)^2 - 4\, \cos(q\pi)\Big) q^2 + \\ & q \sin(q\pi)\Big((\cos(q\pi) - 1)(2k + \pi)\Big) \\ & -4 + 2\, \sin(q\pi)^2 + 4\, \cos(q\pi) \\ p_1(q,k) = \quad & -p_2(q) \\ p_1(q,k) = \quad & x_0\sqrt{\Big(x_1 + x_2 q + x_3 q^2 + x_4 q^3 + x_5 q^4\Big)} \end{aligned}$$

$$
\begin{aligned}
x_0 = &\ \frac{(q+1)(q-1)}{2\sin(q\pi)^2 q^4}\\
x_1 = &\ 4\Big(\sin(\pi q)^2\left(\sin(\pi q)^2+4\cos(\pi q)-8\right)+\\
&\ 8(1-\cos(\pi q))\Big)\\
x_2 = &\ 4(2k+\pi)\sin(\pi q)\cdot\\
&\ \Big((\cos(\pi q)-3)\sin(\pi q)^2+4(1-\cos(\pi q))\Big)\\
x_3 = &\ \left(-\pi^2-12\right)\sin(\pi q)^4-64+64\cos(\pi q)+\\
&\ \left(-2\,\pi^2\cos(\pi q)+2\,\pi^2+72-40\cos(\pi q)\right)\sin(\pi q)^2\\
x_4 = &\ 8\sin(\pi q)^3\Big(\left(-\cos(\pi q)+3\right)k+\pi\left(2-\cos(\pi q)\right)\Big)\\
&\ +16(\cos(\pi q)-1)\sin(\pi q)(2k+\pi)\\
x_5 = &\ \left(\pi^2+4\right)\sin(\pi q)^4+32-32\cos(\pi q)+\\
&\ (16\cos(\pi q)-32)\sin(\pi q)^2
\end{aligned}
$$

### C. Design sets for Class-$E_{VS}$ operation

The results of the complex mathematical derivation of the (infinitely many) solutions leading to Class-$E_{VS}$ operation can be simplified considerably, yielding an easy-to-use design procedure for general Class-$E_{VS}$ PAs. In the previous subsection it was mentioned that $p$ and $\varphi$ both can be solved as a function of $q$ and $k$;

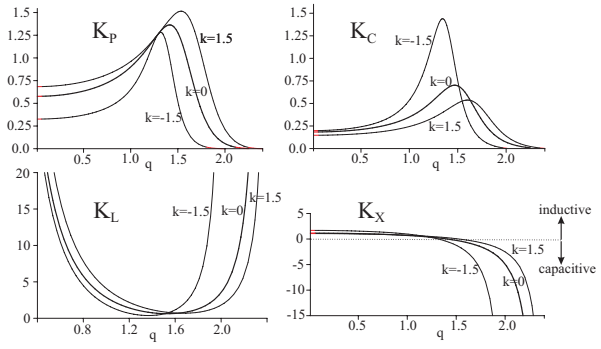


Fig. 2. Elements of the design set $K_P(q), K_C(q), K_L(q), K_X(q)$ as a function of $q$ for different values of $k$

Using the relations for $\varphi$, $p$, $q$ and $k$, design sets $K = \{K_L, K_C, K_P, K_X\}$ can readily be derived.

$K_L$ : The expression for $K_L$ can be derived by using the fact that (with the assumption of an ideal switch) the conversion efficiency from DC power to AC power is $100\%$:

$$I_R^2\frac{R}{2} = I_0 V_{DD} \tag{9}$$

In this relation, $I_0$ is the average supply current:

$$
\begin{aligned}
I_0 &= \frac{\omega}{2\pi}\int_0^{2\pi/\omega} I_S(t)\,dt\\
&= \frac{I_R}{2\pi}\Big(\frac{\pi^2}{2p}+2\cos(\varphi)-\pi\sin(\varphi)+\frac{k\pi}{q^2 p}\Big)
\end{aligned}
\tag{10}
$$

Substitution of (10) and $p$ in (9) yields

$$K_L(q,k) = \frac{p(q,k)}{\frac{\pi}{2p(q,k)}+\frac{2\cos(\varphi(q,k))}{\pi}-\sin(\varphi(q,k))+\frac{k\pi}{q^2 p}} \tag{11}$$

Since $p$ and $\varphi$ both are functions of $q$ and $k$, $K_L(q)$ is a function of e.g. only $q$ and $k$.

$K_C$**:** $K_C$ follows directly from the definition of $q$ and (11):

$$K_C(q,k) = \frac{1}{q^2 K_L(q,k)} \tag{12}$$

$K_P$**:** An expression for $K_P$ as a function of $p$ and $q$ can easily be found using $I_R = \sqrt{2P_{OUT}/R}$ and the definition of $p$:

$$K_P(q,k) = \frac{1}{2}\frac{p(q,k)^2}{K_L(q,k)^2} \tag{13}$$

$K_X$**:** An analytical expression for $K_X$ can be derived using two fundamental quadrature Fourier components of $V_C(t)$.

$$V_R = \frac{1}{\pi}\int_0^{2\pi/\omega}\left(V_C(t)\sin(\omega t+\varphi)\right)dt$$

$$V_X = \frac{1}{\pi}\int_0^{2\pi/\omega}\left(V_C(t)\cos(\omega t+\varphi)\right)dt$$

$$K_X(q,k) = \frac{V_X}{V_R}$$

The values for $K_L$, $K_C$, $K_P$ and $K_X$ are plotted in Fig. 2 as a function of $q$ for certain $k$ values. $K_C$ for finite dc-feed Class-$E_{VS}$ (q=1.35,k=-1.5) is $\approx 2.1$ times larger than for finite dc-feed Class-E (q=1.41,k=0) and $\approx 7.8$ times larger than for RF-choke Class-E (q=0,k=0). The analytical design equations were verified with transient and periodic steady state (pss) simulations (Spectre) by using an (almost) ideal switch with very low on resistance ($R_{ON} << R$). Good agreement in the waveforms are observed between simulations and the theory with a difference less than $4\%$, which is attributed to finite $Q_L$=20 and non-zero $R_{ON}$.

## III. Comparison and Design Example

A very important performance criteria for switching PAs is drain efficiency ($\eta$). In this section, we compare $\eta$ for Class-E PA and Class-$E_{VS}$ PA by taking into account two crucial conditions in switching PA designs:

a) the peak switch voltage must not exceed the switch (transistor) break-down voltage ($V_{BD}$),

b) the switch output capacitance ($C_{OUT}$) must be smaller than $C$.

Existence of a small switch on-resistance ($R_{ON}$) is assumed which causes a small power consumption ($P_{cond} \approx I_{RMS}^2 R_{ON}$) but doesn't influence the voltage and the current waveforms [3]. Taking into account these assumptions, the drain efficiency can be expressed as [4]:

[3] $I_{RMS}$ is the rms value of the switch current.

[4] While this approach to efficiency calculation is not expected to predict $\eta$ with great accuracy, it is very useful to compare the different classes of PA's performance as it is used by [6] to compare Class-E and Class-E/F PAs.

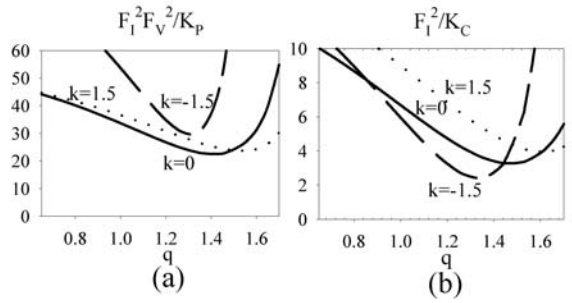


Fig. 3. Loss-factors (a) ($\frac{F_I^2 F_V^2}{K_P}$) for limited size transistor Class-E$_{VS}$ and (b) ($\frac{F_I^2}{K_C}$) for freely chosen size transistor Class-E$_{VS}$ PA

$$\eta = \frac{P_{DC} - P_{cond}}{P_{DC}} = 1 - \frac{R_{ON}}{\frac{V_{DD}}{I_0}} (\frac{I_{RMS}}{I_0})^2$$

$$= 1 - F_I^2 \frac{R_{ON}}{\frac{K_P V_{DD}^2}{P_{OUT}}}$$

$$= 1 - \frac{F_I^2 F_V^2}{K_P} \cdot \frac{R_{ON}}{V_{BD}^2} \cdot P_{OUT} \quad (14)$$

$$= 1 - \frac{F_I^2}{K_C} \cdot \beta^2 \cdot \omega^2 \quad (15)$$

where, $F_V = \frac{V_{BD}}{V_{DD}}$, $F_I = \frac{I_{RMS}}{I_0}$ and $\beta = R_{ON} C_{OUT}$.

(15) is derived from (14) with the assumption that $C_{OUT} = C$. In (14), the term $F_I^2 F_V^2 / K_P$ is dependent on the tuning strategy while $R_{ON}/V_{BD}^2$ and $P_{OUT}$ are dependent on the transistor technology and the given design specs respectively. Similarly, in (15) the term $F_I^2/K_C$ is dependent on the tuning strategy and the terms $\beta^2$ and $\omega^2$ are dependent on the transistor technology and the design specs respectively. Therefore, it is possible to compare the drain efficiency of Class-E$_{VS}$ and Class-E PAs by using (15) and (14) assuming that the technology and the design specs are the same. For the designs where the device size is limited [5] to well below the theoretical maximum size $C$ (14) can be used to evaluate the drain efficiency whereas for the designs for which the device size can be chosen freely large (15) can be used for drain efficiency comparison.

In Fig. 3, the loss-factors $(F_I^2 F_V^2/K_P, F_I^2/K_C)$ for Class-E$_{VS}$ are plotted for $0.65 < q < 1.7$ and $k = -1.5, 1.5$ and $k = 0$ (Class-E). It is seen in Fig. 3a that the loss factor $F_I^2 F_V^2/K_P$ for limited device case is the lowest for $k = 0$ (Class-E). For the case in which the optimal transistor size is freely chosen, $k = -1.5$ (Class-E$_{VS}$) has $19\%$ lower loss factor ($F_I^2/K_C$) than $k = 0$ (Class-E). The conclusions derived from Fig. 3 are verified by simulating (Spectre) three PAs designed in 90nm CMOS technology. The condition b) and $C = K_C/(\omega R)$ show that the maximum allowed switch (transistor) size decreases as $\omega$ increases. As it is given in

[5]this may occur at low frequencies where the maximum size is excessively large or for technologies where large devices are prohibitively expensive [6].

| **Design Details** | **Class-E** | **Class-E$_{VS}$** | **Class-E$_{VS}$** |
|---|---|---|---|
| (q,k) | (1.41,0) | (1.35,-1.5) | (1.35,-1.5) |
| Frequency | 40 GHz | 40 GHz | 40 GHz |
| $P_{OUT}, P_{DC}$ | (70.8, 101.2)mW | (110.9, 127.6)mW | (59.2, 107.9)mW |
| $\eta$ | **69.9%** | **86.9%** | **54.9%** |
| $K_P, K_C,$ | 1.365, 0.685, | 1.245, 1.437, | 1.245, 1.437, |
| $K_L, K_X$ | 0.732, 0 | 0.382, -0.163 | 0.382, -0.163 |
| L, C, | 29pH, 0.27pF, | 15pH, 0.57pF, | 15pH, 0.57pF, |
| R, $C_X$ | 9.22 Ω, $\rightarrow \infty$ | 10 Ω, 2.45pF | 10 Ω, 2.45pF |
| Transistor (W/L) | **(0.63mm/0.1u)** | **(1.32mm/0.1u)** | **(0.63mm/0.1u)** |
| Technology | CMOS 90nm | CMOS 90nm | CMOS 90nm |
| $V_{DD}$ | 0.917 V | 1 V | 1 V |
| $Q_L$ | 20 | 20 | 20 |

Table 2: Comparison and design summary for Class-E and Class-E$_{VS}$ PAs

Table 2, in the second column a Class-E PA is designed at a very high frequency on purpose so that $C$ is totally made from the switch (transistor) output capacitance. A Class-E$_{VS}$ PA operating at the same frequency is designed as seen in the third column of Table 2. Since Class-E$_{VS}$ PA has a higher $C$ (2.1 times) a larger transistor width (2.1 times) is used thus a higher $\eta$ is obtained as seen in Table 2; which is supporting the theoretical result given in (15). In the third column, the switch (transistor) for Class-E$_{VS}$ PA is reduced to the same size as Class-E PA and lower efficiency than Class-E PA is obtained; which is supporting the theoretical result in (14).

## IV. Conclusion

In this paper, we have presented the analytical solution for Class-E$_{VS}$ PA with finite dc-feed inductance. Based upon the analytical solution, analytical design equations for Class-E$_{VS}$ PA with finite dc-feed inductance are given; which expands the design space of switching PAs. The given design equations were verified with simulations.

The tolerance to the switch (transistor) output capacitance for Class-E$_{VS}$ PA with finite dc-feed inductance can be $\approx$ 2.1 times more than Class-E PA with finite dc-feed inductance and $\approx$ 7.8 times more than Class-E PA with RF-choke. Therefore, in Class-E$_{VS}$ PA larger switch (transistor) can be used hence higher drain efficiency than Class-E PA can be obtained.

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