A New Test Generation Approach for Embedded Analogue Cores in SoC

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Abstract

This paper proposes a new test-generation approach for embedded analogue cores in SoC. The key features of this approach are the developed testability-analysis based multi-frequency test pattern generation method, the novel PID feedback-based test signal backtrace procedure and the fast tolerance-box propagation algorithm. Moreover, possible DfT solutions are discussed. Finally, this approach has been validated by experiments conducted on a real hardware implementation.

1. Introduction

Applications of mixed-signal devices range across the entire spectrum of electronics, for instance the telecommunication applications, computer peripherals and consumer electronics applications. In order to provide efficient and high quality solutions for those applications, the recent trend in semiconductor manufacturing is the integration of highly complex mixed-signal systems on one single chip, System-on-Chip (SoC) [1][2]. As the number of analog basic cores manufactured in the SoC increases, the overhead of providing test access to each block in terms of primary SoC I/Os, area and performance becomes increasingly unacceptable in practice. Therefore, the limited controllability and observability of the embedded cores is a crucial issue in mixed-signal SoC testing.

On the other hand, due to its complexity, hierarchical approaches are always employed for mixed-signal SoC testing [2][3][4]. In the hierarchical test approach, first, a potential test set for each stand-alone core is generated by using some analogue test-pattern generation method. Then, some test translation schemes are used to convert the core-level test set to the system-level through the use of the existing functional paths or extra DfT circuits.

In this paper, we propose an efficient test generation approach for mixed-signal SoC testing. Compared to other

results in [2][3][4][5], the key features of our approach are the testability-analysis based test pattern generation, PID feedback-based test signal backtrace procedure and sensitivity analysis based tolerance-box propagation. The main advantage of using testability analysis is the reduction of simulation time compared with normal AC analysis, e.g. using the HSPICE simulator. The associated problem of testability for circuits with multiple inputs/outputs is also discussed in our paper. With the proposed PID (Proportional Integral Derivative) feedback [6] based backtrace procedure [7], any kind of test input signals required at the input of the embedded core can be backtraced to the primary SoC inputs and its computational effort is quite low. In order to set the optimal threshold to detect the fault, the tolerance-boxes for the fault-free circuit response and faulty circuit response should be generated. Compared to the traditional tolerance-box generation approach, in which Monte Carlo simulations are performed at transistor level for the complete circuit, our new approach is much faster.

2. Overview of the Proposed Methodology

In our approach, a test set for each embedded core in the system is generated first by a new testability analysis based test-pattern generation method. Next, the test translation scheme is employed to translate the embedded core-level test set into system-level through the existing functional signal paths in the system or some extra DfT circuits. The test translation schemes include the test input signal backward propagation (backtrace), test output response forward propagation and the tolerance-box propagation, as shown in Figure 1.

A multi-frequency test generation technique for detecting catastrophic faults using testability analysis has been developed to generate test signals for stand-alone analogue embedded cores under test. In this method, the testability analysis is performed for the fault-free circuit and for all possible faults from the fault list and the test patterns are generated subsequently.

Figure 1: Overview of system-level SoC testing.

Since the input of an embedded core does not have to be directly accessible from the primary SoC inputs, the backtrace procedure should be used to check whether the test vectors generated for the stand-alone core could be realized by applying a suitable stimulus to a primary SoC input. The backtrace procedure has to determine the required stimulus on the primary SoC inputs which will produce the desired test signal at the input of the embedded core under test. This can be propagated through intermediate cores or the DfT circuits (for instance, the analogue wrapper structure [8][9]) which can potentially transform the input signal. In this paper, a new PID feedback based backtrace procedure [7] is proposed to determine whether it is possible to find the input stimulus to be applied at the primary SoC inputs to get the required test input signal at the inputs of the embedded core and to find the stimulus if it is existing.

The forward test-signal propagation procedure is to propagate the test output response of the embedded core to the primary SoC outputs via the existing functional path or additional DfT circuits since the output response can only be evaluated at the primary SoC outputs. Normally, this procedure can be carried out with a normal circuit simulator.

Due to the fact that the specification of an analogue circuit allows some variations in practice, the tolerance box is a very important issue in analog testing. In order to evaluate the test response at the primary SoC outputs, the tolerance box at the output of the embedded core should also be propagated to the primary SoC outputs during test translation. The traditional approach to obtain the tolerance-box is to perform Monte Carlo simulations at transistor level for the complete circuit in the test path. However, this becomes very CPU-time intensive for SoC. In this paper, a sensitivity-analysis based approach is proposed to reduce the CPU time used for the tolerance-box propagation in mixed-signal SoC testing.

Due to the limited test controllability and observability, it is possible that some embedded cores cannot be completely

tested via the existing functional path, i.e. via other cores. For those embedded cores, a DfT structure should be used to provide the additional test access. In our approach, the ideas developed in IEEE P1500 have been extended for embedded analog/mixed-signal cores [8][9]. By using a wrapper cell structure and analog test bus, the test stimuli can be transported from the external SoC inputs to the inputs of the embedded core, and subsequently the test response can be propagated from the embedded core to the primary SoC outputs. The digital input and output wrapper cells are identical to the ones as suggested within P1500. The new analog input and output wrapper cells have already been developed and the results show that this approach can effectively detect catastrophic as well as parametric faults.

3. Testability Analysis Based ATPG

A. Testability analysis

Conceptually, testability transfer factors (TTF) of components are discussed in [10]. However, the proposed TTF equations in [10][11] give a low sensitivity of TTF on variation of the components, especially for low impedances. Additionally, the derived test patterns are very complex for practical implementation by signal generators.

A new definition of the testability transfer factor of a frequency dependent impedance $Z(\omega)$ is presented [12] to increase the sensitivity for low impedances:

$$T(Z(\omega)) = (1 - \log_{OC}|Z(\omega)|)^a \quad (1)$$

An open circuit (OC) is modeled with a 10MΩ resistance. The parameter a provides an additional possibility to increase (decrease) the sensitivity of the TTF for low (high) values of impedance $Z(\omega)$. Using this approach, any circuit can be described with a signal flow graph (SFG). For further analysis, the SFG of a circuit with n nodes will be described with a matrix $A(n,n)$, where $A(i,j)$ has a value equivalent to the TTF fan-in from node j to node i . From (1) one can derive:

$$Z(\omega) = OC^{1-T(Z(\omega))^{1/a}} \quad (2)$$

From the equation for equivalent impedance of parallel-connected impedances and equation (2), a value Te for an equivalent TTF (parallel connection of n fan-in/outs), can be constructed:

$$Te = (1 + \log_{OC} \sum_{i=1}^n OC^{(Ti)^{1/a}-1})^a \quad (3)$$

If the contribution of node j , with controllability C_j , to the controllability of node i is defined as $A(i,j)*C_j$, values for controllability (C_i), observability (O_i) and testability (T_i) for node i can be found by using the following equations (4-6). The measures for all three properties of nodes are normalized to range between 0.0 (minimum) and 1.0 (maximum).

$$C_i = (1 + \log_{OC} \sum_{j \neq i} OC^{(C_j * A_{i,j})^{\frac{1}{a}} - 1})^a \quad (4)$$

$$O_i = (1 + \log_{OC} \sum_{j \neq i} OC^{(O_j * A_{j,i})^{\frac{1}{a}} - 1})^a \quad (5)$$

$$T_i = \sqrt{C_i * O_i}, \quad i = [1, \dots, n] \quad (6)$$

Systems of nonlinear equations like (4) and (5) can be solved using the Newton-Raphson method. In order to speed up CPU time, the method is modified in such way that the matrix of the partial derivatives (Jacobian) is found directly. The values for the controllability of the primary inputs and the observability of the primary outputs are 1.0 by default. For that reason, the values for the testability of the primary inputs and the testability of the primary outputs are only dependent on the observability and the controllability of the nodes respectively.

The obtained values for the testability of nodes are associated with the primary input and primary output. For circuits with multiple inputs/outputs one input node has to be chosen as primary input, and one output node has to be chosen as primary output. Finally, the testability of a node will be the maximum obtained value for the testability of that node for all possible choices.

B. Example circuit

In order to validate our approach, a fully integrated continuous time filter for audio applications [13] is used for the circuit under test (Figure 2). This so-called Tow-Thomas Biquad section is consisting of four operational transconductance amplifiers (OTAs) and integrated capacitors.

The filter is implemented with fully differential inputs and outputs in 0.8 μ m AMS CMOS technology. The bias current for these OTAs is 200nA which defines the frequency output characteristic of the filter. The center frequency f_c of the band-pass output is set on 13.4kHz and cutoff frequency of the low-pass output f_{cutoff} is 18kHz.

Figure 2: The Tow-Thomas Biquad filter based on Operational Transconductance Amplifiers (OTAs) [13].

The filter is described with a SPICE netlist and a list of primary input/output nodes. By analyzing the netlist of the benchmark circuit with a program based on testability analysis, the circuit is transformed into a SFG. The testability of each node in the circuit is found for the complete frequency range of the filter, using eight points per decade and 5Hz for the start frequency. A list of nodes with the lowest testability for the fault-free case and associated values for testability are listed in the Table 1.

Table 1: List of nodes with the lowest testability in the filter.

Node	Position	Testability
NET11	OTA1	0.5277
NET11	OTA2	0.5671
NET20	OTA1	0.6000
NET37	OTA1	0.7209
NET37	OTA2	0.7211

Two types of faults are used in the fault list: bridging faults between nodes modeled with a resistance of 500 Ω and interconnection faults modeled by a serial resistance. The testability analysis is performed for all possible faults from the fault list for the complete frequency range. An error function is defined as the difference between the testability for the faulty and the fault-free case of the node where the fault occurred. If the error function for a frequency is under a predefined threshold, then that test signal frequency can be used for detecting that fault in the circuit.

Figure 3: The transistor schematic of the Operational Transconductance Amplifier with a bridging fault Rb.

As seen from the Table 1, node NET11 in the amplifier OTA1 is the node with the lowest testability. A bridging fault on that node can be considered as a worst-case bridging fault. In that case the band-pass output (out_BP) is considered as primary output and a bridging fault Rb is inserted as depicted in Figure 3.

Figure 4: a) Measured test stimulus generated by the AWG. b) Simulation results for test output for fault-free and faulty case as response of a).

For the detection of this fault, the next two frequencies have been calculated: $f1=13.3\text{kHz}$ and $f2=17.7\text{kHz}$. For the test stimulus, a multi-frequency signal is generated from two

sine waves with frequencies $f1$ and $f2$. According to specification of the filter, the DC offset of the test signal is set to 1.3V, equal to value of the V_{ref} , and a magnitude of the 50mV is calculated for both. The resulting test stimulus can be generated using an Arbitrary Waveform Generator (AWG) as can be seen in Figure 4(a). The simulation results for fault-free and faulty embedded cores are presented in Figure 4(b).

4. Backtrace Propagation

The main previous results on backtrace methods have been presented in [4][14][15][16]. The method proposed in paper [4] needs a lot of computation. In [14], the authors use the modified node analysis formulation and swap the variables of solution to determine an input signal which will produce the desired signal at the output. In this method, the desired waveform is required to be in the feasible signal space so that a solution exists. In [15], the authors present an approach for backtrace based on the use of signal flow graphs. However, this has limited applicability to linear circuits. The feedback-driven backtrace method proposed in [16] is quite simple. However, since only a proportional gain is used in the feedback, it has the following disadvantages: the steady state error is large if the gain is small and the loop becomes unstable if the gain is too large. According to feedback control theory [6], a PID (Proportional Integral Derivative) controller can be used in the feedback to solve this problem.

The proposed PID feedback-based backtrace structure is shown in Figure 5. In the figure, MODULE 1 stands for all the circuits between the primary SoC input and the input of the embedded core under test. MODULE 1 could be one core or the combination of some cores or some DfT circuits. During the backtrace procedure, in order to save simulation time, the embedded core under test is disconnected with MODULE 1 and the input impedance of core under test is connected at the output of MODULE 1 as the load, as shown in Figure 5. Normally, this input impedance of the core under test can be found in the data sheet provided by the core provider. Now, apply the desired test input signals for the embedded core to the input of the feedback loop at point (A), and then perform the circuit simulation on the structure as shown in Figure 5. Afterwards, at point (B), the required stimulus at primary SoC inputs is available if this stimulus exists.

If during the above-mentioned backtrace procedure the suitable stimulus cannot be found, then it means that this test vector cannot be realized with the existing functional path. In this case, this test vector can be deleted if other test vectors can also detect the faults in the embedded core detected by this test vector. If some faults in this embedded core can only be detected by this test vector, then additional DfT circuits

(for instance, the DfT structure proposed in [8][9]) should be employed to get additional test access.

Figure 5: The proposed PID feedback-based backtrace structure.

From a mathematical point of view, the PID algorithm can be described as:

$$u(t) = K_P e(t) + K_I \int_0^t e(\tau) d\tau + K_D \frac{de(t)}{dt} \quad (7)$$

where $e(t)$ is the error between the desired signal and the output signal of MODULE1, $u(t)$ is the output signal of PID controller, and K_P , K_I and K_D are the control parameters of the proportional action, integral action and derivative action respectively. Basically, the output signal of a PID controller is a sum of three terms: the P-term (which is proportional to the error), the I-term (which is proportional to the integral of the error) and the D-term (which is proportional to the derivative of the error).

According to the PID feedback control theory [6], the purpose of the derivative action is to improve the closed-loop stability and the function of the integral action is to make sure that the output of the MODULE1 is same as the desired signal (i.e. $e(t) \rightarrow 0$). Moreover, the influence of the noise in the feedback loop can be very small because of the integral action. Therefore, our approach can ensure that the stimulus can be found if it exists and the desired test input signal can be obtained at the input node of the embedded core under test by applying the resulted stimulus at the primary SoC input.

With regard to the computational effort of our approach, during the backtrace procedure simulation, the PID feedback structure as shown in Figure 5 can be implemented using a high-level language, for instance, Verilog-A and VHDL-AMS. Therefore the computational effort will be very low.

In order to verify the viability of the proposed approach, an experiment was carried out on part of a locally designed system-on-chip, as shown in Figure 6, which includes a pre-amplifier, a continuous time filter (FILTER) and a voltage-current converter (VIC). In this example circuit, the FILTER is the embedded core under test and its details are given in section 3. The schematic of the opamp used in the pre-

amplifier and the VIC is shown in Figure 7. Based on the opamp shown in Figure 7, a noninverting operational amplifier with resistive feedback is constructed for the pre-amplifier (gain=2). The VIC is built based on the negative feedback amplifier structure. For the stand-alone FILTER, the testability analysis based test pattern generation approach is used to generate the potential test vectors, as discussed in section 3. Among these potential test vectors, the test input signal for one test vector is the combination of two sine waves, one 13.3kHz sine signal (AC amplitude is 50mV and DC offset is 1.3V) and one 17.7kHz sine signal (AC amplitude is 50mV and DC offset is 1.3V). Since the input of FILTER cannot be directly accessed via the primary SoC input, the backtrace procedure should be employed to find the stimulus at the primary SoC input that can provide the required test input signal at the input node of the FILTER.

Figure 6: The general structure of the example circuit.

Figure 7: The schematic of the opamp used in the pre-amplifier and VIC.

The structure of the PID feedback-based backtrace approach used for our example circuit is shown in Figure 8. With regard to the load impedance, based on the specification of FILTER, it is the combination of one resistor (1M Ω) and one capacitor (1pf). In the figure, $V_{desired}$ is the desired test input signal for the FILTER, i.e.. the combination of two sine signals as described in the previous paragraph. In our simulation, the pre-amplifier is simulated at transistor level and the rest of the backtrace structure is

simulated using the high-level language Verilog-A in Cadence.

Figure 8: The feedback loop for the backtrace procedure of the example circuit.

The transient simulation results of the backtrace structure shown in Figure 8 are presented in Figure 9. In Figure 9, the desired test input signal ($V_{desired}$) at the input node of the FILTER, the resulting signal to be applied at the primary SoC input (V_{chip_in}) and the signal at the output of the pre-amplifier (V_{core_in}) are shown. The goal of the backtrace procedure is to find the suitable V_{chip_in} to make the V_{core_in} to be as close as possible to the desired test input signal $V_{desired}$.

The results in Figure 9 show that the output signal of the pre-amplifier, V_{core_in} , is very close to the desired test input signal, $V_{desired}$, when the resulting stimulus, V_{chip_in} , is applied to the primary SoC input. In other words, during chip testing, if the resulted V_{chip_in} as shown Figure 9 is applied to the primary SoC input, then the desired test input signal, $V_{desired}$, can be obtained at the input of the FILTER. Moreover, from a test controllability point of view, the results in Figure 9 also mean that this test vector can be realized with the existing function path and no additional DfT circuits are required for this test vector.

Figure 9: The results of the backtrace simulation.

In order to evaluate the computational effort of our PID feedback based backtrace approach, the CPU time used for the backtrace procedure and the simulation of pre-amplifier only with same input signal are listed in Table 2. Both

simulations are carried out with the same HP workstation and simulator. According to the data in Table 2, the computational effort for our approach is quite low and it is quite acceptable in practice.

Table 2: CPU time comparison.

	CPU time for transient analysis	Total CPU time for transient analysis, input and output
Pre-amplifier only	0.84s	1.1s
PID feedback with pre-amplifier	1.2s	1.6s

Although the example circuit used in this paper is quite simple, the results presented in Figure 9 still verified the correct function of our proposed PID feedback based backtrace approach. In our future work, examples with more complex cores will be used, instead of the simple pre-amplifier core.

5. Tolerance-Box Propagation

Because the tolerance-box generation is necessary to set the optimal threshold to detect the fault in analogue testing, in this section, the sensitivity-based tolerance-box propagation method is proposed to reduce the CPU time used for the tolerance-box generation of linear circuits with small signals. Suppose that $f(p_1, p_2, \dots, p_n)$ is the circuit output performance function with parameters $p_i (i = 1, 2, \dots, n)$ and each parameter has a maximal deviation $|\Delta p_i|$, then the lower and upper bounds of f under parameter deviations can be estimated as [17][18]:

$$f_{\min} = f_0 - \sum_{i=1}^n |s_{p_i}^f| \cdot |\Delta p_i| \quad (8)$$

$$f_{\max} = f_0 + \sum_{i=1}^n |s_{p_i}^f| \cdot |\Delta p_i| \quad (9)$$

where f_0 is the nominal value of the performance function and $s_{p_i}^f$ is the sensitivity of f with respect to p_i . Normally, the tolerance-box is defined as the band for all the possible circuit output performances when the parameters are changed with all the possible small values. Therefore, the tolerance box can be estimated with the band $[f_{\min}, f_{\max}]$.

In order to carry out tolerance-box propagation, the concept of normal sensitivity is extended to the *input sensitivity* in our approach. The *input sensitivity* is defined as the deviations of the circuit performance around the nominal value with regard to the corresponding input deviation around the nominal value.

Figure 10: The illustration of the system structure with different sorts of parameter deviations.

To illustrate our approach, as an example without loss of any generality, core A, core B and core C are connected as shown in Figure 10. In Figure 10, $\Delta p_i^G (i=1,2,\dots,n)$ are the deviations of the possible *global* parameters for all the cores (G). $\Delta p_i^A (i=1,2,\dots,n_A)$, $\Delta p_i^B (i=1,2,\dots,n_B)$ and $\Delta p_i^C (i=1,2,\dots,n_C)$ are the deviations of the *local* parameters for core A, core B and core C, respectively. Moreover, the deviations Δp_i^G , Δp_i^A , Δp_i^B and Δp_i^C are made to be mutually independent when the model is constructed. After some mathematical derivations [19], one can derive

$$|\Delta w| = \sum_{i=1}^n |s_{G,i}^C \cdot s_{in}^C \cdot s_{G,i}^B + s_{in}^C \cdot s_{in}^B \cdot s_{G,i}^A| \cdot |\Delta p_i^G| + \sum_{i=1}^{n_C} |s_i^C| \cdot |\Delta p_i^C| + \sum_{i=1}^{n_B} |s_{in}^C \cdot s_i^B| \cdot |\Delta p_i^B| + \sum_{i=1}^{n_A} |s_{in}^C \cdot s_{in}^B \cdot s_i^A| \cdot |\Delta p_i^A| + |s_{in}^A \cdot s_{in}^B \cdot s_{in}^C| \cdot |\Delta x| \quad (10)$$

where $s_{G,i}^A$, $s_{G,i}^B$, $s_{G,i}^C$, s_i^A , s_i^B , s_i^C are the corresponding sensitivities with regard to the global parameters and local parameters, and s_{in}^A , s_{in}^B , s_{in}^C are input sensitivities. According to equation (8) and equation (9), the final tolerance box for the whole test path with core A, core B and core C is

$$[w_0 - |\Delta w|, w_0 + |\Delta w|] \quad (11)$$

where w_0 is the nominal value of the circuit output performance with nominal parameters and $|\Delta w|$ is calculated using equation (10).

In the above derivation, only three analogue cores are connected as shown in Figure 10. For the case that more than three cores are connected in serial, the same propagation procedure can be employed to calculate the final tolerance box.

Compared to the traditional tolerance-box generation approach, in which Monte Carlo simulations at transistor level are performed for the complete circuit, our new approach has two advantages. The first advantage is that the sensitivity analysis is not computationally expensive [17][18]. The second advantage is that the simulation time can be reduced because a single large SoC is divided into a number of smaller cores and the simulation is performed for these smaller cores. The simulation results presented in [19] show that this approach is quite effective. The disadvantage of this method is that it can only be applied to small signals.

For our example circuit as shown in Figure 6, the following steps have to be used to carry out the tolerance-box propagation. First, the sensitivity analysis is conducted for each standalone embedded core, i.e. the pre-amplifier, the FILTER and the VIC. Then, by using equation (10) and equation (11), the tolerance-box for the corresponding test response at primary SoC output can be obtained. Finally, with the tolerance-box for the fault-free circuit response and faulty-circuit response, the optimal threshold for testing can be calculated.

6. Experimental Results

In order to verify the basic principles of our new analogue structural test-signal generation for an embedded core, the improved test-signal backtracing to primary SoC inputs, the response signal forward propagation to primary SoC outputs, and the new algorithm for overall tolerance-box calculation, several hardware experiments have been carried out.

The vehicle used, being a front-end for audio-range purposes, is part of a SoC and consisting of two pre-amplifiers, an embedded programmable (differential) band-pass filter built-up from four OTAs and embedded capacitors, and an operational amplifier serving as voltage-to-current converter (VIC). The filter has a (programmable) center frequency of 13.4 kHz and a bandwidth of 12.43 kHz. The basic (block as well as transistor-level) schemes of the preceding, embedded and succeeding cores can be found in the previous paragraphs (Figures 2, 3, 6, 7).

The IntegraTEST verification test system has been used as test environment. This is a hardware and software

platform for VXI-based measurement subsystems developed by Microlex Systems and Integrated Measurement Systems (IMS). A small part of this system is shown in Figure 11. The basic hardware architecture consists of all VXI modules which are inside the VXI mainframe rack and incorporates the slot 0 controller.

Figure 11: The basic test set-up for the experiments, using the IntegraTEST verification tester.

The test controller workstation includes software programs required to control all tests. Among others, it consists of a program to import, generate/adapt and visualize mixed-signal waveforms (WaveMAKE), the test-programming environment LabVIEW and LabVIEW VI's (Virtual Instruments). The VXI instrument modules used in this experiment are the HP1445 arbitrary waveform generator (AWG) and the HP1428 signal digitizer.

The HP1445 AWG has a resolution of 13 bits including a sign bit. The maximum output rate is 42.9 MSa/s. It includes two low-pass Bessel-Thompson reconstruction filters, which can be by-passed if required.

The HP1428 is a high-speed digitizer. This is basically an AD converter, which receives the signal and digitizes it at a maximum rate of 1Giga sample per second (1Gsa/s). For the experiments, the real-time acquisition mode has been used. The sensitivity range is from 8mV to 40 V full scale with a resolution of 0.4% (8 bit A/D). A first-in-first-out (FIFO) memory stores the numerical values as the AD converter digitizes the signal. The memory has a depth of 8000 points.

The experiments have been conducted as follows. First, the local test-signal generator (section 3) is used to derive a signal to detect a specific fault in an embedded analogue core. It also provides the resulting output signal of the core. In our case, a parametric (resistive) fault has been chosen in

the second OTA (OTA2) of the filter (Figure 2). It has been assumed that a serial resistance of 3 k Ω is present in the control line of the bias current I_b (Figure 3).

Figure 12: Measurement results: a) applied (generated) test signal to primary SoC input. b) measured primary output of SoC if embedded core is fault-free. c) measured primary output of SoC if embedded core is faulty. d) detectable error signal between primary outputs b) and c).

Next, these generated input and output signals are used as input for the backtracing and forward propagation procedure as discussed in section 4. These procedures result in a new test signal at the primary input of the SoC and an expected signal at the primary output of the SoC.

Simultaneously, tolerance-box calculations are carried out, according to section 0, to provide the accepted tolerance band at the primary output of the SoC. This makes a proper distinction between fault-free and faulty signal possible. The test signal is subsequently imported in WaveMAKE from the CAD workstation, on which the previous software tools have been implemented (Figure 11). Then this signal is converted

to control the AWG, which provides the actual signal. This (measured) signal is shown in Figure 12a.

The output of the voltage-to-current buffer after the filter is designated to be a primary output of the SoC. The result in the case the embedded filter core is fault-free is shown in Figure 12b. Next, the chosen fault in the filter has been emulated in hardware by means of an additional resistor of 3 k Ω in the biasing current I_b of OTA2 (Figures 2, 3). The same measurement as the previous one has been carried out, and the result of the faulty filter core is shown in Figure 12c.

In order to stress the differences, the measured data of the faulty and fault-free primary output responses are subtracted in the test program. The result is shown in Figure 12d. As can be seen, this difference is sufficient to detect the fault, in the presence of accepted tolerances.

7. Conclusions

In this paper, an efficient test generation approach for analogue embedded cores in mixed-signal SoC has been proposed. Compared to other published results, our approach has a number of advantages. First, the simulation time for analogue test-pattern generation has been reduced by using the testability analysis based method. Second, the proposed tolerance-box propagation approach is faster than the traditional tolerance-box generation based on Monte Carlo simulations at transistor level for the complete circuit. Finally, the fast PID feedback-based backtrace procedure is suitable for any kind of test input signals. The presented measurement results on our vehicle show that our approach is correct and effective.

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References:

- [1] N. Nagi, "System-on-a-chip mixed-signal test: issues, current industry practices and future trends," *Proceedings of 5th International Mixed Signal Testing Workshop*, Whistler, BC, Canada, pp. 201-211, 1999.
- [2] S. Ozev, I. Bayraktaroglu and A. Orailoglu, "Test synthesis for mixed-signal SOC paths," *Proceedings of DATE*, pp. 128-133, 2000.
- [3] R. Voorakaranam and A. Chatterjee, "Hierarchical test generation for analog circuits using incremental test development," *Proceedings of VTS'99*, pp. 296-301, Dana Point, CA, April 1999.
- [4] A. V. Gomes and A. Chatterjee, "Robust optimization based backtrace method for analog circuits," *Proceedings of ICCAD*, pp. 304-307, 1999.
- [5] J. L. Huang, C. Y. Pan and K. T. Cheng, "Specification back-propagation and its application to DC fault simulation for analog/mixed-signal circuits," *Proceedings of VTS'99*, pp. 220-225, 1999.
- [6] K. Astrom and T. Hagglund, "PID controllers: theory, design and tuning," Instrument of Society America, ISBN:1-55617-516-7, USA, 1995.
- [7] L. Fang and H. G. Kerkhoff, "PID feedback based backtrace method," *Proceedings of 8th IEEE International Mixed-Signal Testing Workshop*, Montreux, Switzerland, pp. 147-152, 2002.
- [8] L. Fang, M. Stancic and H. G. Kerkhoff, "Mixed-signal core-based testing," *Proceedings of European Test Workshop (ETW)*, Cascais, pp. 279-280, 2000.
- [9] M. Stancic, L. Fang and H. G. Kerkhoff, "Detecting parametric faults in embedded cores of mixed-signal ICs" *Proceedings of 6th IEEE International Mixed-Signal Testing Workshop (IMSTW)*, Montpellier, France, pp. 20-21, June 21-23, 2000.
- [10] S. D. Huynh, S. Kim, M. Soma and J. Zhang, "Testability analysis and multi-frequency ATPG for analog circuits and systems," *Proceedings of ICCAD*, pp. 376-383, 1998.
- [11] S. D. Huynh, S. Kim, G. Devarayanadurg and M. Soma, "Efficient test set design for analog and mixed-signal circuits and systems," *Proceedings of Asian Test Symposium (ATS)*, pp. 239-244, 1999.
- [12] M. Stancic and H. G. Kerkhoff, "Test generation for mixed-signal circuits using testability analysis," *Informal proceedings of the 7th European Test Workshop (ETW02)*, Corfu, Greece, pp. 249-254, 2002.
- [13] A. Yufera and A. Rueda, "Programmable low-voltage continuous time filter for audio applications," *Proceedings of IEEE International Symposium on Circuits and Systems*, Orlando, USA, pp.200-203, 1999.
- [14] R. Ramadoss and M. L. Bushnell, "Test generation for analog circuits using partitioning and inverted system simulation," *Proceedings of International Mixed-Signal Testing Workshop (IMSTW)*, pp. 68-73, June 1998.
- [15] R. Ramadoss and M. L. Bushnell, "Test generation for mixed-signal devices using signal flow graphs," *Journal of Electronic Testing: Theory and Applications*, no. 14, pp. 189-205, 1999.
- [16] R. Voorakaranam and A. Chatterjee, "Feedback driven backtrace of analog signals and its application to circuit verification and test," *Proceedings of 20th Anniversary Conference on Advanced Research in VLSI*, pp. 342-358, 1999.
- [17] C. J. R. Shi and M. W. Tian, "Simulation and sensitivity of linear analog circuits under parameter variation by robust interval analysis," *ACM Transactions on Design Automation of Electronic Systems*, vol. 4, no. 3, pp. 280-312, July 1999.
- [18] J. Vlach and K. Singhal, "Computer methods for circuit analysis and design," New York: Van Nostrand Reinhold, 1994.
- [19] L. Fang and H. G. Kerkhoff, "Sensitivity Analysis Based Tolerance-Box Generation and Propagation in Mixed-Signal SoC Testing," *Informal proceedings of the 7th European Test Workshop (ETW02)*, Corfu, Greece, pp. 255-260, 2002.