Performance, Improvement and Perspective Application of an All-Optical Shift Register

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Abstract: An all-optical shift register based on Self Electro-Optic Effect Devices is introduced. The switching behavior, system performance and some possible improvements are presented. Calculations show the system bit rate could be up to 790 Mbps with 1 mW clock power. An improved scheme is discussed, which can provide 2 Gbps throughput for 1 mW clock power. Finally we presented an application of this all-optical shift register in fast photonic packet switching.

Introduction

Perhaps the most interesting research area in photonics switching optoelectronic devices is the quantum well Self Electro-optic Effect Devices (SEEDs). SEEDs works on the changing optical absorption which is dependent on the changing electrical field perpendicular to the thin semiconductor layers in quantum well material. The physics of the SEED has been presented in many papers. In this paper, an all-optical shift register based on SEEDs, which is certainly the heart of an all-optical switch, is presented. Based on master-slave system configuration, the switching behavior and the system performance is analyzed, and the system bit rate is calculated as well. Based on these results, Some simulations for the dependence of the system bit rate are given, some factors on optimization of system performance are discussed. Based on these results, an improved all-optical shift register is presented, which can provide 2 Gbps system throughput for 1 mW clock power. It is shown that the design of this all-optical shift register is a compromise, higher power clock beam, devices with optimum absorption coefficients in the "high" and "low" states while minimum applied electrical field will exhibit better performance.

All-optical shift register based on SEEDs

The shift register will be implemented by optical integrated chip; it is made up of a number of memory cells, which are cascaded as master-slave configuration, and is operated in a time sequential manner as shown in Fig.1. In a single memory cell, a pair of lower input signals set the state of the S-

SEEDs, the higher power clock beams will be injected to read out the state of the S-SEEDs. The further detail of this all-optical shift register can be found in [1].

Fig.1 All-optical shift register implemented by S-SEED's

System bit rate

The system bit rate is limited by the time it takes the photocurrent to charge the capacitance of the four SEEDs in one memory cell. This photocurrent is proportional to the optical power incident on the device windows. The system bit rate can be found by first determining the absolute powers from the output of the preceding memory cell, which are incident on the first stage devices, and then calculating the switching time of the first stage devices from these inputs. In the same way, the second stage devices switching time can be calculated by determining the clk/clk powers.

The System bit rate can be given as:

$$B = \frac{1}{2kCV_0} \left\{ \left[\frac{1}{P_{clk}} + \frac{1}{P_{clk}} \right] \right. \\ \left. \left[\frac{1}{T_{op}T_{on}(1-T_{on}) - T_{op}T_{off}(1-T_{off})} + \frac{1}{T_{op}T_{on}(1-T_{off}) - T_{op}T_{off}(1-T_{on})} + \frac{2}{(T_{on}-T_{off})} \right] \right\}^{-1} \quad (1)$$

Here $k = hv/q$, hv is the photo energy; q is the charge of an electron; C is the capacitance of a single SEED.

T_{on} is the high transmission coefficient; T_{off} is the low transmission coefficient. P_{clk} and P_{clk} are the clock power injected onto the SEED cell windows, T_{opt} is the passive waveguide connection efficiency between adjacent memory cells.

$C=12.5\text{fF}$, $V_0=2\text{V}$, $T_{on}=41\%$, $T_{off}=17\%$, $P_{clk}=P_{clk}=1\text{mW}$ and $T_{opt}=55\%$ for the sample supplied by our partner, the system throughput can be 460 Mbps then. However, the system throughput can be up to 790 Mbps with transmission states of 60% and 10%.

Discussion

When $\frac{1}{2kCV_0}\{[\frac{1}{P_{clk}}+\frac{1}{P_{clk}}]\}^{-1}$ is replaced by a

constant, the system bit rate in Eq.(1) can be looked as the relative bit rate B_r , Fig.2 and Fig.3 are based on

$\frac{1}{2kCV_0}\{[\frac{1}{P_{clk}}+\frac{1}{P_{clk}}]\}^{-1}=4\text{s}^{-1}$ and $T_{opt}=1$. There is an

optimum transmission difference for the better system performance, for example, in Fig2, the bit rate of transmission states of 60% and 10% would yield a higher system bit rate than that of 80% and 10%. The optimum bit rate is with transmission states of 66.5% and 0 giving a maximum relative bit rate of 0.44. When T_{on} varying from 50% to 80% and T_{off} equal to 0, the relative bit rate is within 1% of this optimum. From Fig.2 we can see the decrease in T_{off} will bring us greater improvement, especially in optimum area. Some improvement proposed in [5] will produce devices with transmission states of 60% and 10%, this will yield the relative bit rate of 0.32, 72% of that optimum.

Fig.2 The relative bit rate B_r dependence with transmission coefficients

Considering the relationship between the absorption coefficients $a_{on(off)}$ and transmission coefficients $T_{on(off)}$, $-a_{on(off)}L = \ln T_{on(off)}$, L is the thickness of the multiple quantum well region of the device. The system speed dependence with absorption

coefficients is shown in Fig.7. We can see $a_{on(off)}L$ has more influence to the relative bit rate.

Fig.3 The relative bit rate B_r dependence with absorption coefficients

An improved scheme

Based on the system performance analysis of the all-optical shift register, here we presented an improved scheme of the all-optical shift register shown in Fig.4. We combine the two stages S-SEED as a single S-SEED in a memory cell; the optical input signal and optical clock signal are coupled by an effective waveguide coupler. So there are two SEEDs in a memory cell instead of four. By this way, half amount of the SEEDs can be saved; the capacity that needed to be charged by photocurrent will be reduced to half amount; the capacity introduced by the electrical connection will be decreased;

Fig.4 an improved all-optical shift register

This all-optical shift register operated in a time sequential manner. The lower power input signal that get from previous stage set the switching state; then the higher power clock signals are applied to read the state to the next stage. This operation bring the time sequential gain. The switching time of a stage is determined by the input signals set the switching states, the time that clock signal read out the states can be neglected.

The system bit rate of the improved all-optical shift register is given as:

$$B = \frac{1}{kCV_0} \left\{ \left[\frac{1}{P_{clk}T_{cpl}} + \frac{1}{P_{clk}T_{cpl}} \right] + \frac{1}{T_{opt}T_{on}(1-T_{on}) - T_{opt}T_{off}(1-T_{off})} + \frac{1}{T_{opt}T_{on}(1-T_{off}) - T_{opt}T_{off}(1-T_{on})} \right\}^{-1} \quad (2)$$

Here T_{cpl} is the coupling efficiency of the waveguide coupler applied before the SEED window. When applied with a lossless waveguide coupler, $T_{cpl}=1$. With $C=12.5$ fF, $V_0=2$ V, $T_{cpl}=50\%$, $T_{on}=41\%$, $T_{off}=17\%$, $P_{clk}=P_{clk}=1$ mW and $T_{opt}=55\%$, the system throughput put can be 610 Mbps, however if a lossless waveguide coupler is applied, the system throughput put can be 1.2 Gbps. With the higher contrast transmission coefficients 60% and 10%, the system throughput is 1 Gbps, and 2 Gbps is possible with lossless waveguide coupler.

Application

The all-optical shift register we presented here can be used to construct optical memory for data storing, optical wavelength converter, optical modulator, but the most interesting application is to construct an optical switch.

For instance, an 848 S-SEEDs array can be used to store the 424 bits ATM cell data. Optical connections (i.e. passive optical waveguides) are integrated between two neighbor memory cells. The clock signals of CLK and $\overline{\text{CLK}}$ can be generated by current modulating two laser diodes. After the two clock signals are coupled into the chip, they can be splitted by integrated beam splitters into 424 CLK and 424 $\overline{\text{CLK}}$ signals, which are connected to the odd memory cells and even memory cells respectively. "Data in" and "Ref" signals can be coupled into the first S-SEED optical window by a coupling system, the input signals and optical clock signals are coupled to SEED window by an effective waveguide coupler. An ATM switch controller provides the cell header translation, routing function by reading and writing the all-optical shift register.

Conclusion

In this paper, we proposed an all-optical shift register, which can be the heart of an optical switch. The switching behavior and the system bit rate are presented, the first stage in one memory cell will have more influence than the second stage, especially for the switching process V_b changing from zero to $V_0/2$. The system bit rate is also relative to the clock beam power; higher power clock beam, devices with optimum absorption coefficients in the "high" and "low" states while minimum applied electrical field

will exhibit better performance. An improved scheme was shown by combine two parallel S-SEEDs as a S-SEEDs, this improvement reduces the devices amount, decreases the device capacity, decreases the introduced capacity. A 2 Gbps system throughput can be achievable by using lossless waveguide coupler. Faster circuits are possible by producing smaller devices, but there will be many optical and optomechanical constraints. The initial input signals do not have much influence on the system performance except for the first memory cell.

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