A CMOS Wideband Linear Current Attenuator with Electronically Variable Gain

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Abstract - In this paper a CMOS highly linear current attenuator is described. The circuit is suited for both differential and single input currents. The current gain is electronically variable between -1 and +1 by means of two controlling currents. A simple additional circuit is described to obtain a gain that is linearly dependent on a single control current. Then the circuit can be used as a four-quadrant current multiplier.

The current attenuator was realized in a standard 2.5 μm CMOS process using channel lengths of 5 μm . The measured nonlinearity is less than 1% over the entire input current range. Simulations indicate a feasible -3dB bandwidth of over 100 MHz.

I. INTRODUCTION

Variable gain circuits and analog multipliers are useful building blocks with many applications. In this paper a wideband CMOS current attenuator is presented, which can easily be extended to perform a four-quadrant current multiplication. The circuit consists of two interconnected MOS translinear loops [1] and is therefore insensitive to temperature or process variations. Furthermore, the circuit is insensitive to the body effect and therefore it is not necessary to place transistors in individual wells, which results in a relatively large bandwidth. The current gain of the attenuator is electronically variable between -1 and +1 by means of two controlling currents. The input currents of both the attenuator and the four-quadrant multiplier circuit may be differential or single currents.

II. CIRCUIT PRINCIPLE

The operation of the circuit is explained by first considering the stacked transistor structure shown in fig. 1(a). This circuit has been analyzed extensively [2]. The sum of the gate-source

voltages of transistors M₁ and M₂ is kept constant and equal to a reference voltage V_{bias} . The differential output current of the circuit is equal to the input current. In [2] it was shown that the input resistance of the circuit is dependent only on the bias voltage V_{bias} and independent of the input current. A simple circuit to generate V_{bias} is shown in fig. 1(b). In fact, by using this circuit we close the translinear loop formed by M₁, M₂, M₃ and M₄. Using a simple square-law transistor model:

$$I_d = k (V_{gs} - V_{th})^2, \quad \text{with } k = \frac{1}{2} \mu C_{ox} \frac{W}{L}, \quad (1)$$

it can be shown that the input resistance is given by [2]:

$$R_{in} = \sqrt{\frac{1}{16kI_{bias}}} \quad (2)$$

If we could connect the inputs of two of these circuits in parallel, then the input current would be distributed between the two circuits in a way determined by the values of the input resistances and thus by the values of the bias currents. The current distribution could then be controlled by changing the values of the bias currents. However, the input node of the circuit in fig. 1(a) also carries a dc-voltage equal to half of V_{bias} . Therefore, a parallel connection of two of these circuits is only possible if the bias voltages are equal.

A circuit that does not have this limitation is shown in fig. 2. In this circuit, the translinear loop M₁..M₄ is arranged in an "up-down" topology [1]. Just as in fig. 1 the transistors M₃ and M₄ conduct the constant current I_{bias} . The current mirror M₅, M₆ is used to force the difference between the drain currents of M₁ and M₂ equal to the input current I_{in} , as is the case in fig. 1(a). Now, the input resistance R_{in} (eqn. (2)) is not given with respect to ground, but it is the differential input resistance between the nodes A and B. In fig. 2 the input current may be a

single current as shown, but it can also be a differential current between the nodes A and B. A common mode input current at nodes A and B is eliminated by the current mirror M5, M6.

A fully symmetrical circuit with an improved high frequency behavior is obtained by replacing the current mirror M5, M6 by two mirrors connected anti-parallel. This is shown in fig. 3.

The circuits of figures 2 and 3 do not have a bias voltage between their input nodes A and B. Therefore, two circuits can be placed in parallel, as illustrated in fig. 4(a). The input current will now be distributed between the two circuits depending on the values of their input resistances. A part I_{in1} will flow into one subcircuit and a part I_{in2} will flow into the other subcircuit:

$$I_{in1} = I_{in} \frac{R_{in2}}{R_{in1} + R_{in2}} \quad (3)$$

$$I_{in2} = I_{in} \frac{R_{in1}}{R_{in1} + R_{in2}} \quad (4)$$

The differential input resistances R_{in1} and R_{in2} are dependent on the corresponding bias currents I_{b1} and I_{b2} according to (2). In fig. 4(a) the outputs of the two subcircuits are cross-coupled. Therefore, the differential output current I_{out} will be equal to the difference between the differential output currents of the subcircuits:

$$I_{out} = I_{out1} - I_{out2} = I_{in1} - I_{in2} \quad (5)$$

fig. 2 A circuit performing the same function as the circuit of fig. 1. The loop of transistors is now arranged in an "up-down" topology. The constant input resistance is now a differential input resistance between nodes A and B.

fig. 1 A simple stacked transistor structure (a) with an input resistance R_{in} which is independent of the input current. The simple circuit consisting of two diode-connected transistors (b) can be used to generate the bias voltage V_{bias} .

Substituting (3) and (4) into (5) results in:

$$I_{out} = I_{in} \left\{ \frac{R_{in2} - R_{in1}}{R_{in1} + R_{in2}} \right\} \quad (6)$$

Using (2) to obtain the values of the input resistances gives:

$$I_{out} = I_{in} \left\{ \frac{\sqrt{I_{b1}} - \sqrt{I_{b2}}}{\sqrt{I_{b1}} + \sqrt{I_{b2}}} \right\} \quad (7)$$

fig. 3 The current mirror below the loop of transistors in fig. 2 can be replaced by two current mirrors in parallel. The circuit is now fully symmetrical, which results in an improved high-frequency behaviour.

Therefore, we see that the output current is linearly dependent on the input current with a variable gain defined by the two bias currents. For each subcircuit the absolute value of the input current is limited to four times the bias current [2]. This results in the following input current range for the complete circuit from fig. 4(a):

$$|I_{in}| \leq 4 \cdot \min(I_{b1}, I_{b2}) + 4\sqrt{I_{b1} \cdot I_{b2}} \quad (8)$$

III. FOUR-QUADRANT CURRENT MULTIPLICATION

The current gain as given by (7) is a nonlinear function of the bias currents. It will now be shown that a third circuit as shown in fig. 2 or 3 can be used to obtain a gain that is linearly dependent on a single control current.

Eqn. (7) would become linear if the sum of the square root terms in the denominator is kept constant and the difference of the square root terms in the numerator is proportional to a control current. This is exactly what happens in the circuits of figures 2 and 3 for the drain currents of transistors M₁ and M₂. In these circuits, the sum of the gate-source voltages of M₁ and M₂ and thus the sum of the square roots of their drain currents is kept constant. The difference between these gate source voltages is proportional to the input current I_{in} because of the

constant input resistance. Therefore, the drain currents of M₁ and M₂ can be used as the bias currents I_{b1} and I_{b2} . This is illustrated in fig. 4(b). The response of the complete circuit is now given by the following expression:

$$I_{out} = I_{in} \cdot I_{control} \frac{1}{4I_{bias}} \quad (9)$$

This is the transfer of a four-quadrant current multiplier. The input current ranges are as follows:

$$|I_{in}| \leq 8I_{bias} - 2|I_{control}|, \text{ and} \\ |I_{control}| \leq 4I_{bias} \quad (10)$$

IV. SIMULATION AND MEASUREMENT RESULTS

The circuit from fig. 4(a) was realized in a standard 2.5 μm CMOS process using transistors with a channel length of 5 μm and a channel width of 50 μm . Fig. 5 shows a microphotograph of the test chip, which contains two current attenuator circuits. Fig. 6 shows the measured output current of the circuit and the first derivative. The measured nonlinearity is less than 1% over the entire input current range, as given by (8) or (10). Simulations indicate that a -3dB bandwidth of 100 MHz is feasible using transistors with a channel length of 5 μm .

fig. 4 The complete current attenuator circuit (a). The gain is given by:

$$\frac{I_{out}}{I_{in}} = \frac{\sqrt{I_{b1}} - \sqrt{I_{b2}}}{\sqrt{I_{b1}} + \sqrt{I_{b2}}}$$

A simple additional circuit (b) can be used to generate the bias currents I_{b1} and I_{b2} . In that case the gain is proportional to the control current $I_{control}$ and the complete circuit can be used as a four-quadrant current multiplier:

$$I_{out} = I_{in} \cdot I_{control} \frac{1}{4I_{bias}}$$

V. CONCLUSION

A new CMOS current attenuator has been presented, which can easily be extended to perform a four-quadrant current multiplication.

The circuit's performance is insensitive to temperature and process variations. The circuit features a measured nonlinearity of less than 1% over the entire input current range. The circuit is insensitive to the body effect and it is therefore not necessary to place transistors in individual wells connected to their sources. This results in a relatively large bandwidth. Simulations indicate that a -3dB bandwidth of 100 MHz is feasible.

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fig. 5 Die photograph of the current attenuator circuit of fig. 4(a).

fig. 6 Measured output current of the current attenuator circuit of fig. 4(a) and the first derivative (DI) at different values of the bias currents.