Design of Pixel-Level ADCs for Energy-Sensitive Hybrid Pixel Detectors

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Abstract

Single-photon counting hybrid pixel detectors have shown to be a valid alternative to other types of X-ray imaging devices due to their high sensitivity, low noise, linear behavior and wide dynamic range. One important advantage of these devices is the fact that detector and readout electronics are manufactured separately. This allows the use of industrial state-of-the-art CMOS processes to make the readout electronics, combined with a free choice of detector material (high resistivity Silicon, GaAs or other). By measuring not only the number of X-ray photons but also their energies (or wavelengths), the information content of the image increases, given the same X-ray dose. We have studied several possibilities of adding energy sensitivity to the single photon counting capability of hybrid pixel detectors, by means of pixel-level analog-to-digital converters. We show the results of simulating different kinds of analog-to-digital converters in terms of power, area and speed.

I. INTRODUCTION

Semiconductor pixel detectors are now widely used in high-energy physics experiments [1],[2]. Their application as photon counting devices for X-ray and gamma-ray detection has also been demonstrated [3],[4].

A detailed explanation of the principle and functionality of pixel detectors can be found elsewhere [5]. The basic differences with other imaging detectors (such as CCDs, CMOS imagers, film, phosphor plates, etc…) are *direct conversion* and *individual photon detection*. Direct conversion means that the photon deposits an amount of charge in the detector directly proportional to the energy of the photon. This charge is then processed by the readout electronics. Individual photon detection refers to the fact that photons are detected individually one by one in each pixel, and thus no charge integration is taking place, as is the case in almost all other imaging detectors.

In hybrid pixel detectors, the detector and the readout electronics are manufactured independently and they are connected afterwards using flip-chip bonding techniques. This allows for separate optimization of the detector and the readout electronics.

A review of the design and assembly issues of pixel detectors for use in biomedicine and high energy physics can be found in [6].

In X-ray imaging, the detection and measurement of the energy of individual X-ray photons can improve the final image given the same X-ray dose used in integrating or photon counting techniques.

The individual photon detection performed in pixel detectors allows the addition of pixel-level energy sensitivity by adding circuitry that converts, stores and sends off-chip the energy information. The conversion can be performed using analog-to-digital converters (ADCs) in the pixel electronics. The use of ADCs at the pixel level has also been shown to improve the spatial resolution in particle detection applications [7].

We will start by introducing the pixel architecture that will be the basis for our design. Then, we will explain the different ADC structures we have studied. Finally, we will mention the future work we intend to do and the conclusions that can be drawn from the work done so far.

II. PIXEL ARCHITECTURE

We assume that the pixel electronics have a structure such as the one shown in *figure 1*. The signal deposited in the detector by each individual photon is first amplified and integrated (for example, using a charge sensitive amplifier [8]). This is needed in order to convert the deposited charge to a voltage or current that can be converted by the ADC, and also to increase the signal-to-noise ratio. At the same time, a pulse is generated if the signal is above the noise level. We will not study this block in this paper.

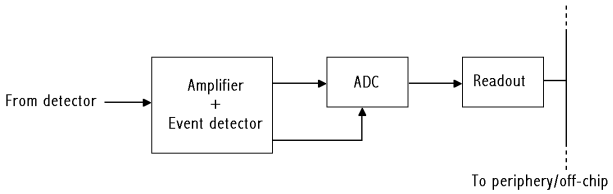

Figure 1: Block diagram of the pixel architecture

The analog signal and the digital pulse coming out of this first block are the inputs to the analog to digital converter. The pulse is used to start the conversion, and the output of the amplifier is the signal that will be converted.

After the ADC, a fast digital readout circuit is needed in order to allow a new photon hit to be processed in the pixel. In most pixel readout chips there is a clear distinction between the image acquisition and the data readout. In our case, however, the digital readout has to be working while an image is being acquired, as we do not intend to provide means for storing more than one hit in the pixel. This means that an event by event readout is needed for this kind of circuit. The circuitry needed to perform this readout will not be explained in this paper.

III. ANALOG TO DIGITAL CONVERTERS

A. Noise considerations

As we have seen in the previous section, a relatively large amount of digital circuit activity will be happening at the same time the amplification and the conversion are taking place. This is not the case in most pixel readout chips, where the different time slots for image acquisition and data readout divide clearly the analog processing and the digital activity between the two processes.

This means that, for the ADC, the effects of electronic device noise will be less important than the noise generated by the digital activity. Noise from power supply coupling, crosstalk, substrate fluctuations and stray carriers are likely to be well above the thermal, shot and flicker noise associated with silicon devices [9].

B. Specifications

Our goal in studying different ADC structures is to find out the trade-offs that each architecture offers. The different applications where an energy sensitive pixel detector readout chip would be used have different requirements in terms of pixel area and photon rate.

As our first goal, we will design 4-bit ADCs, as this corresponds approximately to the best resolution that can be achieved with a room temperature GaAs detector [10].

The area for the pixel (including amplifier, ADC and readout) should not exceed 100• m by 100• m. Assuming a typical active imaging area of 1 cm by 1 cm, we end up with approximately 10000 pixels.

In order to calculate a typical conversion rate, we assume a photon rate of 10^6 photons per second and per square millimetre. This is the typical rate for radiological applications. With this photon rate and a pixel size of 100• m by 100• m we get a photon rate per pixel of 10^4 photons per second. Taking a conservative approach (as we have to add the integration and readout time), we will use a conversion time of approximately 1 • s. This time is also comparable to the counting frequency in photon counting pixel detectors [3].

The power consumption of the ADC should be minimal. Assuming that the power consumed by all the ADCs is approximately 100 mW, and supposing a number of 10000 pixels, we will take a typical power consumption of 10 • W per pixel. In order to be able to compare the performance of the different ADCs we choose a first value of full-scale current equal to 1• A.

All the designs are being done in a 0.25• m CMOS digital process with 6 metal layers. We used a current-mode approach for all the designs reported in this paper.

C. Flash ADC

A flash analog-to-digital converter is probably the fastest, but its cost in area and power consumption can be too prohibitive if we want to have several hundreds of these ADCs in the same chip. However, by working in the current-mode domain, we can reduce significantly the power and area requirements.

In our case, we use a current-mode comparator based on the one described in [11]. We can see the principle of the comparator in Figure 2.

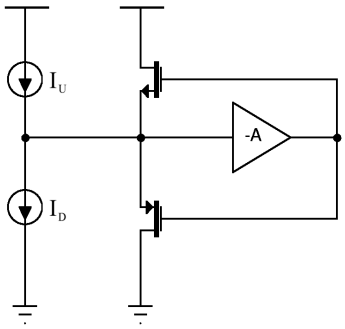

Figure 2: Schematic view of the current-mode comparator

The basic circuit consists of an inverting amplifier and a feedback consisting of an NMOS transistor and a PMOS transistor. The NMOS transistor is connected from V_{DD} to the input of the amplifier with its gate controlled by the amplifier output, and the PMOS transistor is connected between the input of the amplifier and ground with its gate also controlled by the output of the amplifier.

Figure 3 shows the simulated input/output characteristic of the ADC with a 1 μs conversion time.

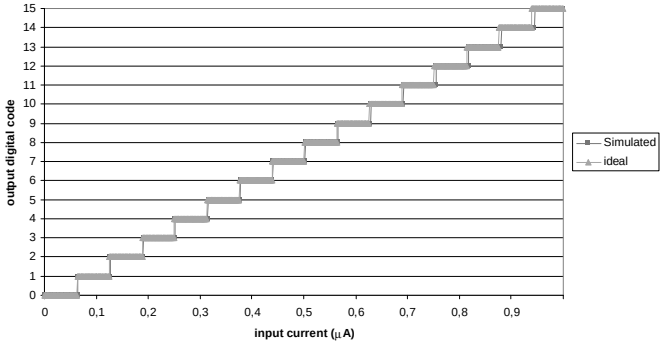

Figure 3: I/O characteristic of the Flash analog-to-digital converter

The following table summarizes some of the specifications of the flash ADC.

Table 1
Characteristics of the flash ADC

Characteristic	Value	Units
Full scale	1	μA
Resolution	4	bits
Power supply	1.8	V
Static power consumption	18	μW
Area	70 x 70	μm^2

D. *Successive Approximation ADC*

The converter explained in the previous section is fast, but the power consumption is relatively high. We can think of trading some speed for power and use a successive approximation type of converter. Figure 4 shows a block diagram of such a converter.

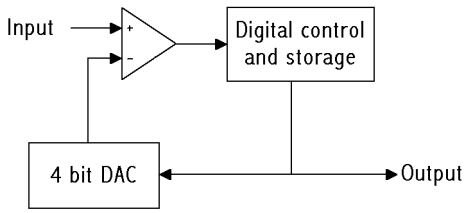

Figure 4: Block diagram of the successive approximaation ADC

This converter needs a number of clock cycles equal to the number of bits in order to perform the conversion. We use a current-mode binary-weighted DAC, and the comparator is the same type as the one used in the flash converter. The complexity of the circuit lies mostly in the digital circuitry, as it is responsible for switching ON and OFF the current sources in the DAC in response to changes in the comparator output.

Figure 5 shows the layout of this converter.

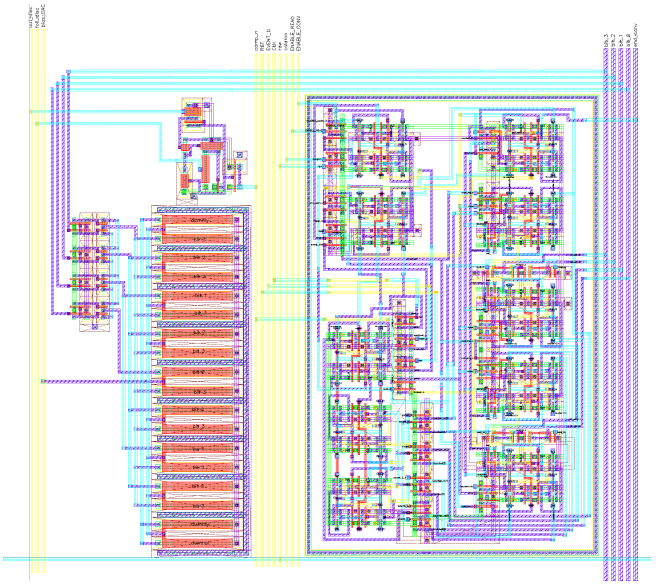

Figure 5: Layout of the successive approximation analog-to-digital converter

In the left side the DAC and the comparator can be seen, while the digital circuitry is located on the right. It can be clearly seen that the digital circuitry takes more than half the total area of the converter. In this first prototype, the logic was designed using conventional CMOS logic.

Figure 6 shows the input/output characteristic of such a converter working at a 1 µs conversion time.

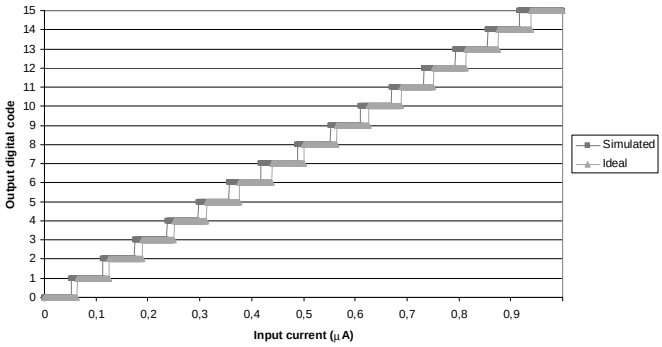

Figure 6: I/O characteristic of the successive approximation analog-to-digital converter

The speed of the comparator used is proportional to the difference of currents applied to its input. This means that by increasing the full scale current (and hence the I_{LSB} value) we could achieve higher conversion speeds at the price of a higher power consumption. This would translate to a lower offset in the I/O characteristic.

The following table summarizes the characteristics of this converter.

Table 2
Characteristics of the successive approximation ADC

Characteristic	Value	Units
Full scale	1	µA
Resolution	4	bits
Power supply	1.8	V
Static power consumption	3.8	µW
Area	90 x 70	μm^2

E. *Algorithmic-pipelined*

The problem with the previous two types of converters is the need for a relatively complex digital circuitry in the pixel. This can lead to crosstalk as well as substrate coupling noise problems. We can also think of moving some (of all) the processing done in the digital domain to the analog domain.

A converter that does such a thing is the current-mode algorithmic ADC, as described in [12]. The basic building block of this converter can be seen in Figure 7.

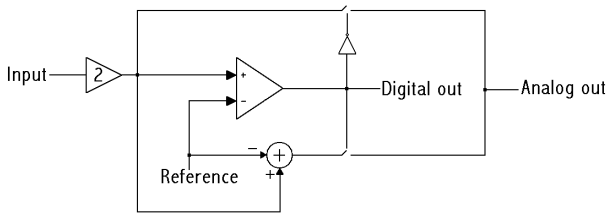

Figure 7: Block diagram of the basic building block for the algorithmic analog-to-digital converter

In Figure 7, the input signal is multiplied by 2 and compared with a reference value equal to the full-scale current of the converter. If the reference is higher, the analog output is

set equal to the input multiplied by two, and the digital output is set low. If the reference is lower, the analog output is set equal to the input multiplied by two minus the reference, and the digital output is set high.

By connecting N such blocks one after the other, we can obtain an N-bit ADC, as Figure 8 shows for a 4-bit case.

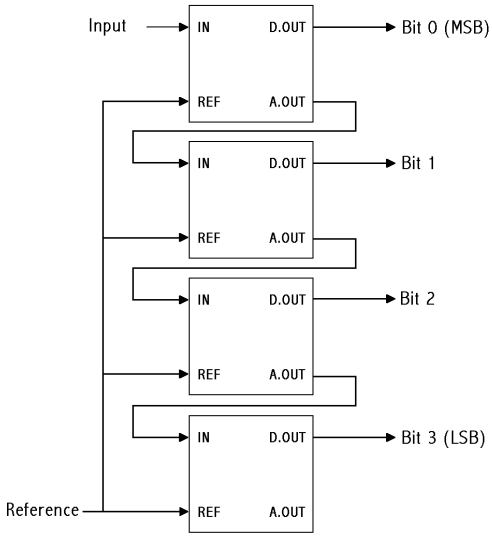

Figure 8: Block diagram of an algorithmic-pipelined analog-to-digital converter

The simulated input/output characteristic of the ADC with a conversion time of 1 μscan be seen in Figure 9.

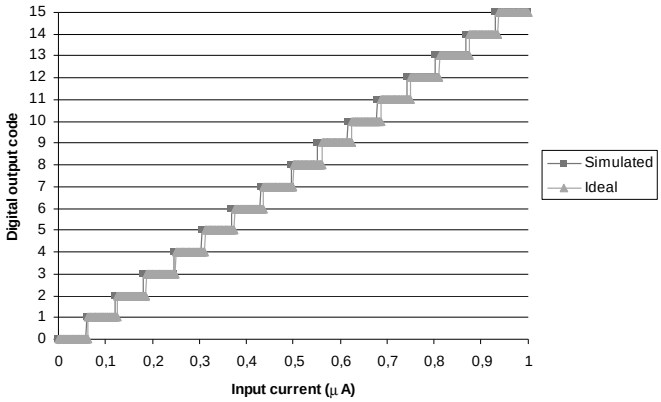

Figure 9: I/O characteristic of an algorithmic-pipelined ADC

The characteristics of the ADC can be seen in the following table.

Table 3
Characteristics of the algorithmic ADC

Characteristic	Value	Units
Full scale	1	μA
Resolution	4	bits
Power supply	1.8	V
Static power consumption	9.8	μW
Area	80x80	μm^2

IV. Future Work

At the end of this year, it is expected to submit a test chip with arrays of these ADC structures in order to test their functionality. Once the circuits have been measured and characterized, a study of how to perform a fast readout of the digital values has to be performed in order to be able to build a first working prototype.

Additionally, ways to improve the conversion speed while keeping the same power consumption and occupied area must be studied deeper.

V. Conclusions

We have shown that it is possible to add analog to digital converters at pixel level in pixel detector readout chips. In terms of power and occupied area, all three architectures studied so far fall inside the requirements. The biggest differences between them are in the digital circuitry needed to perform the conversion and in the speed/linearity relationship. It is clear that a faster current comparator would allow for faster ADCs, but the power requirements for the system must be taken into account.

VI. Acknowledgments

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VII. References

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