Quasi Monolithic Silicon Load Cell for Loads up to 1000 kg with Insensitivity to Non-homogeneous Load Distributions

Remco Wiegerink, Robert Zwijze, Gijs Krijnen, Theo Lammerink, Miko Elwenspoek

MESA Research Institute, University of Twente
P.O. Box 217, 7500 AE Enschede, The Netherlands
phone: x-31-53-4894373, fax: x-31-53-4893343,
e-mail: R.J.Wiegerink@el.utwente.nl

Abstract - In this paper, a micromachined silicon load cell (force sensor) is presented for measuring loads up to 1000 kg. The sensitive surface of 1 cm² contains an array of sensing elements to make the load cell insensitive to non-homogeneous load distributions resulting in higher accuracy. The load cell has been realized and tested. Measurement results show an accuracy of 0.2 % of full scale limited by the measurement electronics. An accuracy of 0.03 % or better is expected to be feasible.

I. Introduction

Load cells are force sensors which are used in weighing equipment. Most conventional load cells for loads of 1000 kg and more are made from steel. The steel part of these load cells deforms under a load, which is measured with resistive strain gauges. The accuracy of these load cells is limited by hysteresis and creep. To minimize these effects, expensive high-grade steels and labor intensive fabrication methods are required.

Silicon does not suffer from hysteresis or creep and, therefore, it is an ideal material for use in load cells.

Batch fabrication potentially offers low production costs. In this paper, a silicon load cell is presented for loads up to 1000 kg. Different from a previous design [1], an array of sensing elements is used to make the load cell less sensitive to non-homogeneous load distributions resulting in higher accuracy. The design can easily be adapted for higher loads by increasing the chip area or using multiple chips in a single package.

II. Operation principle

Figure 1 shows a schematic drawing of the load cell. The design consists of two bonded silicon wafers. Figure 2 shows a crosssection of the load cell and a bottom view of the top wafer. The top-wafer contains poles which bear the load. The bottom-wafer contains an electrode pattern forming an array of capacitors with the top wafer as a common electrode. On application of a load the poles will be compressed and the distance between the metal electrodes and the top-wafer at the position of the capacitors will decrease thereby increasing the capacitance.

Figure 1 Schematic drawing of the load cell chip.

The change in height of each pole as a result of the applied load can be expressed as (assuming that the force distribution is homogeneous over the surface of a single pole):

$$\Delta l_{i,j} = \frac{l_{pole}}{E \cdot A_{pole}} F_{i,j} \quad (1)$$

where l_{pole} and A_{pole} are the height and surface area of the poles, respectively, E is the Young's modulus of silicon and $F_{i,j}$ is the force acting on the pole. The indices i and j indicate the position of the pole in the array.

For each capacitor, the capacitance is given by:

$$C_{i,j} = \frac{\epsilon A_{cap}}{d_0 + \Delta d_{i,j}} \quad (2)$$

where ϵ is the dielectric constant, A_{cap} is the surface area of each capacitor, d_0 is the distance between the capacitor plates with no load applied and $\Delta d_{i,j}$ is the change in distance as a result of the load.

Approximating the change in distance $\Delta d_{i,j}$ by the average change in height of the surrounding poles, (2) can be written as:

$$C_{i,j} = \frac{\epsilon A_{cap}}{d_0 - \frac{1}{4}(\Delta l_{i,j} + \Delta l_{i+1,j} + \Delta l_{i,j+1} + \Delta l_{i+1,j+1})} \quad (3)$$

or:

$$\frac{1}{C_{i,j}} = \frac{d_0 - \frac{1}{4}(\Delta l_{i,j} + \Delta l_{i+1,j} + \Delta l_{i,j+1} + \Delta l_{i+1,j+1})}{\epsilon A_{cap}} \quad (4)$$

which is, according to (1), proportional to the forces acting on the poles.

Summation of (4) for all capacitors gives:

$$\sum_{i=1}^{n-1} \sum_{j=1}^{n-1} \frac{1}{C_{i,j}} = (n-1)^2 \frac{d_0}{\epsilon A_{cap}} - \sum_{i=1}^{n-1} \sum_{j=1}^{n-1} \frac{\frac{1}{4}(\Delta l_{i,j} + \Delta l_{i+1,j} + \Delta l_{i,j+1} + \Delta l_{i+1,j+1})}{\epsilon A_{cap}} \quad (5)$$

Substituting (1) into (5) gives:

$$\sum_{i=1}^{n-1} \sum_{j=1}^{n-1} \frac{1}{C_{i,j}} \approx (n-1)^2 \frac{d_0}{\epsilon A_{cap}} - \frac{l_{pole}}{E \epsilon A_{cap} A_{pole}} F_{tot} \quad (6)$$

where F_{tot} is given by:

$$F_{tot} = \frac{1}{4} \sum_{i=1}^{n-1} \sum_{j=1}^{n-1} (\Delta F_{i,j} + \Delta F_{i+1,j} + \Delta F_{i,j+1} + \Delta F_{i+1,j+1}) \quad (7)$$

When the total force acting on the chip is homogeneously distributed over the poles (all $F_{i,j}$'s are equal) F_{tot} is exactly equal to the total force. In case the force distribution is not homogeneous, examination of (7) shows that for a large number of poles F_{tot} is still a very good approximation of the total force acting on the chip.

Figure 2 Structure of the load cell chip.

Note that in order to perform the summation given by (6) it is necessary to measure each capacitance individually. It would be much easier to connect all capacitors in parallel and, thus, measure the total capacitance. For a homogeneously distributed load this makes no difference and the reciprocal of the total capacitance will also be proportional to the total force acting on the chip. However, for non-homogeneous force distributions an error will be introduced when the total capacitance is measured instead of the sum of the reciprocal values of the capacitors.

III. Realized prototype

A first prototype has been designed and fabricated using a relatively small number of $5 \times 5 = 25$ poles and 16 capacitors. Each pole has a diameter of 2 mm, resulting in a total area bearing the load of 0.8 cm^2 . The height of the poles was approximately $200 \text{ }\mu\text{m}$, resulting in a change in height of $0.2 \text{ }\mu\text{m}$ at a load of 1000 kg. The distance between the capacitor plates was chosen $1 \text{ }\mu\text{m}$, in order to obtain a 20 % change at the maximum load. The area of the capacitor plates was 0.5 mm^2 , resulting in capacitance values in the order of a few pF.

Figure 3 shows the process sequence used for fabricating the load cell chip. Both wafers have to be highly conductive, the bottom wafer to form a stable ground contact and the top wafer because it forms the common top electrode for the capacitors. Therefore, we used highly boron doped wafers ($0.01\text{--}0.018 \text{ }\Omega\text{cm}$). In the bottom wafer, first the gaps are etched which define the capacitor distance d_0 using Reactive Ion Etching (RIE) with a resist mask. Next, wet thermal oxidation is used to obtain a $1.5 \text{ }\mu\text{m}$ thick SiO_2 layer for electrical isolation from the substrate. The SiO_2 layer is stripped from the backside which will be used to make the ground contact. Finally, aluminum is deposited and structured on both sides of the wafer. The process for the top wafer starts with RIE etching (with a resist mask) the shallow gaps in the backside, which ensure that the load is applied at the position of the poles and not at the capacitors. Next, wet thermal oxidation is used to obtain an 800 nm thick SiO_2 layer, which will later be the mask when etching the $200 \text{ }\mu\text{m}$ deep grooves which separate the poles from the capacitors. After structuring the SiO_2 layer a polymer layer is applied on the backside to allow etching through the entire wafer in the subsequent RIE steps [1]. A cryogenic RIE process is used to etch the first part of the contact holes using resist as the mask material and finish etching the contact holes and etching the grooves using the previously structured SiO_2 layer as the mask. Finally, the wafers are connected by low temperature silicon direct bonding using a bonding temperature of $450 \text{ }^\circ\text{C}$. Prior to bonding, the bottom wafer is treated with an O_2 plasma and the top wafer with a piranha cleaning. Figure 4 shows a photograph of the finished load cell chip. Besides the 16 sensor capacitors the chip contains 4 reference capacitors located at the corners.

Figure 3 Process sequence for the fabrication of the load cell chip.

Figure 4 Photograph of the fabricated load cell chip. The area in the center bears the load and has dimensions of $1 \text{ cm} \times 1 \text{ cm}$. The entire chip measures $1.5 \text{ cm} \times 1.5 \text{ cm}$.

IV. Package

Figure 5 shows a cross section of the package which was designed and realized for the load cell chip. The purpose of the package is to apply the load to the load cell chip as homogeneous as possible. Ceramic blocks (1 cm x 1 cm and 2 cm high) are used above and below the chip. The surfaces which are in contact with the silicon are polished to obtain a surface roughness comparable to the roughness of the unpolished backside of the silicon wafers. The ceramic blocks are kept in position by thin steel membranes. Steel balls are used to apply a (reproducible) point force to the ceramic blocks.

Figure 5 Schematic drawing of the package.

Figure 6 Photograph of the load cell chip and electronics mounted in the package.

V. Electronics

A so-called modified Martin oscillator [2,3,4] is used to measure the capacitance changes with respect to the on-chip reference capacitors, hence eliminating temperature and humidity variations. A simplified schematic of the circuit is shown in Figure 7. The core of the circuit is an oscillator built around the two operational amplifiers and the two digital NAND gates. The oscillation period of this oscillator is proportional to $R \cdot C_{off}$. With the help of a digital multiplexer the capacitors in the load cell chip can be connected in parallel to C_{off} resulting in a change in the oscillation period proportional to the additional capacitance.

Figure 7 Oscillator circuit used for measuring the 16 capacitor ratio's C_{ref} / C_{s_i} .

Essential is that the voltage at the node common to all capacitors is kept constant, thus largely eliminating the influence of parasitic capacitance from this node to ground (e.g. the capacitance between the top and bottom wafer of the load cell chip). Furthermore, the other side of the capacitors is driven by a digital output voltage, again eliminating the influence of parasitic capacitance (e.g. the capacitance between the metal electrodes and the grounded bottom wafer substrate).

For one complete measurement cycle, 18 period measurements have to be performed:

$$\begin{aligned} T_{s_i} &\propto R \cdot (C_{off} + C_{s_i}) \quad i = 1..16 \\ T_{ref} &\propto R \cdot (C_{off} + C_{ref}) \\ T_{off} &\propto R \cdot C_{off} \end{aligned} \quad (8)$$

It can be shown that the capacitance ratio's are now given by:

$$\frac{C_{ref}}{C_{s_i}} = \frac{T_{ref} - T_{off}}{T_{s_i} - T_{off}}, \quad (9)$$

independent of all additive and multiplicative errors introduced by the oscillator circuit.

In the current measurement setup, the capacitor address lines are controlled by an AT89S53 microcontroller, which in turn is controlled by a personal computer. The oscillator output frequency is counted by the microcontroller.

VI. Measurement results

The packaged load cell has been tested with loads up to 1000 kg. The 16 capacitance ratio's C_{ref}/C_{s_i} were measured individually and subsequently averaged to obtain a measure for the total applied load. Figure 8(a) shows a plot of the change in the average capacitance ratio as a function of the applied load. Each load has been applied two times: first the load cell is not loaded, then loaded, then unloaded and finally loaded again. Figure 8(b) shows the difference between each pair of measurements, both with and without incorporating the shift in zero-load output between the measurements. It is seen that the error is rather random but always within 0.2 % of full scale. Measurements over longer time periods with a constant load (see Figure 9) show that the error is dominated by random noise, probably

originating from the measurement electronics. At the moment, an important source of errors is the slow communication between the personal computer and the microcontroller, which causes each complete measurement cycle to take 15 seconds while 10 measurements per second should be feasible.

Figure 8 Measured average capacitance ratio as a function of the applied weight (a) and difference between successive measurements (b).

VII. Conclusion

We have presented an accurate and low-cost distributed capacitive load cell, which is a promising alternative to traditional load cells made from steel. A first prototype shows an accuracy of 0.2 % of full scale limited by the measurement electronics. Future research focuses on optimization of the measurement setup combined with an increase of the number of poles and capacitors in order to obtain an accuracy better than 0.03 %.

Figure 9 Variation of the measured capacitance ratio as a percentage of full scale over a period of 5 hours with:

- (a) no load applied, and
(b) a load of 400 kg.

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