TOWARDS IN-SITU TEM ANALYSIS OF PLD $Pb(Zr,Ti)O_3$ THIN FILM MEMBRANES

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***Abstract* — In this paper, a novel technique for fabricating Transmission Electron Microscopy (TEM) chips for investigating structural and piezoelectric properties of Pulse Laser Deposited (PLD) Lead Zirconium Titanate (PZT) thin films is presented. The method involves silicon-on-insulator (SOI) wafer technology together with deep reactive ion etching (DRIE) and highly selective etchants.**

This study is unique in the sense that it will facilitate in-situ characterization of the PLD PZT membranes during actuation. As well as PLD PZT, the proposed method can be applied to a variety of materials by proper selection of the etchants and tuning of the process parameters.

Being a critical step of the process sequence, the deposition profile of the PZT layer on the Lanthanum Nickel Oxide (LNO) seed layer is characterized prior to fabrication. The results reveal that the PLD process is not conformal and the thickness of the LNO/PZT layer is different on surfaces with different topographies.

***Keywords:* Lead Zirconium Titanate (PZT), Pulsed Laser Deposition (PLD), Transmission Electron Microscopy (TEM) Membrane, In-situ Analysis**

I - Introduction

Piezoelectric materials are used in a wide variety of applications in the field of microelectromechanical systems (MEMS) including sensors [1] and actuators for various purposes [2].

Lead zirconium titanate (PZT) is the most commonly used piezoelectric material due to its excellent ferroelectric and piezoelectric properties [3]. A number of different methods are used for PZT deposition [4-7]. Among these, pulsed laser deposition (PLD) is a promising technique since it enables deposition of PZT thin films with superior piezoelectric and ferroelectric properties [8, 9].

Characterization of the crystal structure becomes rather important at nano-scale since it has a great influence on the material properties. Although there are efforts for more advanced in-situ TEM experiments [10-12], the TEM studies carried out on PZT thin film membranes are mostly cross-sectional, for which preparation of the samples is rather demanding [13, 14].

In this paper, the method for fabricating TEM chips with a PLD PZT thin film membrane will be presented. The chips fabricated using this method will enable investigation of the PZT membranes from the top, through their thickness. Top view TEM has many more advantages than cross-sectional TEM, such as the possibility of determining the crystal size, revealing the diffraction patterns perpendicular to the plane and observing grain boundaries, crystal defects and such. Moreover, there is no need for modifying or damaging the structure to be investigated. Most importantly, the chips fabricated during this study will enable in-situ investigation of the membranes during actuation.

II – Design

A. Chip Design

The designed chips should be able to fit into a standard TEM holder, where the length of the diagonal should be smaller than ~3.05 mm. The chip geometry is selected to be a square with a side length of 2.1 mm, accordingly.

There exist 20 μm-wide rectangular grooves through the device layer, which define the chip boundaries. Matching grooves are also present at the backside until the half thickness of the carrier wafer, in order to ease the cleavage of individual chips.

Square membranes are located at the center of each TEM chip. Side lengths of these membranes vary in the range from 5 μm to 50 μm in order to investigate the effect of the size on different properties of the membranes, such as the internal stress.

Top and bottom electrodes as well as their contact pads are included in some designs in order to enable actuation of the membranes, even during TEM investigation, using a specially designed holder with electrical connections.

At the center of each individual chip, there is a 100 μm-diameter circular hole through the bottom of the wafer until the LNO bottom electrode.

B. Process Design

As well as the chip itself, the techniques to be used and the process parameters should be carefully designed in order to accomplish the fabrication of the TEM chips successfully.

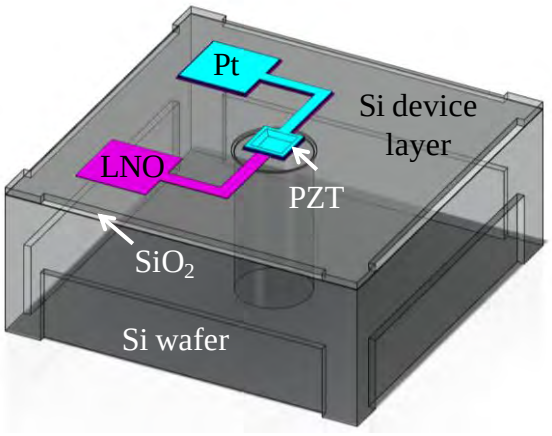

Figure 1*: Schematic illustration of the TEM chip.*

Initially, the carrier wafer should be selected considering the most critical process steps. Rather than a standard silicon wafer, an SOI wafer is used in this process. The main reason behind this is to take advantage of the buried oxide layer as an etch-stop during the through DRIE etching of the holes from the backside. Hence, the effect of any non-uniformity during this step is eliminated.

Moreover, by stopping at the buried oxide layer rather than the membrane itself, both this layer and the device layer will provide strength to the membrane. Hence, fracture of the thin film membranes due to the pressure difference during etching in a DRIE system with helium backside-cooling will be prevented.

One final advantage of the SOI wafer is that, any variation in the size of the membranes can be eliminated by defining their location by etching rectangular grooves into the silicon device layer from the top, prior to the deposition of the thin film membrane. However, the device layer should not be etched through to maintain the strength during the backside etch. Furthermore, the deposition profile of the PZT layer inside the grooves should be carefully investigated in order to account for any discontinuity of the thin film at the corners or possible short-circuits.

Selection of the top and the bottom electrodes are also rather important. A metal (e.g. platinum) top electrode can easily be realized through a straightforward lift-off process after deposition and patterning of the PZT layer. However, realization of the bottom electrode is more critical, having an influence over the properties of the grown PZT layer. Furthermore, it should be possible to pattern the PZT layer selectively from the bottom electrode. Considering the above issues, LNO is selected as the bottom electrode since it is electrically conducting, it serves an excellent seed layer for PZT deposition and it can be etched selectively from the PZT layer using an HCl-based solution [15].

As briefly mentioned above, the through etching of the holes from the backside is carried out using a DRIE system, which exerts a limitation on the size of the through-holes. For a more uniform etch profile, the diameter of the holes is selected to be equal to each other and 100 µm as stated in the previous section. Furthermore, the front side of the wafer should be properly protected during etching.

III- Fabrication

For the fabrication of the TEM chips, 4-inch SOI wafers with <100> orientation are used (Figure 2(a)). The thicknesses of the device and the silicon dioxide layers are 10 µm and 0.5 µm, respectively.

As a first step, 20 µm wide grooves defining the chip boundaries are etched by DRIE through the thickness of the device layer until the buried oxide layer is reached (Figure 2(b)). Following this step, the wafers are coated with a 100 nm-thick low-stress LPCVD silicon nitride layer, which is then patterned on the front side to serve as a mask for anisotropic wet etching of the device layer in a in a KOH solution at 75°C (Figure 2(c)).

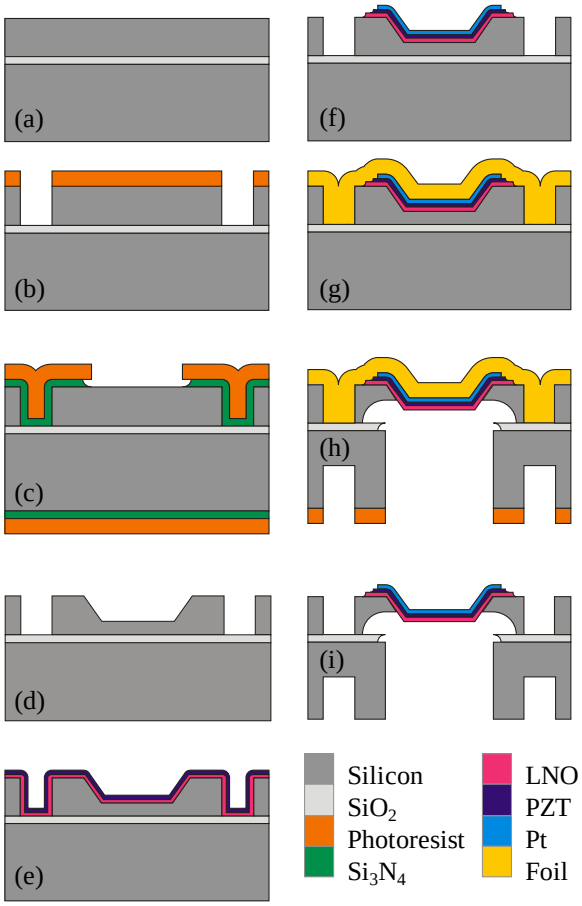

Figure 2*: Fabrication sequence for the TEM chips with PLD PZT membranes.*

The purpose of the anisotropic wet etch step is to define the position and size of the membrane windows (Figure 2(d)). Then, the nitride mask is removed in a phosphoric acid solution at 180 °C and a 20 nm/100 nm-thick LNO/PZT layer is deposited by PLD at 600 °C on the front side of the wafer [16] (Figure 2(e)).

After patterning the LNO bottom electrode) and the PZT layer using HCl- and BHF/HNO_3-based solutions, a 20 nm platinum top electrode is deposited and patterned by a lift-off process (Figure 2(f)).

As the processing of the front side is accomplished, it is coated with a protective foil (DuPont MX 5020) in order to prevent any damage on the PZT layer and the electrodes (Figure 2(g)). 100 µm diameter holes were etched through by DRIE of the carrier wafer [17], BHF (1:7) etching of the silicon oxide layer and isotropic plasma etching of the remaining device layer, respectively (Figure 2(h)). During the DRIE of the carrier wafer, the 20 µm-wide grooves, similar to those defining the chip boundaries are also etched in order to facilitate cleaving of the chips. As the holes are completely etched through the thickness of the carrier wafer, these grooves will be etched only until the half thickness due to the aspect ratio dependent etching (ARDE) effect [18]. Finally, the protective foil is removed (Figure 2(i)) and the chips are cleaved individually from the carrier wafer, glued and wire bonded to a specially designed TEM holder and investigated inside a TEM.

IV –Experimental Work

A. Introduction

In order to investigate the step coverage of the PLD PZT thin films on inclined surfaces and corners, 20 nm/100 nm LNO/PZT layers were deposited on (100) silicon wafers with KOH etched rectangular grooves and v-grooves (Figure 3). Note that, the silicon dioxide layer used as a mask during the etching of the rectangular grooves was not removed in order to investigate the quality of the PZT layer grown on this layer and understand the degree of step coverage during the PLD process.

B. X-ray Diffraction (XRD) Analysis

Results of the XRD analysis performed on the deposited layers reveal that the deposited film is a good quality PZT film, which is a mixture of (100) and (110) directions (Figure 4).

C. The Deposition Profile

High resolution scanning electron microscope (HR-SEM) images showing the cross-section of the samples reveal that the deposition not conformal and the PZT layer grow in a columnar fashion (Figure 4(a-d)). Thickness values for the layers deposited on different surfaces of the grooves are summarized in Table 1.

Comparison of the Surfaces: For both samples, thickness of the PZT layer on the side walls is roughly equal to the thickness of the top layer multiplied by the cosine of the angle between the two planes –(100) and (111)- as follows:

$$t_{Side} = t_{Top} \cdot \cos 54.7° \qquad (1)$$

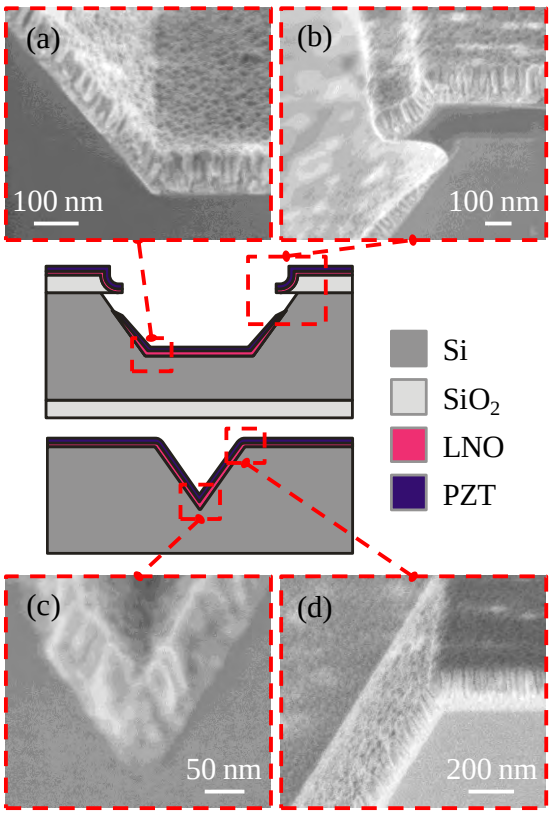

Figure 3: *Cross-section of the samples with (top) rectangular and (bottom) v-shaped grooves. Insets show HR-SEM images of the LNO/PZT layers on different surfaces of the grooves.*

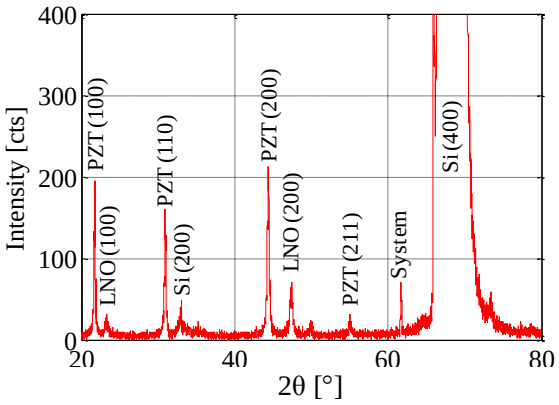

Figure 4*: XRD spectrum of the LNO/PZT thin film deposited on the (100) silicon surface.*

Table *1*: *Thickness of LNO & PZT layers on different surfaces of the grooves.*

	Rectangular grooves		V-grooves	
	LNO	PZT	LNO	PZT
t_{Top} [nm]	30.9	99.3	70.3	108.9
t_{Side} [nm]	20.7	57.1	42.2	63.2
t_{Bottom} [nm]	26.4	79.2	-	-
t_{Tip} [nm]	-	-	40.3	81.5

The relation given in (1) indicates that the film density on the sidewall is identical to that on the top.

Although expected to be the same, the thickness of the PZT layer on the bottom surface of the rectangular grooves is 20% less than those at the top surface. The reason for this may be that, the amount of material entering the groove and reaching the bottom surface is less since part of the target flux is blocked by the sidewalls. This should be further investigated by checking if there is a thickness gradient along the sidewalls.

Comparison of the Corners: The PZT layer is continuous at the bottom corners of the rectangular grooves, as well as the tip of the v-grooves (Figure 3 (a&c)). The ratio t_{Top}/t_{Tip} for a v-groove is similar to the ratio t_{Top}/t_{Bottom} for a rectangular groove.

The PZT layer is also continuous at the top corners of the v-grooves (Figure 3(d)). However, there is a discontinuity between the layers on the top and the sidewalls of the sample with the rectangular grooves as a result of the shadowing due the overhanging silicon dioxide layer (Figure 3(b)). Rather than having a sharp ending exactly under the silicon dioxide edge, the thickness of the PZT layer slowly decreases and finally approaches to zero towards the middle of the overhanging part.

D. The Growth Direction

Comparison of the Surfaces: PZT columns grow along the normal direction of the top and bottom surfaces, which have (100) orientation (Figure 5). However, the directions of the PZT columns on the sidewalls having (111) orientation vary from the <111> direction by an angle, α. This angle varies between 20-35° for individual columns.

Comparison of the Corners: PZT columns grow randomly along a direction between the normal direction of the intersecting surfaces, both at the top and the bottom corners.

V - Conclusion

A novel method for fabricating TEM chips for investigation of PLD PZT thin film membranes is presented. The proposed method enables in-situ characterization of thin film membranes of different materials inside a TEM.

TEM chips are designed considering the space requirements of a TEM and enabling characterization of different properties of the thin films. Furthermore the fabrication sequence is designed carefully in order to eliminate any size variation, non-uniformity or damaging of the membranes.

Having a critical importance for the final experiments, the deposition profile of the PZT layer on the LNO seed layer was investigated prior to fabrication. The results seem promising since the deposited layer is continuous both at the sidewalls and the corners and the thickness is well-controlled. However, the deposition is not conformal, the thickness of the layers on different topographies is varying and discontinuities occur at the shadowed regions.

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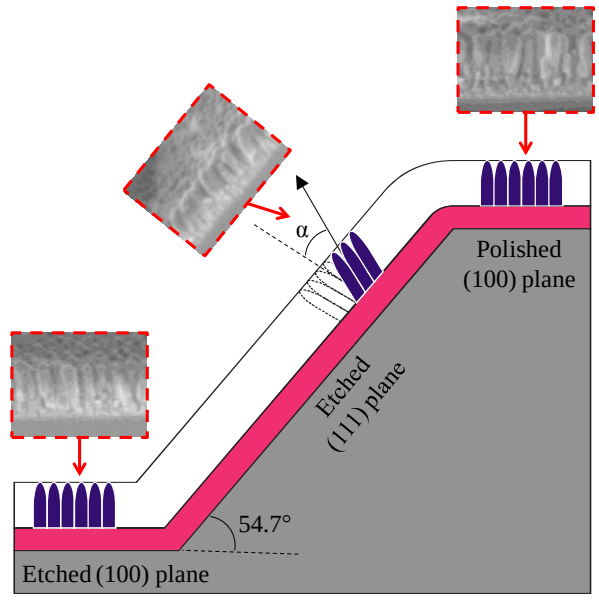

Figure 5*: Growth direction of the PZT columns on different surfaces of the grooves.*

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