The Influence of No Fault Found in Analogue CMOS Circuits

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Abstract: **The most difficult fault category in electronic systems is the "No Fault Found" (NFF). It is considered to be the most costly fault category in, for instance, avionics. The relatively few papers in this area rarely deal with analogue integrated systems. In this paper a simple simulation model has been developed for a particular type of NFF, the intermittent resistive fault resulting from bad interconnections. Simulations have been carried out with respect to a CMOS operational amplifier under influence of NFFs, and the resulting behaviour under different fault conditions has been examined.**

Keywords: No Fault Found; NFF; intermittent resistive faults; TSV; cold soldering; analogue CMOS circuits

I. INTRODUCTION

The downside of the revolution in dimensions and complexity of electronic systems ranging from single Deep Sub-Micron (DSM) transistors in Systems-on-Chip (SoC) up to spacious Printed-Circuit Board (PCB)-based cabinets is a decrease in overall dependability. Most previous studies on failures reducing the dependability are concerned with modelling, test-generation and Design-for-Test (DfT) of permanent and transient faults in mostly digital integrated systems [1].

In electronic systems, interconnect is usually heavily dominating the infrastructure, and hence their potential of showing the above failures.

One category of faults which is most difficult to detect is the No-Fault-Found (NFF), sometimes also referred to as No-Trouble-Found (NTF) and many derivatives [2]. A specific category of NFFs is intermittent (open, short and resistive) faults, characterized by random low-level occurrences in time, randomly fixed in locations, but repairable (at least in PCBs and cabinets) if found. Especially in the space and avionic application fields, this category of faults ranks among the highest in terms of occurrence (>50%) as well as cost [3].

The suspects for this type of intermittent faults are unstable or marginal hardware but usually interconnections in general. Examples are line traces, solder joints, and connectors in PCBs [4, 5] as well as backbone wiring in cabinets.

In advanced integrated circuits there are many (kilometres) interconnection wires subjective to electro migration (EM) as well as billions of vias. Scaling of ICs will increase the number of intermittent faults [6]. In the slowly emerging (3D) chips many very deep and stress-sensitive Through-Via Contacts (TSVs) are used [7]. As during layout design in integrated circuits EM effects can be avoided, only TSVs issues will be looked at.

In both cases of PCBs as well as 3D-TSV integrated circuits, intermittent faults from interconnect could occur. These interconnections can be used to connect digital as well as analogue/mixed-signal chips in the case of PCBs or as IPs in a (3D-TSV) SoC. As almost all research results deal with digital circuits, e.g. [8], this paper will focus on analogue circuits only. The above boundary conditions, however, will limit their influence to inputs, outputs and power-supply lines of analogue (CMOS) circuits.

The paper is organised in the following way. First, in section II it is shown how and where intermittent faults can manifest themselves in practice and general characteristics are provided. In section III, a simulation model is introduced which is highly programmable to emulate and tailor realistic intermittent resistive faults in interconnect. An example *intermittent resistive* injection block is presented. Next, this simulation model is used in the Cadence design environment of our example circuit, a TSMC 65nm OpAmp, in order to investigate the influence of the intermittent parameters on its functional behaviour in section IV. The simulation results give rise to clues on how to detect these intermittent faults. In section V, conclusions are provided.

II. EXAMPLES OF NFFS IN PRACTICE

Besides the well-known permanent and transient faults, the percentage of NFFs is growing rapidly, from around 3% in 1980 up to 70% of all product returns in the year 2008 [9]. Especially in avionics they are already for many

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years a significant part of electric/electronic maintenance costs. A part of NFFs, are intermittent faults as result of bad interconnections and also marginal hardware. This paper will focus on marginal interconnections. The faults appear as bursts [6] (e.g. 2-10 events per burst) in resistivity (e.g. 2Ω - 2kΩ), lasting for relatively short time (e.g. 50ns – 200ns) [3] and appear every now and then (hours up to many days) [10]. Especially the last part is the cause of test problems, as testing is usually performed during a relatively short time frame [3].

In many papers, a distinction is made between different categories of intermittent faults, depending on their application area. One distinguishes between intermittent *stuck-at, open, short*, *timing* and intermittent *resistive* faults [6]. In our case of analogue circuits, only the intermittent resistive faults are considered, ranging from a few Ohms (Ω) to some kΩ resistance. An example of a real measurement result of a system during an intermittent resistive fault is shown in Fig. 1 [10]. In this case the resistive fault ranges between 0 and a few hundred Ohms, and reveals bursts; the time axis can span hours.

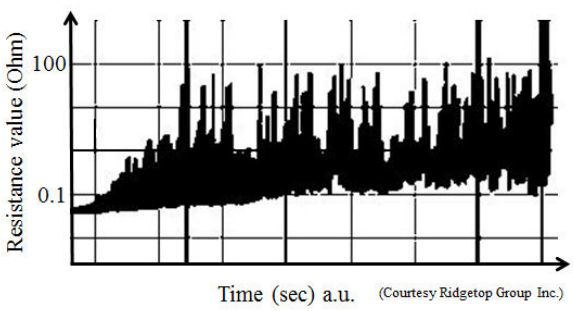
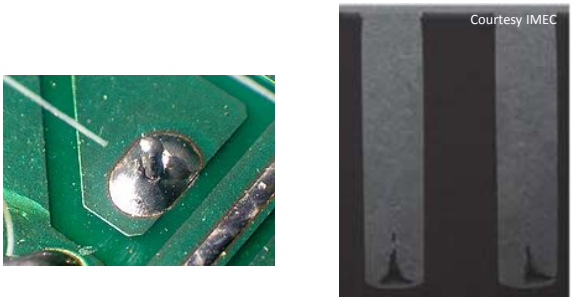


Fig.1: Measurement of a real example of an intermitted resistive fault as result of bad interconnects [10].

Usually, intermittent resistive faults are preceding permanent faults (open) in time (aging) [10, 11]. This has sparked suggestions to detect intermittent faults via extensive (leakage) current tests [6, 12] or by using health monitors [13]. It is important to note that intermittent faults are quite dependent on environmental conditions, like temperature or vibration [3, 14].



a) b)

Fig. 2: Several possible causes of intermittent faults. a) cold (cracked) soldering joint on a PCB, b) voids and cracks in TSVs [7].

There are several physical root causes of intermittent (resistive) faults. At PCB and cabinet level, cold solder contacts (see Fig. 2a), damaged traces/wires, and loose connectors are the major reasons [3]. In integrated circuits, the continued scaling of interconnection is likely to increase intermittent faults [15]. Origins can be electro migration (EM), soft breakdown (SBD) [6], material residuals and induced voids (see Fig. 2b) and cracks in 3D TSVs in chips [16].

It has been shown that intermittent faults can be activated and deactivated by temperature, voltage as well as frequency changes [15].

III. EMULATION OF A FAULT INJECTION SOURCE

In this paper the well-known concept of using a fault injection model in the net list will be used [17, 18]. There is however a number of differences with models applied in this digital domain. In our analog / mixed-signal case an *intermittent resistive* injection tool has been developed, being different from the intermittent stuck-at, open and short as suggested in [6, 17]. Based on the previous section on how intermittent faults manifest [3, 6, 10, 11], a model has been developed for *resistive* intermittent faults to be used for analogue/mixed-signal CMOS circuits including statistic distributions in values and times.

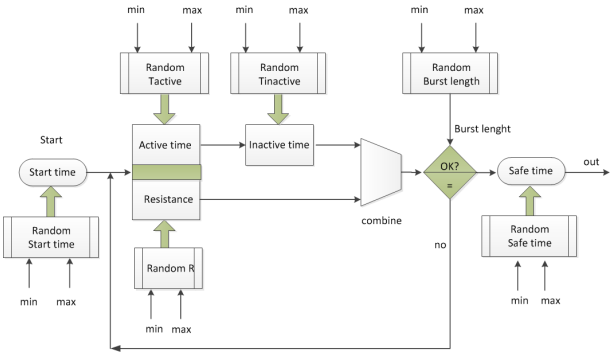


Fig. 3: Basic scheme of a programmable intermittent resistive fault injector for our simulator environment. Resistance, burst number, activation time, inactive time and delay parameters.

The basic scheme of our intermittent resistive fault injector is shown in Fig. 3. There are six parameters that can be set according to the specific application, with a minimum and maximum value and a certain (random) distribution. The values and distributions applied for our simulations are listed in Table I. We employ the concept of *seeds* Sx, enabling an easy replication of the same NFFs for comparisons during simulations. The model has been implemented in Verilog-A, replacing a normal wire in the net list, and is employed in combination with the Cadence Spectre simulation environment.

The begin of a high-rate intermittent burst begins with the random *starttime* generator, with min and max values (Table I) using a uniform distribution; other random

distributions (e.g. Gaussian) are also possible. Then, a random *activation time* (Tactive) is chosen, during which a random *resistance* value R is assigned to this timeframe. This is the first event of a potential burst of events (maximum set to 10 in this paper). After that, an *inactivation time* (Tinactive) between events is randomly generated in which a fault-free situation exists (R=1Ω). In the case of a burst (burst length > 1), there is a feedback loop and the same procedure will be followed again (Fig. 3). After the last event of the burst, the *safe time* is generated, where again there will be a faulty-free situation, thereby completing the intermittent fault procedure. This sometimes long safetime is the major cause of test problems in the case of intermittent faults.

TABLE I: Parameters set as used for our simulations

Parameter	Minimum	Maximum	Distribution
Start time	1µs	10µs	Uniform
Resistance	1 Ohm	1k Ω	Uniform
Tactive	50ns	1µs	Uniform
Tinactive	50ns	1µs	Uniform
Burst length	1	10	Uniform
Safe time	10µs	(years)	Uniform

Two examples of intermittent resistive faults generated by our fault injector are shown in Fig. 4. Note that these are based on a 65nm process and cannot be compared to the figure of the large system in Fig. 1.

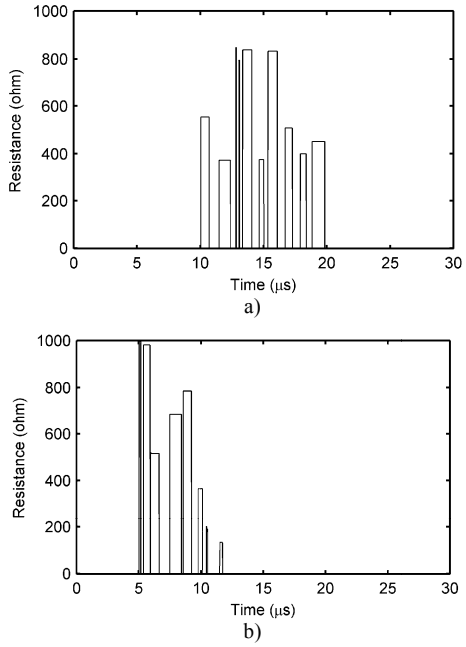


Fig. 4: Two examples of an intermittent resistive fault, generated by our injector. a): R: 1Ω – 850Ω, start time of 10µs, minimum activation and inactivation time, safe time 10µs, and10 events in the burst; all uniform distributions using fixed seed S1. b) R: 1Ω – 1KΩ, start time of 5µs, minimum activation and inactivation time, safe time 15µs, and 8 events in burst; all uniform distributions using fixed seed S2.

In order to get an idea of the influence of the fault parameters on analogue CMOS circuits, a number of experiments have been carried out, to be discussed in the next section.

IV. Intermittent Resistive Fault Simulations in an OpAmp

In this section, the above developed emulator of an intermittent resistive fault has been applied to an OpAmp simulation in 65nm TSMC technology [19]. The full differential OpAmp is shown in Fig. 5. The design makes use of a constant-g_m controlled rail-to-rail input stage, a folding mesh summary stage and a class-AB rail-to-rail output stage. A gain boosting technique is used to further increase the gain, which is realized by three transistor groups M3-M16-M17-M10, M30-M18-M19-M28 and M20-M29-M31. The open-loop gain of the OpAmp is above 80dB for all input common mode voltages. It was connected as an amplifier via a conventional resistive feedback with a gain of 10. The feedback resistor was chosen to be 10kΩ.

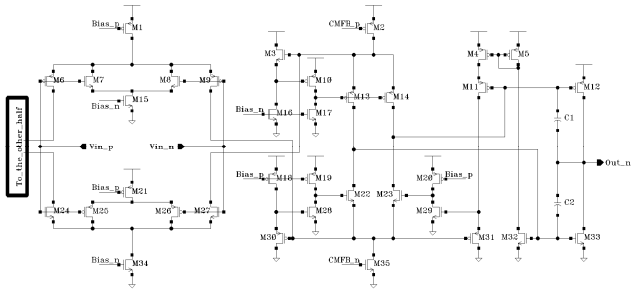


Fig. 5: Basic scheme of our example OpAmp (TSMC 65nm).

As previously discussed, potential bad internal wiring inside the OpAmp will not be considered at this moment because of assumed extremely low probability of occurring; it is stressed this is not a fundamental limitation of our approach. In that case, interconnection problems in PCB soldering, traces (of an OpAmp chip) or in TSVs connecting to other chips remain. Hence, only the *input*, *output* and *power-supply* line of the OpAmp will be considered in the fault injection evaluations.

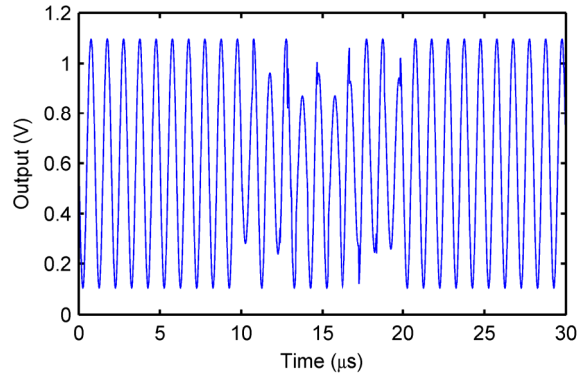


Fig. 6: Simulated output signal of OpAmp with emulated intermittent resistive fault at the *input* of the OpAmp. Table I parameters and all uniform distributions using fixed seed S1.

In order to investigate any influences of intermittent resistances, extreme corners in terms of resistor values, activation and inactivation times have been used. Start time and safe time are considered to have no influence on the final results.

It is obvious, that the particular CMOS circuit implementation, as well as feed-back resistor have a direct influence in the case of a single intermittent resistive fault at the *input(s)*. The target OpAmp has been loaded with a buffer (full feed-back) OpAmp (10MΩ) input. Fig. 6 shows the transient response of the resistive closed-loop from an input sine with 50mV amplitude and 1MHz frequency. It indicates that there is a significant change in gain, which was to be expected. In parallel, also the output voltage frequency spectrum and power-supply current were simulated and evaluated. The output current hardly changed while the spectrum will be dealt with later. In the case of environmental stress (e.g. increased temperature) and long-term aging, the resistive maximum at the input can become so large (worst case, an open) that the gain is lost, and a total failure will result.

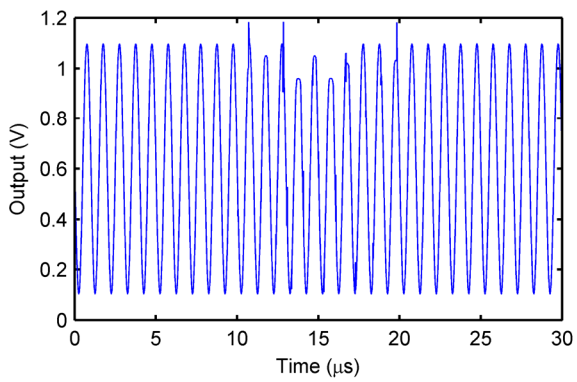


Fig. 7. Simulated output of the OpAmp with emulated intermittent resistive fault at the power-supply line of the OpAmp; parameters according to Table I. All uniform distributions using fixed seed S1.

The next simulation experiment concerned the occurrence of an intermittent resistive fault in the *power-supply* line. This resembles to some extent the presence of an IR drop in a SoC [20]. The simulation in this case for the OpAmp output signal is shown in Fig. 7. The output voltage turns out to be close to the power-supply voltage (1.2V), and hence some non-linear behaviour is likely to occur. This will be shown in its spectrum later on.

Besides the influence on the output signal, an intermittent resistive fault in the *power-supply* line also has a significant influence on the total current consumption. Fig. 8 shows the simulated current consumption. There are series of lower current values as the simulation shows.

This means an intermittent resistive fault in the power line can be detected with a power-supply current monitor. The change of gain in the case of an intermittent resistive can be observed by a (modified) envelope detector [21].

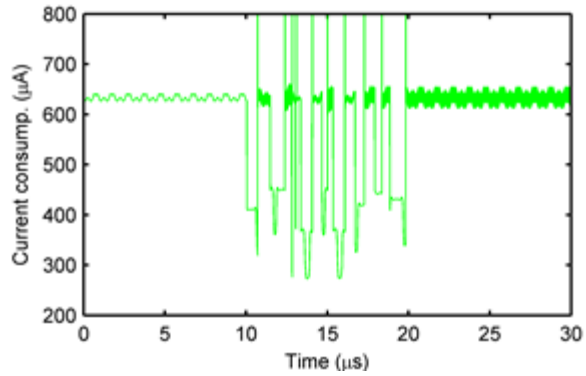
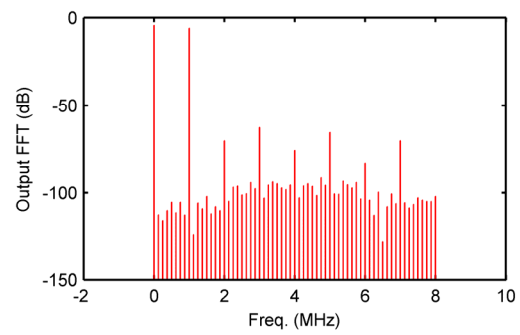


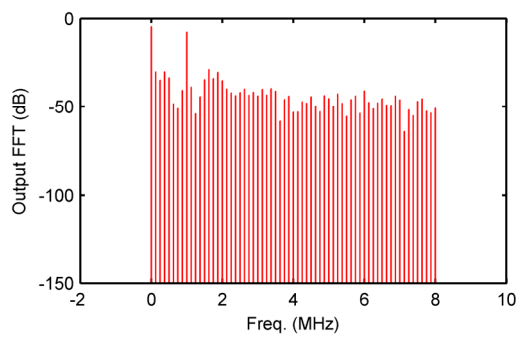
Fig. 8. Simulated power-supply current in the case of an intermittent resistive fault at the power-supply line of the OpAmp. Used parameters are according to Table I.

All simulations resulting from an intermittent resistive fault at the *output* of the OpAmp did not reveal any significant change in either gain, current or spectrum.

Fig. 9 shows the spectrums of the outputs of the OpAmp in two cases (fault-free, input line).



a)



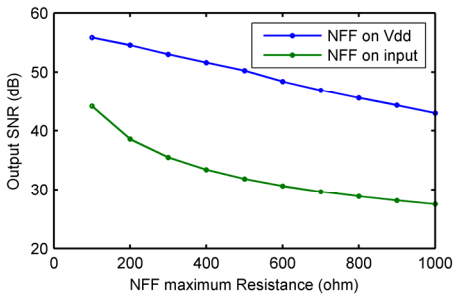
b)

Fig. 9. Simulated OpAmp output spectrums. a) in the fault-free case. b) in the case of an intermittent resistive fault at the *input* of the OpAmp. Used parameters are according to Table I.

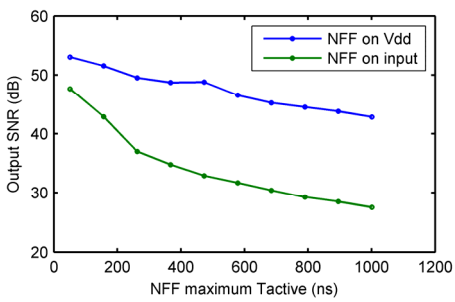
In Fig. 9a, the normal situation in the absence of an intermittent resistive fault is shown (fault-free); it has a low noise floor (~ -100dB) with a number of higher

harmonics. However in Fig. 9b, the spectrum is shown in the case an intermittent resistive fault (Fig. 4a) is present at the input. The actual noise floor has now increased to around -50dB. Or, differently stated, the SNR has been drastically reduced after fault injection introduction. A similar tendency is observed in the case of an intermittent fault in the power supply. An intermittent resistive fault at the output is close to the fault-free case and has hence no influence. The above has stimulated the idea to use the signal-to-noise ratio (*SNR)* in evaluating the influence of the different fault locations.

Fig. 10 shows simulated SNRs for sweeping the intermittent resistance fault parameters.



a)



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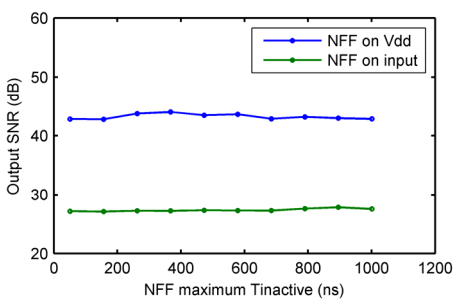

c)

Fig. 10. Influence of intermittent resistance parameters on the output SNR of the example OpAmp. a) Sweeping the NFF maximum resistance. b) Sweeping the maximum Tactive time. c) Sweeping the maximum Tinactive time.

It should be noted that the results are based on 100 seeds per point and Table I data, while the mean value of the SNR is shown. In Fig. 10a, the maximum resistance of the fault is swept from 100Ω to 1KΩ. It can be observed that the SNR is decreasing as the maximum resistance increases. The input has a lower SNR as compared to an intermittent fault at the power-supply line. Fig.10b shows the influence on SNR while changing the maximum Tactive time. It shows the SNR is sensitive to the maximum Tactive in both cases; the input intermittent resistive fault causes the lowest SNR. In Fig. 10c, the maximum Tinactive is swept from 50ns to 1µs. Simulation results indicate that both SNRs are not sensitive for changes in maximum Tinactive. The intermittent resistive fault at the input shows the lowest SNR.

Finally, Fig. 11 shows the SNR of the OpAmp output as function of the number of events in a burst of an intermittent resistive fault in the input and power-supply line. It can be observed that the SNR decreases if the number of events increases, which was to be expected.

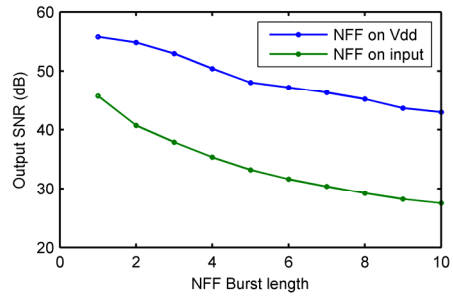

Fig. 11: Influence of sweeping the burst length from 1 to 10 on the output SNR of the example OpAmp.

V. Conclusions and Remarks

In this paper, a first step has been made to investigate the effects of a special category of No Faults Found, being single intermittent resistive faults resulting from interconnection flaws which are random in time, but not in location(s). They are known to be extremely difficult to detect, diagnose and in chips to correct. They occur in PCBs as well as integrated circuits; with the arrival of 3D-TSV in future integrated systems they are likely to occur more frequently than nowadays. To limit the simulation effort, the number of resistive open faults in more complex circuits should be confined; layout-based Inductive Fault Analysis (IFA) should be employed to find the top-ranking probabilities of resistive opens [22].

A simulation injection model for intermittent resistive faults has been developed, based on measurement experiences of others. The parameters in this simulation fault injection model can be extended and changed at will, as are the probability functions.

An example has been investigated; at several locations this type of fault was introduced and its response in an analogue IP, an OpAmp, investigated. It shows that these intermittent resistive faults in the input signal line have the

largest influence, basically introducing a decrease in SNR. These results are particular to this process and design and cannot be generalized for all OpAmps.

One potential approach for intermittent resistive detection can be the simultaneous on-line testing of the most susceptible locations (e.g. input, or power in the case of TSVs). Monitoring the output voltage, current (and frequency) domain can log potential anomalies accompanied by a time stamp and subsequently stored in a log memory to support maintenance / repair later on.

VI. ACKNOWLEDGEMENTS

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