A 12GHz 210fs 6mW Digital PLL with Sub-sampling Binary Phase Detector and Voltage-Time Modulated DCO

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Abstract

An integer-N digital PLL architecture is presented that simplifies the critical phase path using a sub-sampling binary (bang-bang) phase detector. Two power-efficient techniques are presented that can reduce DCO frequency tuning step by voltage-domain and time-domain (pulse-width) modulating the DCO LSB varactors. Measurement shows 210fs RMS jitter at 11.8GHz DCO frequency and 6mW power.

Main Text

Digital PLLs [1]-[4] exploit a digital loop filter offering advantages of re-configurability and small chip area compared to analog PLLs. Despite of the often-used name "All Digital PLL", the digitally-controlled oscillator (DCO) produces an analog carrier with jitter. Jitter is equal to the integral of phase noise, which is affected by both device and quantization noise in the DCO and the time-to-digital converter (TDC).

For an integer-N PLL, a "bang-bang" or binary phase detector (BPD), i.e. 1-bit TDC, is in principle sufficient to convey DCO phase information (early or late) to digital. Traditional bang-bang PLLs (BBPLL) [2]-[4] all share phase and frequency paths in one loop by employing a divider preceding the binary phase-frequency detector. Fig. 1 shows our BBPLL architecture with separate phase and frequency feedback paths. The upper path conveys phase information consisting of a buffer and a BPD, using the reference signal to (sub-)sample the DCO signal. As f_{REF} is much lower than f_{DCO}, locking on many multiples of f_{REF} is possible. To define frequency, the lower path conveys frequency information via a buffer, divider and frequency detector (FD). Note that the phase noise is determined by the phase path while the frequency path merely assists frequency locking and becomes inactive in lock. This separation simplifies the critical path and eliminates divider jitter, while the frequency path can be powered down after locking [5]. The digital loop filter (DLF) consists of a proportional path with gain of 1 and an integral path whose gain is reconfigurable for optimum phase noise.

The architecture using separate phase-frequency paths has been applied in fractional-N digital PLLs [1], however, a binary detector used here is much simpler than a multi-bit TDC required for a fractional-N PLL. This is good for both jitter and power, so we can better explore the advantage of such architecture in an integer-N digital PLL.

A PLL with sub-sampling analog phase detector [5] shows excellent jitter performance by exploring the high slew-rate of a VCO carrier. This translates a small timing error Δt into a big voltage Δv as illustrated in Fig. 2 (left). The sub-sampling BPD enjoys a similar feature and is shown in Fig. 2 (right). A latched sense amplifier [6] is clocked by the reference signal whose rising edge triggers the comparison of the differential DCO signals. The effect of the input-referred noise of the comparator is suppressed by the high slew rate of the DCO signal. Unlike a sample-and-hold in Fig. 2 (left), the BPD can have higher input-impedance and avoids the losses of a switched capacitor which are serious at a high DCO frequency (e.g. 12GHz).

DCO tuning resolution is another bottleneck for phase noise. To reduce quantization noise, a small frequency tuning step is desired, i.e. small capacitor size. To achieve good linearity, switched capacitors are commonly used in DCO tuning, however the minimum capacitor size is limited by IC technology. Typically power hungry high-speed dithering such as sigma-delta modulation (SDM) is applied to decrease effective step size [1] [2]. We present two simple techniques to reduce the minimum DCO step size power-efficiently.

As shown in Fig. 3, the DCO control is split into four banks: three coarse banks PVT (covering PVT variations), ACQ (acquisition) and TR (tracking), and one fine bank determining phase noise (PN). All three coarse banks use MOSFET capacitors switched between VDD and GND; the PN bank uses minimum-size MOSFET varactors switched between VDD and V_{DAC}. Voltage-domain modulation via a 16-level resistor DAC tunes bias voltage V_{DAC} to set the varactor value. Note that the DAC control bits are static once the PLL is in lock, different from the DAC used in [3] and [7] whose 5 dynamic control bits come from the phase detector through the loop filter. This brings two advantages: 1) the DAC resolution does not limit the frequency resolution, instead, the difference between VDD and V_{DAC} determines the frequency step; 2) the interface between digital loop and DCO is only 1 bit which directly fits a binary phase detector. The power dissipation of R-DAC can be made small (e.g. 0.1mA) by selecting high resistor values.

To further reduce the tuning step size, we also propose pulse-width modulation (PWM) for the on-time of the PN-bank capacitor; instead of activating the PN-bank capacitor during the whole reference period T_{REF}, now it is activated by t_{pw}: a fraction of T_{REF}. If the pulse duty cycle is 1/M, then effectively the capacitor value is reduced by a factor of M. To show the concept, here we directly use the REF clock pulse for PWM which has a 1/3 duty cycle (M=3). If needed, this concept can produce much smaller step size by adopting a narrower pulse width. Note that the PWM scheme is simpler than the pulse-density modulation in a SDM. It is also power efficient since all clocks involved are running at the low frequency (f_{REF}) through simple logics, compared to SDM.

The proposed digital PLL has been implemented in a 65nm CMOS technology with a total area of $1mm^2$ (active area of $0.15mm^2$) as shown in Fig. 4. At 55MHz reference and 12GHz DCO, the power consumption is 6mW, with an LC-type DCO and its loop buffer taking the majority (about 40% and 25% respectively). The divider consumes an extra 1mW.

The DCO is tunable from 10.2GHz to 13GHz. The minimum varactor size produces a frequency step >300kHz, while the voltage modulation brings it down to <10kHz and the PWM improves it further by 3x. This level of frequency resolution is sufficient to reduce DCO quantization noise to below thermal noise of our target. The measured phase noise of the PLL is shown in Fig. 5 at a carrier frequency of 11.8GHz, with an in-band noise floor of -100dBc/Hz, and an integrated jitter from 10kHz to 20MHz of 210fs. Above 20MHz the phase

noise floor is due to DCO measurement buffer.

Table 1 compares this work with other recently published bang-bang PLLs at ISSCC [2]-[4]. To a directly comparable 11GHz PLL [2], this work achieves 2x better jitter at 1/5 power dissipation, thanks to the proposed techniques. Note that the 200fs mentioned in the title of [2] does not count in-band phase noise due to a specific wireline application. For a figure of merit considering jitter and total power (FoM_{jitter}) [8], this work is at least 5dB better. Considering in-band phase noise and loop power (FoM_{IBPN}) [8] to compare PLLs using different DCO types, this work is at least 8dB better.

Acknowledgements

The authors thank Dutch government for funding the SPITS project and NXP for donating the chip fabrication.

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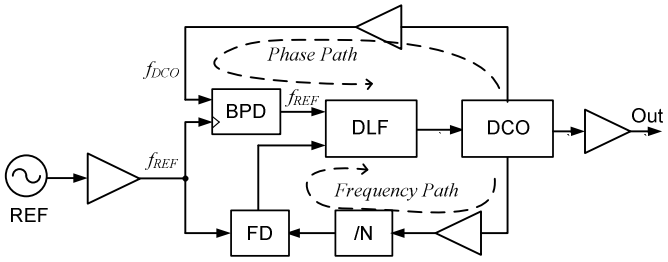

Fig. 1. Sub-sampling BBPLL architecture minimizing components on the critical phase path by separating the frequency path

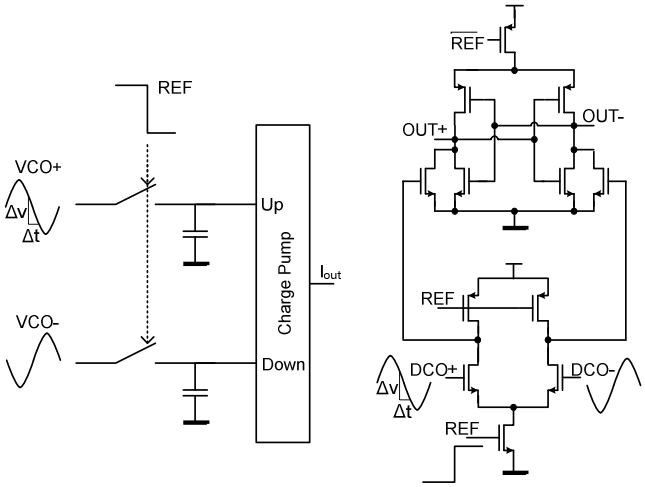

Fig. 2. Sub-sampling analog phase detector (left) and Sub-sampling binary phase detector (right)

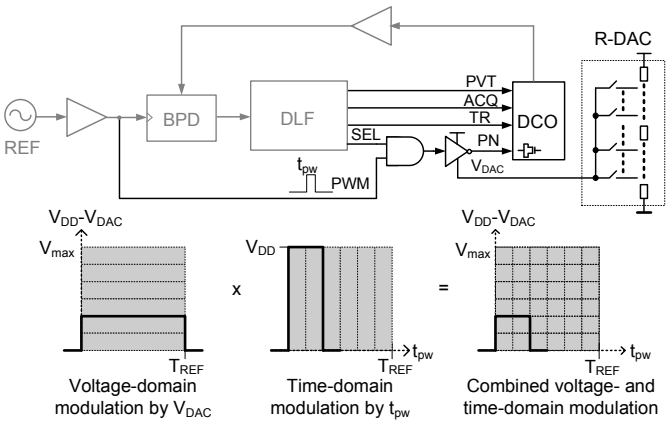

Fig. 3. Reducing DCO minimum step size by voltage-domain modulation (V_{DAC}) and time-domain pulse-width modulation (PWM)

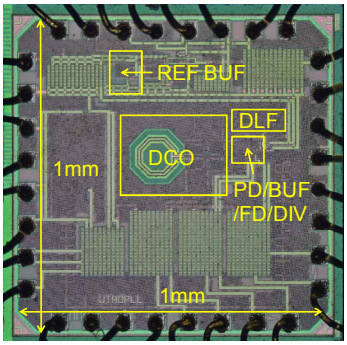

Fig. 4. Micrograph of the 65nm CMOS chip (active area 0.15mm^2)

Fig. 5. Measured phase noise at 11.8GHz carrier frequency

		This Work	[2] ISSCC09	[3] ISSCC11	[4] ISSCC12
DCO type		LC	LC	LC	Ring
Carrier Frequency (f_c)		11.8GHz	11GHz	3.3GHz	1.5GHz
In-Band Phase Noise (IBPN)		-100dBc/Hz	-97dBc/Hz	-102dBc/Hz	-89dBc/Hz
RMS Jitter (σ_t) [10k to 20M]		210fs	400fs	400fs	19ps
Power	DCO	2.5mW	31mW	1.7mW	2.5mW
	Loop	3.5mW		2.8mW	
FoM_{jitter}		-246dB	-233dB	-241dB	-210dB
FoM_{IBPN} [1]		-296dBc/Hz	-286dBc/Hz	-288dBc/Hz	-272dBc/Hz
CMOS Tech.		65nm	65nm	65nm	32nm

[1] FoM for in-band phase noise: half of total power is assumed as loop power if no separate data reported.

$$FoM_{jitter} = 10\log\left[\left(\frac{\sigma_t}{1s}\right)^2 \cdot \frac{P_{tot}}{1mW}\right] \qquad FoM_{IBPN} = IBPN + 10\log\left[\left(\frac{1Hz}{f_c}\right)^2 \cdot \left(\frac{P_{loop}}{1mW}\right)\right]$$

Table 1. Comparison with other Bang-Bang PLLs