# A general weak nonlinearity model for LNAs

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***Abstract*- This paper presents a general weak nonlinearity model that can be used to model, analyze and describe the distortion behavior of various low noise amplifier topologies in both narrowband and wideband applications. Represented by compact closed-form expressions our model can be easily utilized by both circuit designers and LNA design automation algorithms. Simulations for three LNA topologies at different operating conditions show that the model describes IM components with an error lower than 0.1% and a one order of magnitude faster response time. The model also indicates that for narrowband IM2@$w_1$-$w_2$ all the nonlinear capacitances can be neglected while for narrowband IM3 the nonlinear capacitances at the drain terminal can be neglected.**

## I. Introduction

The low noise amplifier (LNA) is a critical building block in the RF front-end. One of the important design specifications of the LNA is its distortion performance, typically specified in terms of IIP2 and IIP3. A number of papers present nonlinearity analyses for LNAs to provide design guidelines [1-2] or for LNA design automation purposes [3-4]. Volterra series theory is widely used as the major nonlinearity analysis approach [5]. Trying to avoid the complex calculation involved in Volterra series, other approaches include:

*A.* Per-nonlinearity distortion analysis [6]

*B.* Combined multisine and Volterra analysis [7]

*C.* Harmonic distortion analysis in feedback amplifiers [8]

Approach *A* treats a MOS transistor as a linear component with a nonlinear drain current source, which allows identifying the transistors that contribute most to the output nonlinearity. Although all the drain-source nonlinearities can be included, no information is given about which nonlinearity of the drain current has more effects [7]. Approach *B* splits the nonlinear behavior in similar contributions as in approach *A* while better insights on the nonlinearity contribution are achieved by using the selective Volterra analysis. Both approach *A* and *B* demand distortion simulations of the circuit to provide the data for post-processing, which is not meant for hand-calculation analysis. Alternatively approach *C* only uses conventional algebra to analyze harmonic distortion of feedback amplifiers but can't provide solutions for intercept 1-dB compression point and intermodulation distortions. Despite the complexity difference in all aforementioned methods the nonlinearity analysis must be redone for each new topology.

In this paper we introduce a general weak nonlinearity model that is independent of the LNA topologies. Theoretically, for any LNA topology both in narrowband or wideband applications, this model calculates output IM2 and IM3 of the circuit using simple closed-form expressions. The compact closed-form expression is just a linear combination of nonlinear coefficients of each MOS transistor and terminal AC gains. Therefore, the result of our model can be easily utilized by both circuit designers and LNA design automation algorithms without involving any complex nonlinearity analysis. In section II the weak nonlinearity model for MOS transistor valid from DC to RF frequencies is introduced. Using this MOS nonlinearity model a generalized distortion analysis for weakly nonlinear circuits is discussed in Section III, which presents the approach to obtain the general weak nonlinearity model. Section IV shows the benchmark on accuracy for our model using three different LNAs operating in different load condition and at different frequencies. Conclusions are drawn in section V.

## II. MOS Transistor Nonlinearity Modeling

In this paper it is assumed that MOS transistors' nonlinearities are the (main) cause for distortions in RF-circuits. Therefore, for analyzing the nonlinear behavior of RF circuits, modeling and describing transistor nonlinearity is essential. Taylor series are successfully and dominantly used to describe the weakly nonlinear behavior of the MOS transistor [1-5]. However, most of these descriptions simplify the MOS nonlinearity model to the following extent:

- Only consider transconductance nonlinearity [1-3].
- Consider all resistive drain current nonlinearity but neglect the charge-storage nonlinearity [5], [7- 8].

Aiming for validity from DC to the RF frequency range, we introduce a complete weakly nonlinear model taking into account both resistive and charge-storage nonlinearity.

A MOS transistor is a four-terminal device, in which all currents into and charges at nodes are nonlinear functions of the voltages across any two terminals. Mathematically the transistor can be modeled as a three-port network with the gate-source, drain-source and bulk-source voltage as the inputs and gate current, drain current and bulk current as outputs for any given DC bias. Therefore the transistor's weakly nonlinear behavior in the close vicinity of any DC bias point can be described by the multi-dimensional Taylor series up to (here) the third-order, which is given by

$$\begin{aligned} i_k(t) = {} & G^k_{100}v_{gs} + G^k_{200}v^2_{gs} + G^k_{300}v^3_{gs} + G^k_{010}v_{ds} + G^k_{020}v^2_{ds} + G^k_{030}v^3_{ds} + G^k_{001}v_{bs} \\ & + G^k_{002}v^2_{bs} + G^k_{003}v^3_{bs} + G^k_{110}v_{gs}v_{ds} + G^k_{120}v_{gs}v^2_{ds} + G^k_{210}v^2_{gs}v_{ds} + G^k_{101}v_{gs}v_{bs} \\ & + G^k_{102}v_{gs}v^2_{bs} + G^k_{201}v^2_{gs}v_{bs} + G^k_{011}v_{ds}v_{bs} + G^k_{012}v_{ds}v^2_{bs} + G^k_{021}v^2_{ds}v_{bs} + G^k_{111}v_{gs}v_{ds}v_{bs} \\ & + C^k_{100}\frac{dv_{gs}}{dt} + C^k_{200}\frac{dv^2_{gs}}{dt} + C^k_{300}\frac{dv^3_{gs}}{dt} + C^k_{010}\frac{dv_{ds}}{dt} + C^k_{020}\frac{dv^2_{ds}}{dt} + C^k_{030}\frac{dv^3_{ds}}{dt} + C^k_{001}\frac{dv_{bs}}{dt} \end{aligned} \quad (1)$$

$$+C^k_{002}\frac{dv^2_{bs}}{dt}+C^k_{003}\frac{dv^3_{bs}}{dt}+C^k_{110}\frac{dv_{gs}v_{ds}}{dt}+C^k_{120}\frac{dv_{gs}v^2_{ds}}{dt}+C^k_{210}\frac{dv^2_{gs}v_{ds}}{dt}+C^k_{101}\frac{dv_{gs}v_{bs}}{dt}$$
$$+C^k_{102}\frac{dv_{gs}v^2_{bs}}{dt}+C^k_{201}\frac{dv^2_{gs}v_{bs}}{dt}+C^k_{011}\frac{dv_{ds}v_{bs}}{dt}+C^k_{012}\frac{dv_{ds}v^2_{bs}}{dt}+C^k_{021}\frac{dv^2_{ds}v_{bs}}{dt}+C^k_{111}\frac{dv_{gs}v_{ds}v_{bs}}{dt}$$

where

$$C^k_{mnl}=\frac{1}{m!}\frac{1}{n!}\frac{1}{l!}\frac{\partial^{(m+n+l)}Q_X}{\partial V^m_{gs}\partial V^n_{ds}\partial V^l_{bs}}\quad;G^k_{mnl}=\frac{1}{m!}\frac{1}{n!}\frac{1}{l!}\frac{\partial^{(m+n+l)}I_k}{\partial V^m_{gs}\partial V^n_{ds}\partial V^l_{bs}}\quad k\in\{g,d,b\}$$

are respectively the nonlinear capacitive and resistive coefficients with $Q_k$ for charge at and $I_k$ for current into terminal $k$. For simplicity reasons, in this paper the source and bulk are assumed to be connected, effectively reducing the MOS-transistor to a three-terminal device. As a result only the currents into and charges stored at the gate, drain and source are of concern and hence coefficients $C^k_{mnl}$ and $G^k_{mnl}$ with $l\neq 0$ are zero. Furthermore, the DC gate current is neglected and only the capacitive gate current is taken into account, which is a valid simplification for RF operation [9].

The weak nonlinearity model is shown in Fig. 1a, where the linear current sources ($i_{g,lin}$ and $i_{d,lin}$) and nonlinear current sources ($i_{g,nonlin}$ and $i_{d,nonlin}$) are separated for the circuit distortion analysis discussed in next section. Other capacitances that may be present in the MOS transistor structure can be included in this representation. For example the interconnect capacitance between the gate and drain may be added explicitly across the terminals, but can also be embedded in (1) by using e.g. the Blakesley transform.

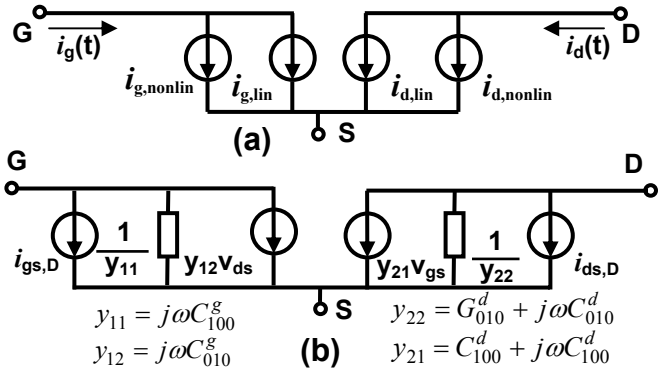


Fig. 1. Weak nonlinearity model for the MOS transistor in (a) time-domain and (b) frequency domain.

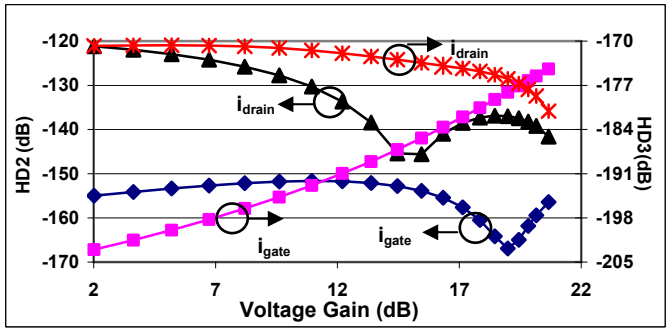


Fig. 2. Comparison on HD2@2GHz and HD3@3GHz in gate and drain current between ADS [13] simulation and the MOS nonlinearity model for different voltage gains ($v_{ds}/v_{gs}$). Symbols represent model prediction, lines transistor-level circuit simulation using a commercial 90nm CMOS process ($f_T$=110GHz)

The nonlinear coefficients are extracted directly from state-of-art MOS model, namely the PSP model [14], which ensures excellent accuracy. Very good agreement with the simulated HD2 and HD3 in gate and drain current is observed for transistors with different dimensions and bias, one of which is shown in Fig. 2 with the transistor under different voltage gain ($v_{ds}/v_{gs}$) conditions.

## III. Generalized Distortion Analysis

In this section a general circuit with $N$ transistors is analyzed. A two-tone input signal $V_{IN}e^{j\omega_1 t}+V_{IN}e^{j\omega_2 t}$ is applied assuming that amplitude $V_{IN}$ is small to ensure the circuit operates in the weakly nonlinear region. The MOS transistors are assumed to be the only nonlinearity sources in the circuit, although this assumption is not necessary. Since no topology information is involved the analysis result is valid for all topologies.

### A. Dependent relation

The frequency-domain MOS nonlinearity model shown in Fig.1b is used. It consists of first-order y-parameters (directly converted from the linear coefficients in (1)) and two distortion current sources (gate distortion current source $i_{gs,D}$ and drain distortion current source $i_{ds,D}$) that contain both harmonic and intermodulation distortion elements. In the frequency domain $i_{gs,D}$ and $i_{ds,D}$ can be regarded as (dependent) small-signal multi-tone stimuli, therefore in any circuit with $N$ transistors the distortion in the circuit output is a linear combination of $i_{gs,D}$ and $i_{ds,D}$ from each transistor. Moreover, the terminal voltages of each transistor ($v_{gs}$ and $v_{ds}$) are linear combination of $i_{gs,D}$ , $i_{ds,D}$ from each transistor and the two-tone input signal, which in total yield

$$v_{out,D}=\sum_{k=1}^{N}(H_{igsk}\circ i_{gsk,D}+H_{idsk}\circ i_{dsk,D}) \tag{2}$$

$$v_{dsj}=\sum_{k=1}^{N}(F^{dsj}_{igsk}\circ i_{gsk,D}+F^{dsj}_{idsk}\circ i_{dsk,D}+F^{dsj}_{vin}(\omega_1)\cdot V_{IN}e^{j\omega_1 t}+F^{dsj}_{vin}(\omega_2)\cdot V_{IN}e^{j\omega_2 t}) \tag{3}$$

$$v_{gsj}=\sum_{k=1}^{N}(F^{gsj}_{igsk}\circ i_{gsk,D}+F^{gsj}_{igsk}\circ i_{dsk,D}+F^{gsj}_{vin}(\omega_1)\cdot V_{IN}e^{j\omega_1 t}+F^{gsj}_{vin}(\omega_2)\cdot V_{IN}e^{j\omega_2 t}) \tag{4}$$

where $H_{ixsk}\ x\in\{g,d\}$ is the AC gain to the output voltage when an AC current source applied between the terminal $x$ and source in transistor k; $F^{ysj}_{ixsk}\ x\in\{g,d\}, y\in\{g,d\}, x\neq y$ is the voltage gain from the current source attached between the terminal $x$ and source in transistor $k$ to the terminal voltage $v_{ys}$ in transistor $j$; $F^{ysj}_{vin}\quad y\in\{g,d\}$ is the AC gain from voltage input to the terminal voltage $v_{ys}$ in transistor $j$.

In summary (2) suggests that the output voltage distortion can be easily calculated once all the distortion current sources are known. (1), (3) and (4) indicate a dependent relation between the controlling voltage $v_{gs}$ and $v_{ds}$ and the distortion current sources of each transistor as illustrated in Fig. 3.

### B. Solving for the general model

The dependent relation shown in Fig 3 generates a linear

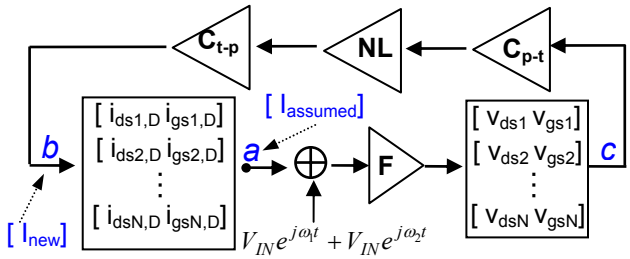


Fig. 3. Illustration of the dependent relation between the distortion current sources and the controlling voltages in any circuit with *N* transistors. Block "F"and "NL" represent the calculation conducted in (3)-(4) and (1) respectively. Block "$C_{p\text{-}t}$" represents the conversion from phasors to the according time-domain expressions and "$C_{t\text{-}p}$" for vice-versa.

equation matrix for solving the closed-form expressions of each distortion current sources ($i_{gsk,D}$, $i_{dsk,D}$, k=1,⋯ N). At first the assumed expression matrix [$I_{assumed}$] for $i_{gsk,D}$ and $i_{dsk,D}$ are input to node *a*. Given the weak nonlinear assumption, [$I_{assumed}$] contains distortion elements up to the third-order, where the magnitude of second-order distortions should be proportional to $V_{IN}^2$ and the magnitude of the third-order distortions to $V_{IN}^3$, any terms with higher-order of magnitude is small enough to be neglected. Following the loop counterclockwise until node *b* we can obtain a new expression matrix [$I_{new}$]. Up to the third-order [$I_{assumed}$] should be equal to [$I_{new}$], which provides the solution for the expressions of $i_{gsk,D}$, $i_{dsk,D}$. Then the circuit output distortion can be easily obtained from (2).

Meanwhile the matrix solving is significantly simplified due to the observation in (3) and (4) that only the terms with fundamental tones contribute to the second-order distortion; only the terms with fundamental tones and second-order tones contribute to the third-order distortion. Therefore other terms in (3) and (4) can be neglected for the calculation of second and third order distortions.

As a result the closed-form expressions for the output harmonic and intermodulation distortions are obtained. Due to the space limitation only their compact forms are given

$$v_{out,\omega_{IM}} = \sum_{k=1}^{N} [P^d_{mn0,k} \cdot (G^d_{nm0,k} + j\omega_{IM} C^d_{mn0,k}) + P^g_{mn0,k} \cdot j\omega_{IM} C^g_{nm0,k}] \quad (5)$$

where $P_{mn0,k}^{j}$ is a function of according AC terminal gains; $\omega_{IM}$ is the intermodulation frequency; $G_{mn0,k}$ and $C_{mn0,k}$ are the nonlinear conductances and capacitances in transistor *k* at terminal gate/drain. We've observed that in a 90nm CMOS process up to 5 GHz $G_{mn0,k}^{d}$ is more than one order of magnitude larger than both $\omega C_{mn0,k}^{d}$ and $\omega C_{nm0,k}^{g}$ and thus for lower RF frequency (5) can be simplified to

$$v_{out,\omega_{IM}} \approx \sum_{k=1}^{N} (P^d_{mn0,k} \cdot G^d_{nm0,k} + P^g_{mn0,k} \cdot j\omega_{IM} C^g_{nm0,k}) \quad (6)$$

or $$v_{out,\omega_{IM}} \approx \sum_{k=1}^{N} (P^d_{mn0,k} \cdot G^d_{nm0,k}) \quad , \text{if } P^g_{mn0,k} \approx P^d_{mn0,k} \quad (7)$$

which provides the following circuit design insights for any LNA topology in a CMOS technology:

a. For narrowband IM2 ($\omega_{IM}$@low frequency) all the nonlinear capacitances can be neglected and only three second-order conductances of each transistor are important, namely, nonlinear transconductance ($G_{200}$), output conductance ($G_{020}$) and cross-modulation conductance ($G_{110}$ ).
b. For IM3 ($\omega_{IM}$@ RF tone) the nonlinear capacitances at the drain terminal can be neglected and if $P_{mn0,k}^{g}$ is not much larger than $P_{mn0,k}^{d}$ the nonlinear capacitances at the gate terminal can also be neglected.

In summary this generalized distortion analysis shares an approach that has similarities with harmonic balance analysis in approximating all node voltages and branch currents by truncated Fourier series. By utilizing the diagram shown in Fig. 3 and cutting redundant frequency elements our analysis method simplifies complex weakly nonlinear analyses into relatively simple calculations. The resulting general weakly nonlinear model can be applied for different LNA topologies as will be shown next. The model uses simple closed-form expressions to describe the total output distortion for both narrowband and wideband application, which is just linear combination of the nonlinear coefficients of each transistor and terminal AC gains. In fact this general model can also be applied to [10] where a state-space approach is used to get low complexity analytic expressions of distortions for different fully balanced band Gm-C filters

## IV. Benchmark On Accuracy

In order to evaluate the accuracy of the proposed general nonlinearity model, a common source (CS) amplifier, a narrowband cascode LNA [11] and a broadband noise-canceling LNA [12] are simulated in ADS using a commercial 90nm CMOS process. The topologies are shown in Fig. 4. The general LNA nonlinearity model is integrated in parametric cells (P-cells) [4] to provide distortion prediction.

The CS amplifier is an example verifying the two design insights given in the previous section. Fig. 5 shows that for narrowband IM2 three nonlinear conductances are the key factors, which verifies the design insight *a*. For the CS amplifier $P_{mn0,k}^{g}/P_{mn0,k}^{d} \approx g_m(Z_{Cgs}//R_s)$ is typically around 1~2 and thus insight *b* is applied ,which is verified in Fig. 6 that all nonlinear capacitances at gate and drain terminals can be neglected for narrowband IM3. For the other two LNAs the 0simulated results by ADS and the results of our model are compared on output IM2 and IM3. The accuracy is defined by $\left|1 - \left|\frac{V_{ADS} - V_{model}}{V_{ADS}}\right|\right|$, where $V_{ADS}$ and $V_{model}$ are the ADS-simulated and model results for voltage magnitude of IM respectively. For the narrowband LNA the two-tone signal is at 5 GHz with 1 MHz spacing. By sweeping the load ($Z_{Load}$) the model is benchmarked for different gains as shown in Fig. 7. For the wideband LNA one tone is fixed at 1 GHz and the other tone is swept from 2.15 GHz to 10 GHz resulting in a perfect description of IM2 and IM3 at different frequency shown in Fig. 8.

In summary the benchmark shows the proposed general nonlinearity model predicts the output distortion for different topologies with very good accuracy. The simple closed-expressions with the model enable a very fast response time for calculating IM distortions (within 40 ms per one sweep)

providing over one order of magnitude advantage versus the transistor-level simulation in ADS, thus making it very suitable for implementation in a design automation loop for optimizing the circuit within short time.

## V. Conclusion

A general weak nonlinearity model for different low-noise amplifier topologies was presented, which is achieved by our generalized weak nonlinearity analysis. Implemented by simple closed-form expressions this model provides a potential solution for LNA design automation with different topology candidates to improve the response time and for the circuit designers to gain insightful guidelines on LNA nonlinearity. Very good accuracy and short response time of this model is shown on intermodulation distortion calculation for different LNAs in both narrowband and wideband applications.

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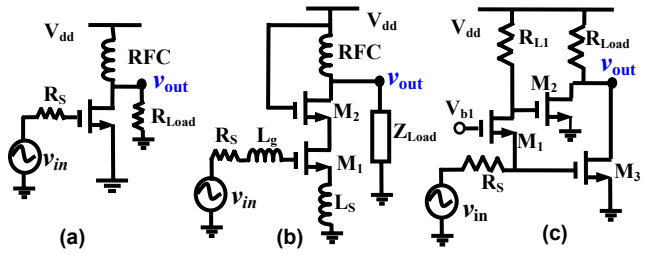


Fig. 4. Schematics of (a) CS amplifier, (b) narrowband cascode LNA and (c) wideband noise-cancelling LNA

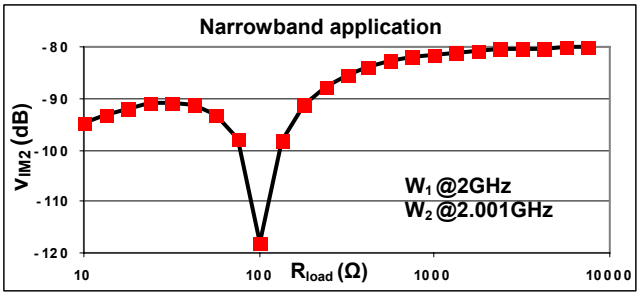


Fig. 5 Comparison between simulated (line) and model (symbol) results on output voltage IM2@1MHz for a CS amplifier as a function of load resistance. Squares represent the model (only contains three nonlinear conductances and neglects nonlinear capacitances).

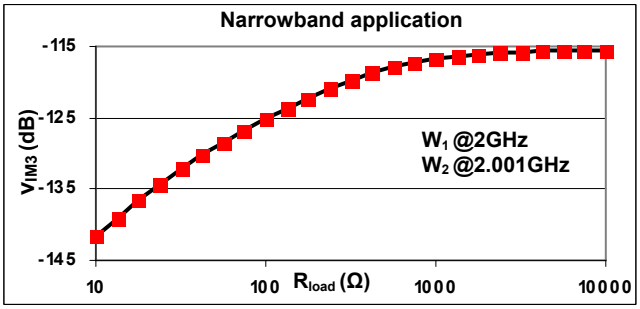


Fig. 6 Comparison between simulated (line) and model (symbol) result on output voltage IM3@1MHz for a CS amplifier as a function of load resistance. Squares represent the model (neglecting nonlinear capacitances at gate and drain terminals)

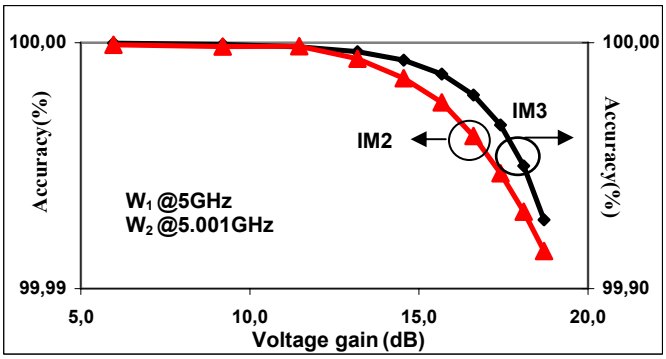


Fig. 7 Accuracy of our model on IM2 and IM3 for narrowband cascode LNAs over different voltage gain ($v_{out}/v_{in}$)

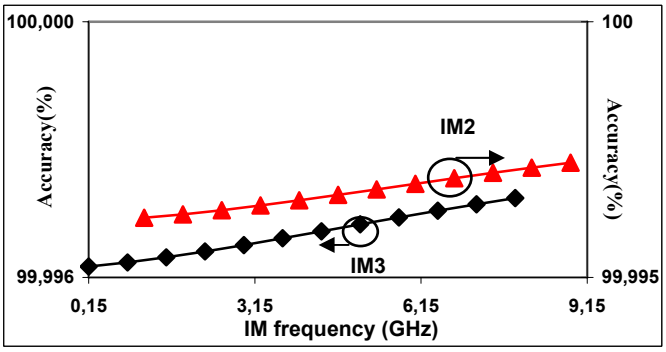


Fig. 8 Accuracy of our model on IM2 and IM3 prediction for a wideband LNA ( IM2 @$w_1$-$w_2$ ranging from 1.15 GHz to 8.85GH; IM3@$w_2$-2$w_1$ ranging from 0.15GHz to7.85GHz)