A Software-Defined Radio Receiver in 65nm CMOS Robust to Out-of-Band Interference

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Abstract — Two techniques are presented in this paper for a software-defined radio (SDR) receiver robust to out-of-band interference. Voltage gain is realized at IF simultaneously with low-pass filtering to mitigate blockers and out-of-band intermodulation distortion. A 2-stage polyphase harmonic rejection (HR) mixer concept robust to gain error achieves 2^{nd}-6^{th} HR of more than 60dB for 40 samples without trimming or calibration. A prototype 0.4-0.9G zero-IF receiver in 65nm CMOS has 34dB gain, 4dB NF, +3.5dBm IIP3 and +47dBm IIP2 while drawing 50mA from 1.2V**.**

Index Terms **- Software-Defined Radio, Out-of-Band Interference, Blocker Filtering, Harmonic Rejection, Wideband, CMOS**

I. INTRODUCTION

In a software-defined radio (SDR) receiver we like to minimize RF band-filtering for flexibility, size and cost reasons, but this leads to increased out-of-band interference (OBI). Besides harmonic and intermodulation distortion (HD/IMD), OBI can also lead to blocking and harmonic mixing. A wideband LNA [1, 2] amplifies signal and interference with equal gain. Even a low gain of 6dB can clip 0dBm OBI to a 1.2V supply, blocking the receiver. Hard-switching mixers not just translate the wanted signal to baseband but also the interference around LO harmonics. Harmonic rejection (HR) mixers have been proposed [3, 1, 4], but are sensitive to phase and gain mismatch. Indeed the HR in [4] shows big spread, whereas other work only shows results from one chip [3, 1]. This paper will propose techniques to relax blocking and HD/IMD, and make HR robust to mismatch.

II. INTERFERENCE-ROBUST SDR RECEIVER

Our zero-IF architecture targets at the 0.4-6GHz band, where most mobile applications reside. The baseband can be shared if the low-pass filter (LPF) is made flexible. As shown in Fig. 1 (bottom), only two external filters for 0.4-2.5G and 2.5-6G are used. The 0.9-6G signals are down-converted by the lower quadrature mixer using a 4-phase LO, while the 0.4-0.9G signal needs a HR-mixer with 8-phase LO to reject 2^{nd}-6^{th} harmonics (0.4G·7 and 0.9G·3 out of filter band). With only one 0.4-6G band filter, an 8-phase LO up to 2GHz would be needed, leading to high power consumption and low phase accuracy. This work focuses on a 0.4-0.9G receiver to demonstrate techniques to counter OBI.

Fig. 1 shows the implemented receiver, consisting of low-noise transconductance amplifiers (LNTA) with input matching added, mixers driven by a divide-by-8 and two cascaded IF-amplifier stages with LPF. Three LNTAs have a gain ratio of 2:3:2 to approximate 1:√2:1 for HR. The LNTA delivers current to the switching mixers. The voltage amplification only occurs after mixing to IF simultaneously with a 1^{st}-order RC LPF to suppress OBI. However, such a filter cannot remove OBI already folded over the wanted signal due to

harmonic mixing. Since harmonics can be as strong as blockers, HR is wanted before the first voltage amplification. The mixers driven by 8-phase clocks provide 2^{nd}-6^{th} order HR.

To reject 3^{rd} and 5^{th} harmonics we can employ gain factors 1:√2:1 and 45° phase shift [3]. Traditionally zero-IF HR mixers deliver quadrature outputs. We propose a 2-stage polyphase HR idea exploiting 8-phase mixer outputs (Fig. 1). The 2^{nd}-stage HR uses gain-ratio of 5:7:5 (via resistor ratios 7:5:7), and the 45° phase shift comes from the 8-phase baseband signal. The 2-stage HR provides two benefits: a) it uses integer ratios which can be realized accurately on chip to approximate √2 closely; b) it reduces the total gain error, e.g. due to mismatch or parasitics, to a product of gain errors (1% becomes 0.01%). Fig. 2 (top) shows a calculation of how √2 is approximated to 0.03% error as 41:29 by simple integer 2:3:2 and 5:7:5 ratios. This 41:29 ratio in the effective LO amplitude is constructed via three signal paths, each with a weighing factor of stage 1 (time-dependent factor 0, 2 or 3 in the array) and stage 2 (constant 5 or 7). Fig. 2 (bottom) shows how for the desired signal, polyphase contributions from three paths add up, while for the 3^{rd} and 5^{th} harmonic, they cancel nominally. As two stages are cascaded, the product of the gains determines the result. *This means that the total relative error ($\alpha\beta/4$) is the product of the relative errors (1^{st} stage: $\alpha/2$, 2^{nd} stage: $\beta/2$).* If the 2^{nd} stage has 1% error (β), this improves HR by $(\beta/2)^{-1}$, i.e. 46dB.

With such a large reduction of gain errors, phase errors are likely to dominate. We propose a power-efficient divider with minimum phase-error accumulation. The divide-by-8 is a loop with eight dynamic transmission gate (TG) flip-flops (FF), one of which is shown in Fig. 3. The same master clock (CLK) with 8-times the LO-frequency clocks all FFs. Only one inverter (INV2) is used as buffer to minimize the path from CLK to mixer, to minimize phase mismatch. A preset data pattern is required to deliver the wanted 1/8 duty cycle. The simulated 3σ phase error is only 0.34° at 0.8G LO including contributions from mixer switches.

Fig. 3 shows the LNTA. M1 provides input matching while the input is also connected to the AC-coupled inverter (M2, M3). The source of M1 is biased to GND via an external inductor. Since the LNTA outputs see a low TIA input impedance, its output swing is small and output distortion low. The distortion caused by in-band interference is suppressed by the negative feedback (Fig. 1). The loop-gain degrades at high frequency, but the LPF suppresses OBI, improving out-of-band linearity. So out-of-band HD/IMD is dominated by the V-to-I function of LNTA. The TIA is based on a two-stage OTA with a class-AB output for high swing [5]. A receiver with LNTA and TIA combination has been presented in [6], however using a narrowband LNTA and no HR. To our knowledge this work proposes the first wideband receiver exploiting the baseband LPF to suppress OBI. In [7], a feedforward path, using mixers and 1^{st}-order high-pass filter, cancels OBI at the LNA output, but it significantly degrades noise.

The chip occupies an active area of $1mm^2$ in 65nm CMOS (Fig. 7). Capacitors take a large portion of area in TIA, and also the OTA input pair is big for low 1/*f* noise corner (measured at 30kHz). To prove the receiver is robust to OBI, we did all measurements on PCB without external filter. Fig. 4 shows the measured gain, NF and in-band IIP2/IIP3. The NF degrades at 0.4GHz due to 1/*f* noise of LNTA since minimum-length transistors are used for wideband low S11 to show valid HR at high frequency (measured S11<-10dB up to 5.5GHz). The frequency range (<1GHz) is limited by clock speed, but the signal path has >5GHz BW (simulation). Fig. 4 also shows signal gain versus blocker power. The measurement was carried out to imitate DVB-H signals (470M & 862M) with a GSM blocker at 935MHz. The signal gain is reduced by 1dB at a blocker power of -5dBm (470M) and -12dBm (862M) respectively, well above the measured 1dB compression point of -22dBm, showing the blocker filtering is effective. Smaller LPF BW or higher filter order can provide more filtering.

Fig. 5 (top) plots the HR ratio (HRR) from 1-stage only and the total 2-stage HR of a typical sample.

A dramatic improvement of 30dB for both 3rd and 5th HR is found, thanks to the 2-stage HR technique. In general, the improvement is in the range of 20-40dB for all samples. Fig. 5 (bottom) shows the 2-stage HRR of 40 randomly-selected samples measured at 0.8G LO. The minimum 3rd HRR is 60dB and 5th HRR is 64dB. All even-order HRR are >60dB. Without extra RF filtering, the 3rd and 5th HRR in literature is around 40dB [1,4]. This work achieves a minimum of 60dB without any calibration. Fig. 6 summarizes the measured parameters. The +18dBm out-of-band IIP3 shows the good linearity of the LNTA.

III. Conclusion

We presented a SDR receiver with enhanced robustness to out-of-band interference. A 2-stage polyphase harmonic rejection mixer concept robust to gain error achieves 2nd-6th HR of more than 60dB for 40 samples without trimming or calibration. Voltage gain is realized at IF simultaneously with LPF to mitigate blockers and out-of-band intermodulation distortion, achieving +3.5dBm in-band IIP3 at a high gain of 34dB.

Acknowledgment

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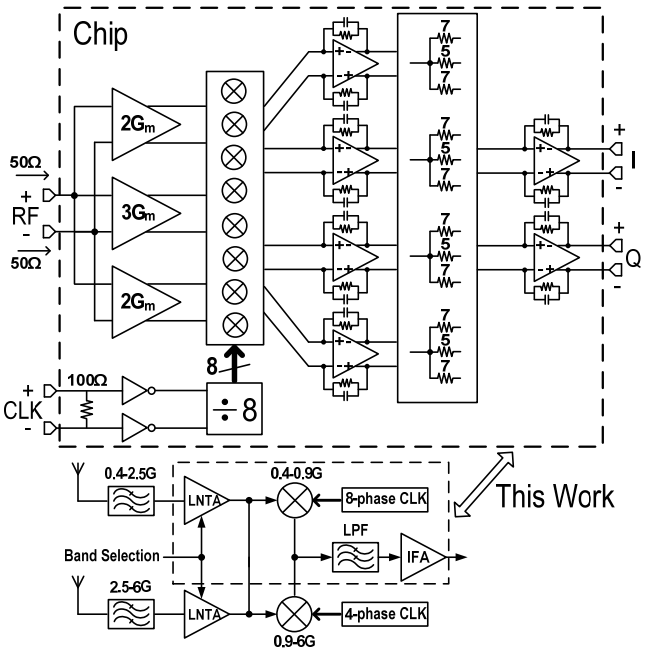

Figure 1: Architecture of the interference-robust software-defined radio receiver.

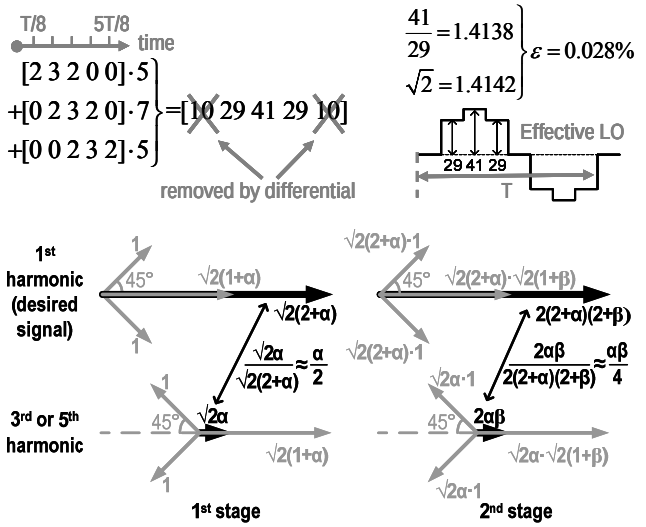

Figure 2: Principle of the 2-stage polyphase harmonic rejection. (α and β are errors in √2 of the 1st and 2nd stages respectively, but it also works for errors in 1:1 mismatch.)

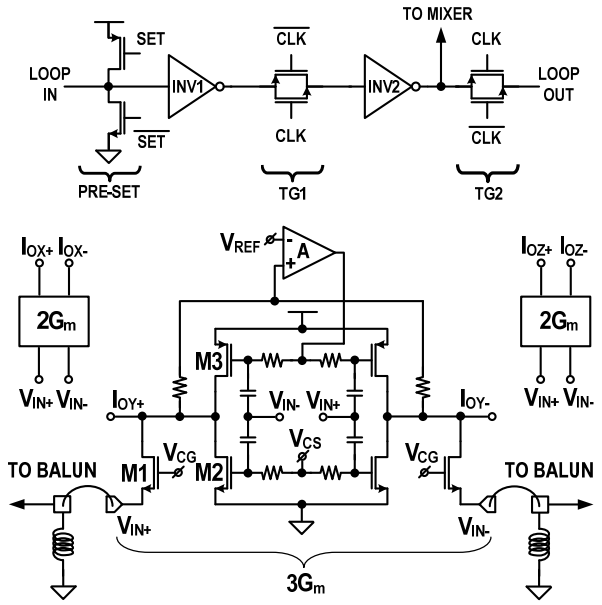

Figure 3: Dynamic transmission-gate flip-flop and low-noise transconductance amplifier.

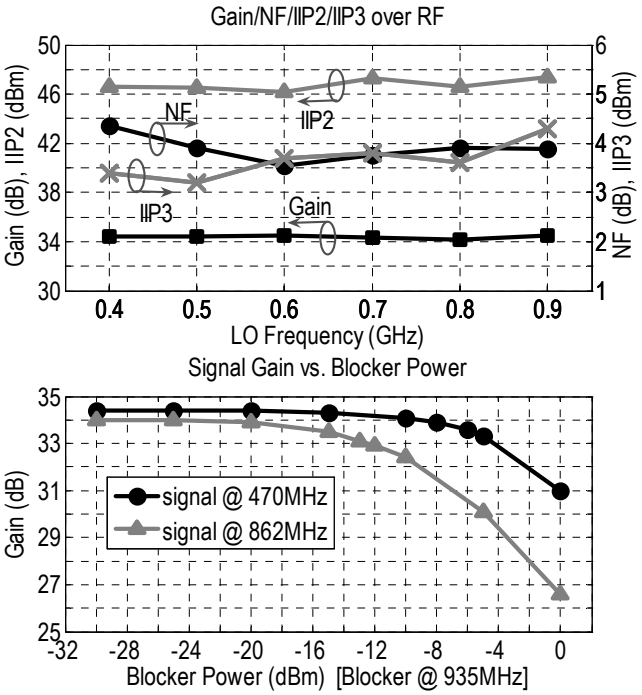

Figure 4: Measured gain, NF, in-band IIP2/IIP3 over RF; measured signal gain vs. blocker power.

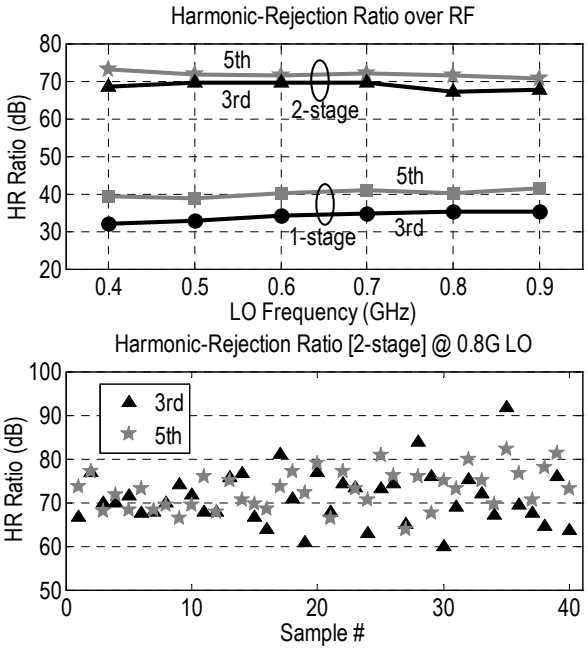

Figure 5: Measured harmonic-rejection (HR) ratio.

Frequency	0.4-0.9GHz
S11 < -10dB	80M-5.5GHz
Gain	34.4± 0.2dB
DSB NF	4dB
In/Out-of-band IIP3[1]	+3.5dBm / +18dBm
In/Out-of-band IIP2[2]	+47dBm / +51dBm
CP1dB	-22dBm
1/f noise	30kHz corner
IF BW	12MHz

VDD	1.2V
Current Consumption	Analog: 33 mA
	Digital (clock): 8 mA @ 0.4G 17 mA @ 0.9G

Harmonic Rejection Ratio (40 samples) @ 0.8G LO	
3rd-order	> 60dB
5th-order	> 64dB

[1] Out-of-band IIP3 scenario: 1.61G & 2.40G
[2] Out-of-band IIP2 scenario: 1.80G & 2.40G

Figure 6: Summary of measured key parameters.

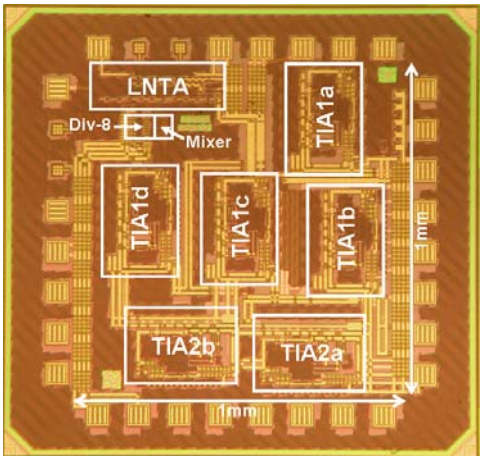

Figure 7: Micrograph of the chip fabricated in a 65nm baseline CMOS.