19.6 A sub-1V Bandgap Voltage Reference in 32nm FinFET Technology

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The bulk CMOS technology is expected to scale down to about 32nm node and likely the successor would be the FinFET. The FinFET is an ultra-thin body multi-gate MOS transistor with among other characteristics a much higher voltage gain compared to a conventional bulk MOS transistor [1]. Bandgap reference circuits cannot be directly ported from bulk CMOS technologies to SOI FinFET technologies, because both conventional diodes cannot be realized in thin SOI layers and also, area-efficient resistors are not readily available in processes with only metal(lic) gates. In this paper, a sub-1V bandgap reference circuit is implemented in a 32nm SOI FinFET technology, with an architecture that significantly reduces the required total resistance value.

The conventional CMOS bandgap voltage reference adds a proportional-to-absolute-temperature (PTAT) voltage and a complementary-to-absolute-temperature (CTAT) voltage to get a stable output voltage that is approximately equal to the material bandgap. The CTAT voltage typically is obtained from a forward-biased diode, e.g., a source-well junction. The resulting reference voltage in CMOS is then about 1.2V, which does not fit in the supply voltage of today's deep sub-micron CMOS technologies. In [2] one of the most widely applied approaches to create good sub-1V bandgap reference circuits is presented and serves as the basis for many circuit implementations, e.g., [3]. A disadvantage of the approach in [2] is that it uses a number of matched high-ohmic resistors that take a significant die area for low-power reference circuits.

SOI FinFET-transistors do not have wells, which eliminates the possibility of using source-well junctions as diodes. As replacement for the typical source-well junction in bulk CMOS processes, a lubistor [3] structure is implemented with the poly tied to ground, similar to the work in [4]. The lubistor structure is shown in Fig. 19.6.1; the gate-material layer above the pn-junction shields the junction from silicidation (i.e. prevents shorting the pn-junction) while an n-type background dope ensures that the region below the shield is non-intrinsic. Due to the lateral junction in the thin silicon layer, the area efficiency is quite low: structures are designed with 1.4µm pitch having 60nm junction height. The dimensions of the diodes in this work, are estimated using 2D semiconductor simulations, resulting in a total of 440µm junction-width per unit diode, which corresponds to 440µm×1.4µm/2=308µm^2 die area and 440µm×60nm=26.4µm^2 effective junction area; for circuit simulations of the total circuit the FinFET-model in [5] is used.

In the SOI FinFET technology used in this work no high resistivity layers are available to allow the creation of dedicated resistors: resistors then are area-inefficient and Banba's approach [2] would result in a large area overhead. Resistorless voltage references in CMOS either show poor accuracy and reproducibility or, are targeted at 1.2V output voltages [6]. Therefore, the approach in this paper uses two relatively small resistors and resistorless weighted-averaging to realize area efficient sub-1V bandgap voltage references, see Fig. 19.6.2. The principle of a conventional bandgap voltage reference can be captured in one relation that describes the voltage-temperature behavior: $V_{ref}(T) = PTAT + CTAT \approx N \cdot \frac{kT}{q} + 1.2 - \frac{2mV}{K} \cdot T$. Here the term $\frac{kT}{q}$ is created by the difference voltage across two diodes operated at different current densities, the term $1.2 - \frac{2mV}{K} \cdot T$ approximates the diode's voltage drop as a function of temperature and N includes things like resistor ratios, diode area ratios, and current-mirror ratios in the circuit. Adding a PTAT and CTAT voltage yields a (in first order) temperature independent output voltage for $V_{ref}(T) \approx 1.2V$. Noting that,

$$V_{ref} = PTAT + CTAT \approx 1.2V \Leftrightarrow \frac{V_{ref}}{m} = \frac{PTAT + CTAT}{m} \approx \frac{1.2V}{m}$$

it directly follows that by weighted averaging of a CTAT voltage and a PTAT voltage a temperature independent sub-bandgap output voltage can be obtained. In related work in [7,8] averaging is done using relatively high-ohmic resistors. In this work, matched OTAs are used to replace the high ohmic resistors in such a way that OTA non-linearity is cancelled, while the reverse isolation of the OTAs decouples the core of the bandgap reference circuit from the output voltage. The total bandgap voltage reference circuit in Fig. 19.6.2 uses two identical OTAs that yields m=2 and hence, an output voltage of about 0.6V. A total of 56kΩ of resistors is used, at 14µA of supply current at room temperature. Compared to using the Banba approach, this is about 6× less in total resistor value for the same supply-current level.

The die micrograph of the FinFET sub-1V bandgap reference is shown in Fig. 19.6.3. The total area of the bandgap voltage reference circuit is about 100×160µm^2. For this design, the total active area can be broken down in 54% diode area, 31% resistor area, and 15% MOS-transistor area. The large diode area is due to the low area efficiency of lubistor structures in thin-body SOI processes. The resistors are implemented as narrow silicided poly lines. Apart from this, some of the area inside the 100×160µm^2 is unused or means for testing purposes.

Figure 19.6.4 shows the I(V) plots of two different lubistors for various temperatures. The left hand side shows typical behavior for the lubistor in the circuit with the highest current density: the leftmost diode in Fig. 19.6.2. The dots correspond to the typical quiescent point in the bandgap reference circuit, which is a little into the region where the I(V) relation starts to deviate from the ideal exponential behavior. The rightmost lubistor in Fig. 19.6.2 has a 10× lower current density and therefore, operates in the exponential regime. The origin of the bump for the curve at 25°C is unexplained, but located well below the quiescent point. The right hand side of Fig. 19.6.4 shows the I(V) behavior of a misbehaving lubistor, for which, the bump occurs in the operating region, making the bandgap reference circuit dysfunctional. It must be noted that this technology is not released for production and is still in an experimental phase.

Figure 19.6.5 shows the output voltage of the reference as a function of supply voltage for a few samples at room temperature. The circuit operates correctly for supply voltages above 0.9V; the sharp transition in the output voltage is due to the start-up circuit. Figure 19.6.6 shows the output voltage of one sample as a function of temperature, at low temperature, the increase in output voltage is mainly due to surface leakage currents due to moist; at high temperature the main cause for the roll-off is the operation into the high-injection region of the lubistor. The measured supply current is 14µA at room temperature.

Acknowledgement:
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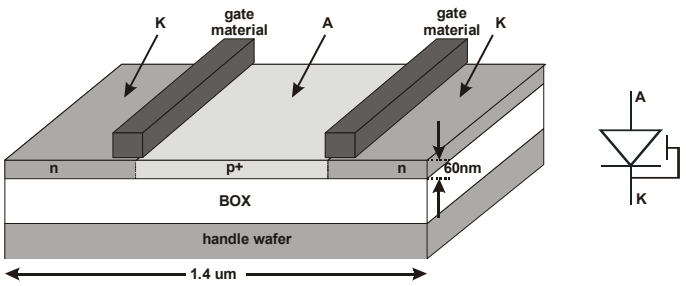

Figure 19.6.1: Lubistor structure (used as a pn-junction).

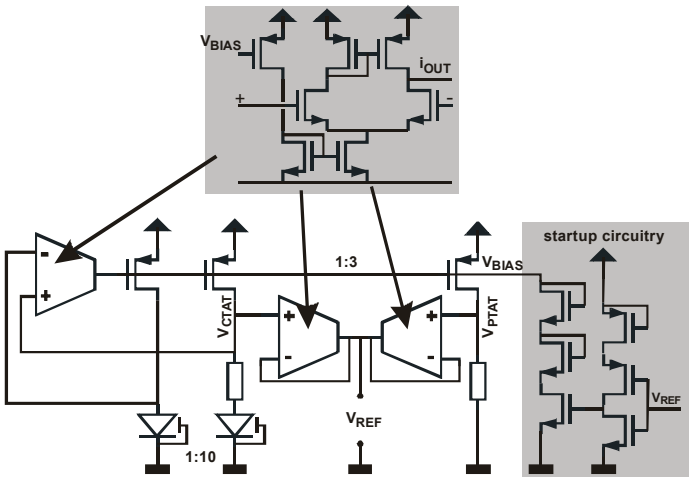

Figure 19.6.2: The sub-1V bandgap circuit in a 32nm FinFet technology.

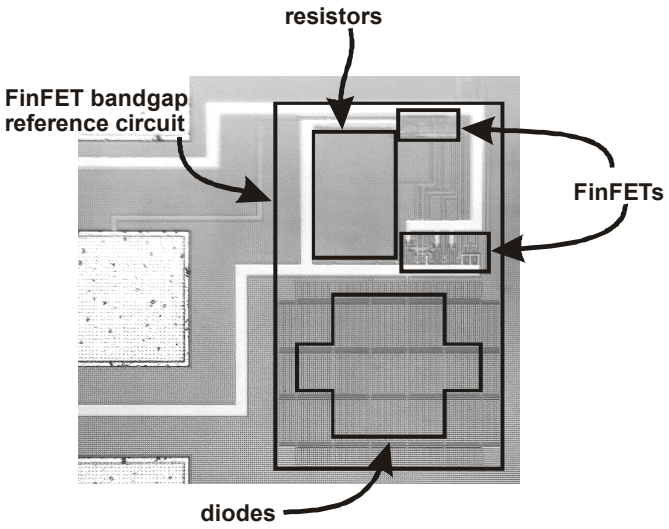

Figure 19.6.3: Die micrograph of the bandgap reference circuit in a 32nm FinFET technology, size 100×160μm².

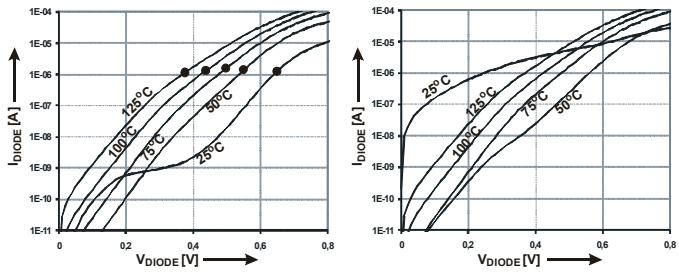

Figure 19.6.4: Lubistor measurement results for a decent lubistor with dots indicating the quiescent point in the bandgap reference circuit (left) and a misbehaving lubistor (right).

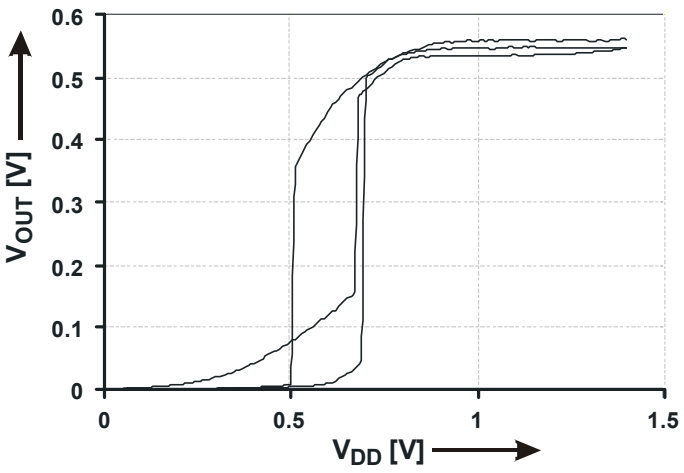

Figure 19.6.5: Output voltage as a function of supply voltage, 3 samples.

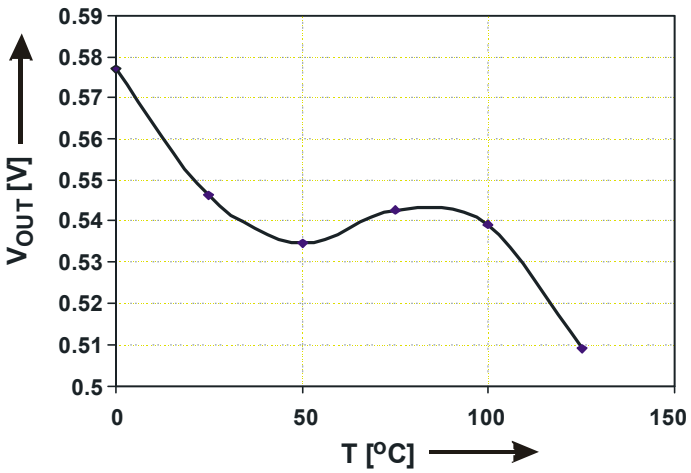

Figure 19.6.6: Output voltage as a function of temperature, 1 sample.