A wideband Noise-Canceling CMOS LNA exploiting a transformer

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***Abstract* — A broadband LNA incorporating single-ended to differential conversion, has been successfully implemented using a noise-canceling technique and a single on-chip transformer. The LNA achieves a high voltage gain of 19dB, a wideband input match (2.5–4.0 GHz), and a Noise Figure of 4–5.4 dB, while consuming only 8mW. The LNA is implemented in a 90nm CMOS process with 6 metal layers.**

***Index Terms* — CMOSFET amplifiers, broadband amplifiers, Low Noise Amplifier, LNA, transformers, autotransformers.**

I. Introduction

Triggered by multi-standard radios and the upcoming Ultra Wideband standards, the interest in broadband receiver techniques has increased over recent years. A number of different CMOS LNAs combining a wideband input-match and gain have been proposed. To compensate for capacitive effects, several inductors are often used [1–4]. Especially in nano-scale technologies inductors are considered expensive, as a complete microprocessor might fit in the same area. To reduce area, a promising wideband technique is the Noise Canceling (NC) technique, which in principle does not require any inductors [5]. In [5] a shunt-feedback LNA is designed and measured. An alternative single input, differential output NC-topology, consisting of a parallel operating Common Gate (CG) and Common Source (CS) stage, was also proposed, but not implemented. This paper reports results on this CG-CD LNA, just as recently done in [3]. However, whereas [3] uses 5 inductors, we only use a single on-chip transformer, which takes about the same area as a single inductor. Moreover, this transformer is exploited to the maximum, by using it simultaneously for biasing, source-impedance matching and for noiseless, powerless, voltage amplification. Section II describes how the NC technique can be applied to a CG-stage. The evolution from the basic idea to a complete implementation is presented in Section III. Measurement results and a comparison to previous work are given in Section IV. Finally, the conclusions are drawn in Section V.

II. The Noise-Canceling technique applied to a Common Gate input stage

The CG-stage is well known for its wideband input match, and can realize wideband gain via a drain resistance (R_{CG}). Neglecting feedback from the drain, the minimum NF of a CG-stage matched to a source impedance is limited to about 4 dB, assuming a Noise Excess Factor (NEF = γ / α) of 1.5 for sub-micron CMOS processes. For a number of broadband standards, this NF is low enough to implement a receiver with acceptable sensitivity, provided one can realize enough gain to reduce the noise contribution of later stages. However, the transconductance g_m of the CG-stage is fixed by the matching, while the next stage determines the capacitive load. As a result, only the resistance R_{CG} remains as a design variable, and a trade-off between gain (high R_{CG}) and bandwidth (low R_{CG}) exists.

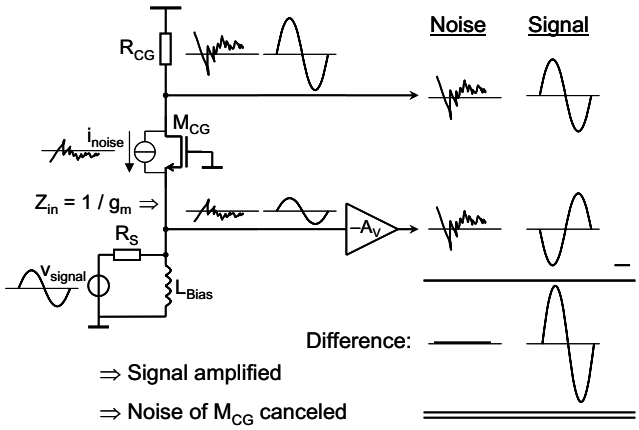

Fig 1: The Noise Canceling Technique applied to a CG-stage.

To remove this trade-off between gain and bandwidth – that is, to increase the gain while maintaining the same bandwidth – a second-stage can be added. A disadvantage is that such an additional amplifier will generate noise and consequently degrade the NF of the complete LNA-circuit. However, as shown in [5] the additional amplifier can be used to cancel the noise of the CG-stage. By applying the NC technique, the gain-bandwidth of the LNA can be increased while maintaining a low overall NF. Figure 1 shows this technique conceptually.

Assuming impedance matching, half of the noise generated by the CG-transistor (i_{noise}) flows via R_S to ground and generates a voltage variation at the source of M_{CG}. The same current necessarily has to flow via R_{CG} and will lead to voltage variation at the drain of M_{CG} (see Fig. 1). These two noise-voltages at drain and source are fully correlated, as they have a common origin (i_{noise}), and are in anti-phase. In contrast, the voltages resulting from v_{signal} at the source and drain are in-phase. This property is exploited in the Noise Canceling Technique. The voltage at the source, a sum of noise and wanted signal, is amplified ($-A_V$) and subtracted from the voltage at the drain. As indicated in Figure 1, the noise is canceled because two correlated voltages with equal amplitude are subtracted. However, the wanted signal will increase in amplitude. This is because the wanted voltage at the drain of M_{CG} and at the amplifier (A_V) output, are combined in a constructive manner. The amplifier will clearly also generate noise, how to design a low-noise implementation will be discussed in the next section.

The required voltage gain of the voltage amplifier ($A_{req} = -A_V$) is easily calculated. A part (say α) of the noise, generated by i_{noise}, will leave transistor. This factor α depends on the source match; $\alpha = ½$ for perfect source matching. However, its value is not relevant in the calculation of A_{req}. The noise resulting from i_{noise} is canceled when the resulting noise-voltage at the output of the voltage amplifier ($v_{noiseAV}$) is equal to the noise-voltage at the output of the CG-stage ($v_{noiseCG}$)

$$v_{noiseAV} = v_{noiseCG} \quad \Leftrightarrow$$

$$\alpha \cdot i_{noise} \cdot R_S \cdot A_{req} = \alpha \cdot i_{noise} \cdot R_{CG} \quad \Rightarrow \quad A_{req} = \frac{R_{CG}}{R_S} \qquad (1)$$

Equation (1) shows that the required voltage gain is equal to the ratio of the common gate resistor and the source resistance. The input impedance of the CG-stage equals $1/g_{mCG}$. When the source is matched, this is equal to the source resistance: $R_S = 1/g_{mCG}$. The required gain can now be expressed as:

$$A_{req} = \frac{R_{CG}}{R_S} = \frac{R_{CG}}{1/g_{mCG}} = g_{CG} \cdot R_{CG} = A_{V,CG} \qquad (2)$$

From (2), the following conclusion can be drawn: the noise canceling condition is met (for a matched input impedance) when the gain of the voltage amplifier equals the voltage gain of the CG-stage. This is a highly desirable property, since source-matching, noise-canceling, and balun-like operation can be obtained simultaneously.

III. Evolution of the Implemented LNA

From the basic principle, described in the previous section, to a fully implemented circuit, requires a number of steps and decisions. This section describes how the original idea has evolved into the final circuit.

First of all, the CG-stage needs to be biased. A low-noise method of biasing the CG-stage is using an inductor between the transistor source node (CG-input) and ground (as shown in Figure 2; top left). An additional advantage is that there is no DC-voltage drop across the inductor. The voltage headroom available for the CG-stage is thus maximized by using an inductor, which is important – especially to achieve high gain at low supply voltages (high voltage drop across R_{CG}). An on-chip inductor will be used for this purpose, even though it occupies a large area compared to the active transistor area. Alternatively, if desired the inductor can easily be moved outside the chip.

As discussed in the previous section, Noise Canceling removes the output noise generated by the CG-transistor. The key to a low overall NF has now shifted to a low-noise implementation of the inverting voltage amplifier ($-A_V$). The most elementary implementation is a resistively loaded Common Source (CS) stage (Figure 2; bottom left). The transconductance (g_m) of this stage should be chosen to be as high as possible, in order to minimize the NF. However, the maximal achievable g_m is limited by biasing and power consumption constraints.

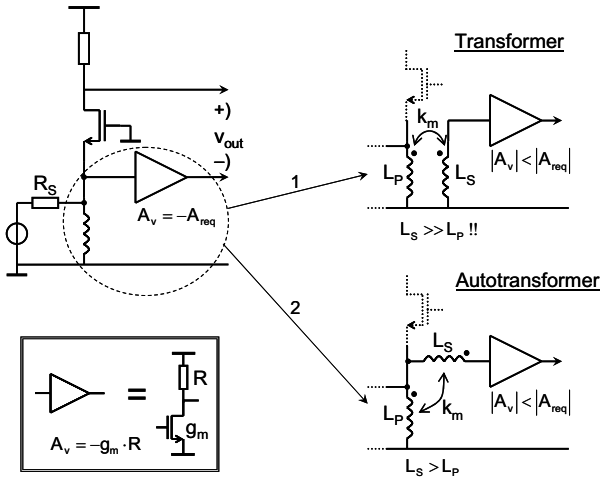

Fig. 2: Alternatives for the implementation of the voltage amplifier A_V.

The top right of Figure 2 shows an alternative to the simple CS-implementation of the voltage amplifier. This configuration exploits the principle that an ideal transformer realizes a noiseless voltage gain at zero power consumption. Such a transformer can be created by inter-twining two inductors. Because an inductor is already

present at the source of the CG-stage, this intertwined transformer will demand only a slight increase in area. The voltage amplifier behind the transformer isolates the output from the input and can still be implemented with a CS-stage. Due to the voltage amplification of the transformer, the requirements placed on the CS-stage are now reduced in two ways: (1) the voltage amplification of the CS-stage can be reduced; and (2) the transconductance (g_m) can be lowered since its noise contributes now less to the overall NF.

The voltage amplification of the transformer should be maximized in order to minimize the noise contribution of the CS-stage. The voltage amplification of a transformer is given by: $A_{V,trans} = k_m \cdot \sqrt{L_S / L_P}$, with k_m the magnetic coupling between primary and secondary windings and L_P and L_S their respective inductances. Typically, a k_m of 0.75 – 0.9 is attained for on-chip transformers [6]. To assess the feasibility of such a transformer, a modest transformer voltage amplification of 2 (6 dB) is assumed. For $A_{V,trans}$ = 2, it follows that L_S should be 5 – 7 times larger than L_P. These ratios are, in principle, realizable; however, wideband matching constraints put a limit to the minimum acceptable inductance of L_P. This results in a high inductance of L_S, which is accompanied by a too low self-resonance frequency (more specifically: $f_{selfres}$ < 10 GHz for multi-GHz operation), which in turn will impair the intended operation of the transformer.

However, an auto-transformer configuration requires much less inductance in the secondary winding for the same voltage gain than a traditional transformer. This configuration is shown at the bottom-right of Figure 2. By stacking the primary and secondary windings, the required ratio L_S / L_P is reduced. The voltage amplification of the autotransformer is given by: $A_{V,auto} = 1 + k_m \cdot \sqrt{L_S / L_P}$. When again a voltage gain of $A_{V,auto}$ = 2 is assumed, the required ratio L_S / L_P is reduced to only 1.2 – 1.8, using the previously assumed k_m-range. This reduction of roughly 4 times of L_S / L_P (from 5 to 1.2) makes it feasible to design a circuit suitable for multi-GHz operation.

The implemented LNA is shown in Figure 3. The part within the box is integrated in a standard digital 90nm CMOS process. The balun at the output converts the differential 100 Ω output impedance of the LNA into a single-ended 50 Ω for measurement purposes. In the circuit, cascode transistors are used to improve the gain and reverse isolation. A symmetric, low-ohmic output is created by the source followers, which do not load the CG- and CS-stages too much.

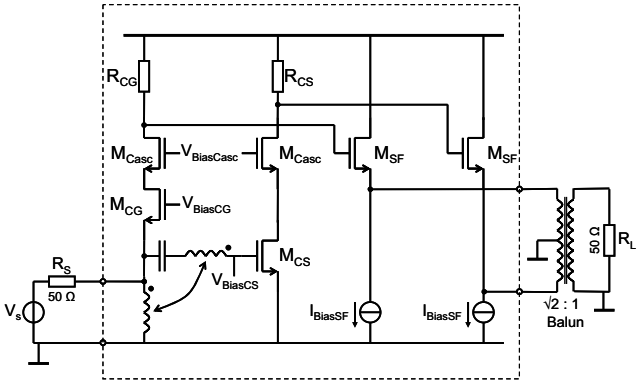

Fig. 3: Simplified schematic of the complete LNA.

The circuit is capable of driving a mixer directly and performs a single-ended to differential conversion. An external balun at the input is thus not needed, which gives a fundamental advantage in system NF. The loss of an input balun (1–2 dB) would add up directly to the total NF.

The effective inductance of the transformer, mainly determined by L_P, resonates with the effective capacitance at the input. An acceptable S_{11} over a broad frequency-range is obtained by keeping the parasitic capacitance as low as possible, which results in a low-Q parallel RLC-section.

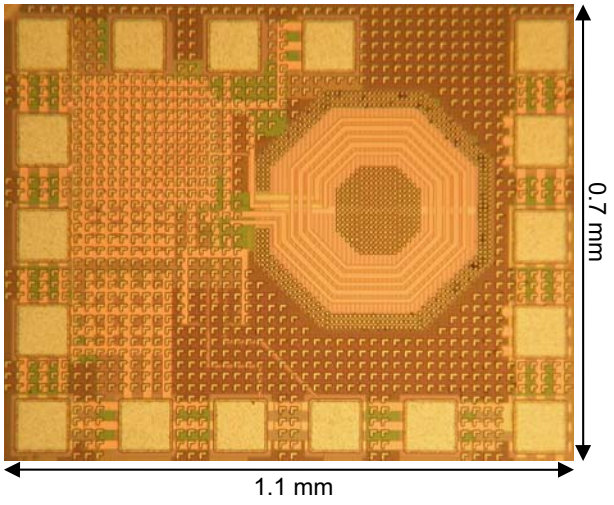

Fig. 4: Die photo of the CS-autotrafo-CG LNA.

The die photo of the LNA is shown in Figure 4. The transformer – consisting of two intertwined inductors – is clearly visible. The single-ended G-S-G input pads are located on the top, while the differential G-S-S-G output pads can be found at the bottom. The five pads at the left side are used to supply and bias the circuit. The chip size measures 0.7 × 1.1 mm, whereas the active area –without pads– covers an area of only 0.2 μm^2. Metal tiles cover a major part of the die to fulfill density rules.

TABLE I

COMPARISON OF PUBLISHED WIDEBAND CMOS LNAS

Ref.	S11 [dB]	$S21_{max}$ [dB]	BW [GHz]	NF_{min} / NF_{max} [dB]	IIP3 [dBm]	Topology	Tech-nology	P_{dis} core (total) [mW]	# inductors	Area [mm^2] (excl.pads)
[1] 2003	< -8	8.1	0.6 – 22	4.3 / 6.0	-	Distributed	0.18 µm CMOS	52	8	~0.7
[2] 2004	< -9.9	9.3	2.3 – 9.2	4.0 / 9.0	-6.7	LC-filter based	0.18 µm CMOS	9 (18)	5	~0.5
[3] 2005	< -10	10*	0.1 – 6.5	3 / 4.2	+1 (sim.)	Noise-canceling + LC-filter	0.13 µm CMOS	12	5	~0.4
[4] 2005	< -9	9.8	2.4 – 4.6	2.3 / 4.0	-7	Induct. deg. + res. shunt feedback	0.18 µm CMOS	12.6 (16.2)	3 (2 off-chip)	~0.4
This design	< -10	10.6	2.5 – 4.0	4.0 / 5.4	-8	Noise-canceling + transformer	90 nm CMOS	8 (16)	1	0.2

*) article reports 19dB *voltage* gain

IV. MEASUREMENT RESULTS AND COMPARISON

The measured S-parameters and Noise Figure are shown in Figure 5. The S_{11} dips below –10 dB from 2.5–4.0 GHz. In this frequency range the S_{21} is above 10 dB, and the NF is lower than 5.4 dB, with a minimum of 4.0 dB at 3.3 GHz. The S_{12} is under –40 dB from 1–8 GHz (not shown) and S_{22} is below –15 dB over the complete 1–10 GHz range.

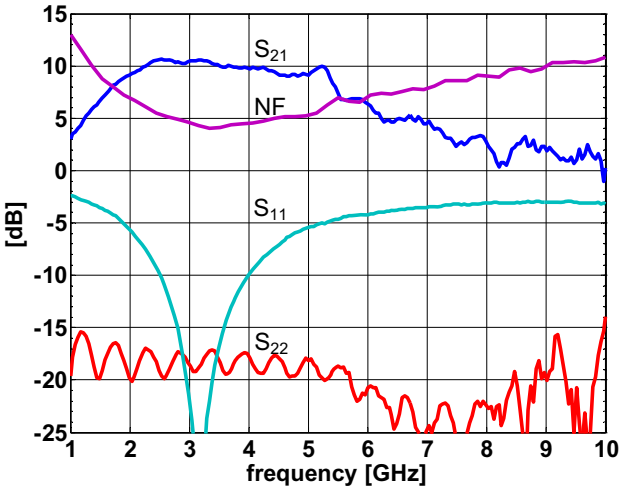

Fig. 5: Measured S-parameters and Noise Figure.

The voltage gain of the LNA is the relevant gain when it is followed by an integrated mixer with a voltage input. The S_{21} of 10 dB translates, in this case, into a voltage gain of 19 dB, due to the single-ended to differential nature of the LNA: to account for the matched output 6 dB needs to be added, and an additional 3 dB is required to take the conversion from 50 Ω input- to 100 Ω differential output-impedance into account.

Table 1 gives an overview of recently published wideband CMOS LNAs. Clearly, this design achieves the highest gain, consumes the least power and occupies the lowest chip-area. The NF is acceptable considering that the large voltage gain of the LNA will lead to minimal noise contributions of stages following the LNA. Next to this, a balun with its associated losses is also not needed.

V. CONCLUSION

Based on the Noise-Canceling Technique a new single-ended-input–differential-output LNA topology is presented, which exploits an on-chip transformer. The transformer is used to tune out the capacitance at the input, and realizes a passive, power-free, low-noise voltage gain. The resulting LNA achieves a high voltage gain of 19 dB, a broadband input match (2.5–4.0 GHz) and a Noise Figure of 4.0–5.4 dB at a core power consumption of 8mW. It is the smallest broadband LNA in the multi-GHz range published so far and it requires no external components.

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