Quadrature Sampling Mixer Topology for SAW-Less GPS Receivers in 0.18 μ m CMOS

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Abstract

This paper describes a new switching topology of a sampling mixer for SAW-less GPS (L1 band) receivers. The GPS receiver with the new mixer achieved NF 2.5dB and good blocking performance. In an alternative implementation, the mixer is stacked under a Quadrature VCO to reuse supply current. As a result, the current consumption of the GPS receiver is 11mA from 1.8V supply while maintaining blocking performance and NF of 3.5dB. Test chips are fabricated in 0.18 μ m CMOS process.

Introduction

Global positioning system (GPS) is one of the noticeable mobile applications and meanwhile GPS receivers are widely integrated in cellular phones. In a system like WCDMA, the transmitter (TX) and GPS receiver operate simultaneously. Due to limited isolation between TX and GPS receiver, a SAW filter is normally deployed to reject TX leakage, which degrades sensitivity and NF. However a SAW-less system is highly desired to save area and cost.

A 2*LO-LO topology is used to realize a 25% duty cycle [1], and has good performance for the RF front-end mixer [2]. In this paper we present a new switching topology for a quadrature sampling mixer(QSM) to realize the 25% duty cycle for application in a SAW-less GPS receiver. A QSM can have a filter function besides down-conversion [3]. Hence it is an attractive solution for SAW-less systems. This paper describes two test chips, which are Type I and Type II. The details of them are mentioned in later section.

The GPS signal coming from the satellite consists of two carriers, which are L1 band (1575.42MHz) and L2 band (1227.6MHz). We designed the RF front end of a L1 GPS receiver, which carries C/A code. The receiver uses a Low-IF of 4.092MHz, and the LO frequency is 1571.328MHz

Circuit implementation for SAW-less GPS RF front end

A. The new switching topology of mixer

Fig.1 shows cascoded common-source inductor-degenerated LNA-topology to provide low noise input current for the sampling mixer. The new switching topology and its timing chart of LO signals are shown in Fig.2 and 3.

Fig.1 Low noise current-source for sampling mixer

Fig.2 The new switching topology of mixer

Fig. 3 Timing chart of LO signal to realize 25% duty cycle

Fig.2 consists of the low noise current source, load R, and switching part I and II. In switching part I, when LOIP and LOQN are simultaneously +1, the current flows into sampling capacitance C1. As a result, the overlap of I-Q LO signals realizes 25% duty cycle. The effective LO signals for mixer, which is represented by multiplied LOIX and LOQX, (where "X" can be either "P" or "N") are also shown in Fig.3.

In switching part I, LOIX drives two switches and LOQX drives only one switch. Hence switching part I has a mismatch between I and Q. To compensate this I-Q mismatch, switching part II, which is driven by opposite I-Q, is deployed, and the outputs of switching part II are connected to the outputs of switching part I. Please note that the width of the transistors of switching part I are now divided by two, to include switching part II, therefore the total gate size remains constant when adding part II. The switching part I and II don't need 2*LO signal. They relax the current consumptions of LO buffers compared to 2*LO-LO topology.

Fig.4 shows the first RF front end to verify the new sampling mixer (Type I). The LNA uses 4mA, and LO buffers for I and Q respectively use 3mA of current. The polyphase filter is used to check the I-Q mismatch of this architecture and IF Amp is used to suppress polyphase noise for total noise.

Fig.4 The block diagram of RF front end. (type I)

C. Low current consumption with Quadrature-VCO

In a second design (type II) the Quadrature-VCO is stacked on the mixer to reuse VCO current. Fig.5 shows the RF front end of type II. This architecture employs Quadrature VCO with the Back-Gate Coupling [4]. The virtual supply voltage for mixer and IF Amp is about $V_{DD}-V_{gs}$ because this LC-VCO needs only one transistor V_{gs} . To remove LO buffer current, Q-VCO outputs are directly connected to the switching part I and II.

Fig.6 shows the block diagram of the GPS receiver. After polyphase, a band pass filter (BPF) rejects an out of band signal. Finally the desired signal is tuned to a certain amplitude by variable gain amp (VGA) to convert analog to digital (ADC). The Q-VCO is fixed 1571.328MHz by PLL.

Fig.5 The mixer and IF Amp stacked Q-VCO (type II)

Fig.6 The block diagram of GPS receiver (type II).

Measurement Results

The test chips are fabricated in 0.18 μ m CMOS with a 1.8V supply voltage. The measurement results and other work [5] are summarized in TABLE I. The test chip of type I is to verify the new switching topology of the sampling mixer while type II includes the stacked Q-VCO. Fig.7 shows the NF changes with a WCDMA 1.7G TX band blocker. When the CW blocker power is -20dBm at RFIN, the NF degrades only 0.5dB from no blocker in both of type I and type II without SAW filter. In case of modulated blocker, the second order intermodulation, which generates at N1 in Fig.1, contaminates noise floor in band through the switching part and capacitance mismatch.

Hence blocking performance results for modulated blocker was 12dB worse than CW. But inductor load of LNA can reject this degradation by BPF of LC resonance. In type II, the RF front end, which includes LNA, mixer, IF Amp and Q-VCO, consumes only 6.5mA, and it achieves 11mA in full receiver.

TABLE I Summary of measured results

Parameter	Type I	Type II	[5]	unit
RF Frequency	1575.42			MHz
NF	2.5	3.5	2.0	dB
Blocker power @NF 0.5dB degradation	-20	-19	-17	dBm
Image Rejection Ratio	44.2	30.1	26.8	dB
Current (Full receiver)	11.0			mA
Technology	0.18 μ m CMOS

Fig.7 Measured degradation of NF versus blocker power at RFIN

Fig.8 Die photo of chip type II

Conclusion

We proposed the new switching topology of a sampling mixer. It achieved NF 2.5dB for an L1 band GPS receiver and good blocking performance without SAW filter (type I). Furthermore it can be stacked with a Q-VCO to reduce the current consumption and achieves 11mA from a 1.8V supply for the RF front end (type II) with 3.5dB NF and good blocking performance in 0.18 μ m CMOS process.

References

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