A Discrete-Time Mixing Receiver Architecture with Wideband Image and Harmonic Rejection for Software-Defined Radio

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***Abstract*— A discrete-time mixing architecture for software defined radio receivers is proposed. It exploits 8x RF voltage oversampling followed by charge domain weighting to achieve 40dB 3rd and 5th harmonic rejection without channel bandwidth limitations. Also noise folding is reduced by 3dB. A zero-IF downconverter chip in 65nm CMOS can receive RF signals up to 900MHz, with NF_{min}=12dB, IIP3=11dBm at <20mW power consumption including multi-phase clock generation.**

***Index Terms* - Software-Defined Radio, RF Sampling, Discrete-Time Mixing, Wideband, Harmonic Rejection**

I. INTRODUCTION

Recently several CMOS software-defined radio (SDR) demonstrators have been presented using mixers as the wideband downconverter [1-2]. Meanwhile, the feasibility of RF samplers as downconverter has also been demonstrated [3-4], allowing for more discrete-time (DT) and digital signal processing. The general architecture of a DT receiver is shown in Figure 1. A DT receiver may offer some advantages compared to a continuous-time (C-T) architecture in a deep submicron digital CMOS process, e.g. due to the excellent component matching of capacitors [9] and the programmability to account for spread in process, voltage and temperature (PVT) and imperfections in simulation models [10], as well as the good compatibility to CMOS downscaling.

However, samplers suffer from several problems if applied in a wideband SDR. Charge sampling [3] gives a conversion gain which is inversely proportional to frequency [5]. Voltage sampling [4] doesn't have this problem, but suffers from wideband noise folding. In both cases, RF pre-filters are needed to prevent interferers around harmonics of the sampling clock from folding to baseband. This paper proposes a DT harmonic-rejection (HR) mixing architecture relaxing RF filter requirements and reducing the noise folding.

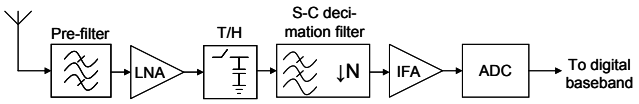

Figure 1. Analog part of a DT receiver

II. DT MIXING RECEIVER ARCHITECTURE

We aim for a SDR downconverter for the DVB-H standard (470-862MHz) and for emerging cognitive radio applications in the 200-900MHz band, suffering from 3rd and 5th harmonic mixing. Figure 2 shows the architecture of our IC. An inverter-based RF-amplifier (RFA) drives a passive switched-capacitor (SC) core consisting of three stages. The first stage is effectively an oversampler, with fs=8fc (fs: sampling frequency; fc: carrier frequency). The second stage consists of I/Q DT mixers for downconversion. The third stage is a low-pass IIR filter. The zero-IF quadrature outputs are buffered via source followers. A clock generator is implemented using a divide-by-4 circuit and NOR gates to generate 8-phase 12.5%-duty-cycle full-swing clocks to drive the sampling circuitry. An external sinusoidal differential master clock was used with a frequency of 4fc. Please note an LNA was not included in this design.

Figure 3 illustrates how the DT HR mixer works. Since the sampling rate is fs=8fc, the 7th harmonic folds to fc, and the 5th harmonic folds to 3fc, etc. Two DT I/Q mixers multiply the incoming samples with a DT cosine and sine wave, i.e. weighting factors of 1 and (1+√2) (cosine and sine with frequency fc sampled at 8fc). Since the DT clock is periodic, its spectrum only contains an impulse at fc. Multiplying the oversampled signal with the DT clock will convert down the signal from fc to DC without folding harmonics at 2fc, 3fc, and 4fc. However, the harmonics already folded to fc during the oversampling process cannot be differentiated from the wanted signal. These undistinguishable RF images are located at (k•n±1)fc (k=1,2,3…; n=fs/fc). If n=8, the un-suppressed RF images are the 7th, 9th, 15th, 17th etc, but the problematic 3rd and 5th harmonics are cancelled. The DT cosine and sine waves have a 90º phase difference, which transfers the phase of the RF input signal to IF in a similar way as a continuous-time mixer does. In contrast to the case with an approximation by a time delay [3-4], which is only exact for one frequency [5], the 90º phase shift by DT I/Q mixing is frequency independent leading to a true wideband image rejection. Furthermore, the HR mixing also suppresses noise around harmonics, and hence reduces noise folding. In simulation, a 3dB NF improvement is observed, which makes sense since half of the odd-order harmonic noise folding is suppressed.

Figure 4 shows the SC core circuitry. For clarity only half of the fully differential system is shown. Eight interleaved sampling cells are controlled by 8-phase non-overlapping clocks, with CLKin for the sampling function and CLKout for the mixing function. Each of the 8-phase clocks has a sampling rate of fc, and altogether an effective sample rate of 8fc is achieved. In each sampling cell, there are two weighted sampling capacitors. To make an non-integer 1:(1+√2) ratio reliably in layout is difficult. We used unit capacitor Csu in a 2:5 ratio as approximation, which is theoretically sufficient for 35dB 3rd and 5th order HR assuming 1º phase error. Second

order effects such as charge sharing and gain roll-off can give several dBs extra. Although 5:12 would be more accurate, gain errors still don't dominate over the phase errors originating from clock timing mismatches. The DT mixing function is implemented via a systematic combination of the output switches, to transfer charges from sampling capacitors to buffer capacitors (Cb). The charge sharing between the sampling and buffer capacitors implements a low-pass IIR filter [3]. The outputs can be decimated, e.g. via a moving average [3], to a lower sample rate and the next stages can use further DT signal processing as done in [3].

Figure 8 shows the micrograph of the chip fabricated in a 65nm CMOS process. The active area of the chip occupies 0.36mm2. Figure 5 shows the measured gain and noise figure over the RF band. At the low side, AC coupling limits the gain and at the high end the clock circuitry speed limit of 3.6GHz is reached. Due to the varying gain, the SSB NF ranges from 12dB to 19dB, which is 20dB better than [4] and is the lowest among all voltage sampling mixers discussed in [6].

In literature, a continuous-time HR mixer for transmitters has been proposed in [7], and a 2MHz IF HR sampler in [8], both using weighted amplifiers. We exploit weighted capacitors which can have superior matching properties, and only need one RF amplifier, while still generating quadrature IF signals. The same number of clock phases is needed for our architecture and [7,8], so there is no extra cost on clock speed.

A good HR ratio over a wide channel BW is important for wideband standards and for future cognitive radio applications which might use multiple segments of free spectrum spread over a wide band. It is also important to reduce distortion caused by strong out-of-channel interferes. In [8], the IF HR sampler was implemented by summing up the sampled data. This operation is equivalent to using a FIR filter to reject harmonics, which is only effective for a limited channel BW due to the limited notch BW intrinsic in any FIR filters. DT mixing does not have this limitation. In Figure 6, the upper plot shows the HR ratio for a sampler using FIR filter drops significantly over the channel, while our architecture gives wideband HR without channel BW limitation. The trend of measured results meets well with the simulated results. However, phase and gain mismatches limit the achievable HR ratio (not considered in both simulation results).

The lower plot in Figure 6 shows the measured results for the HR ratio over the RF band, averaged over 10 chips (σ=5dB). On average, the 3rd order from 0.5-0.8G and the 5th order from 0.3-0.9G reach around 40dB HR ratio, comparable to the state-of-the-art continuous time HR mixer for RF receivers reported at only one frequency [1].

Figure 7 summarizes the measured parameters. The noise and linearity performance is competitive with continuous-time mixers at reasonable power consumption. This shows the feasibility of our architecture for a practical receiver front-end.

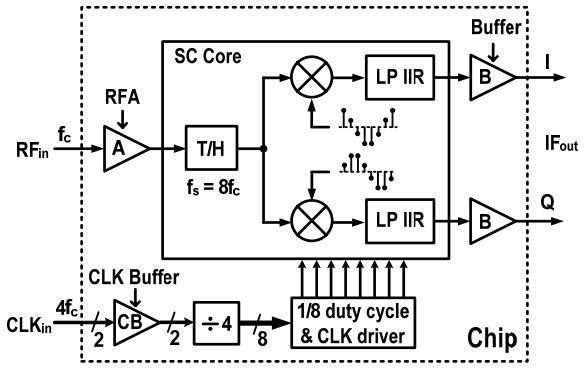

Figure 2. Architecture of the harmonic-rejection (HR) sampling downconverter IC using the discrete-time (DT) mixing technique. All blocks are implemented on chip.

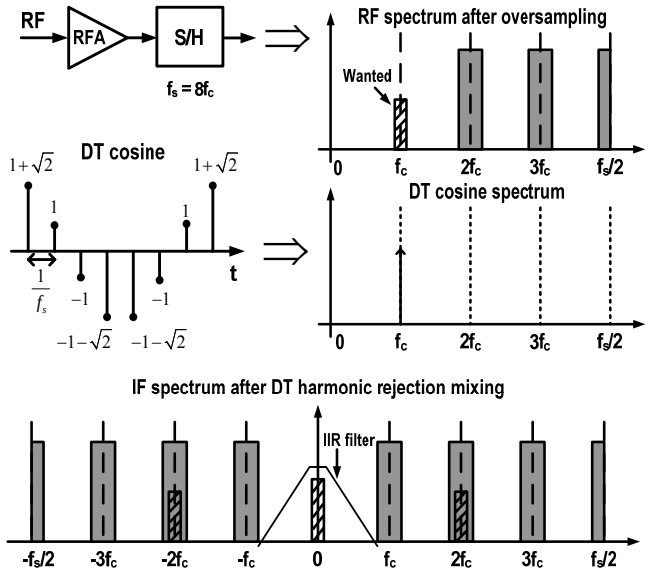

Figure 3. Illustration of the discrete-time (DT) harmonic-rejection mixing mechanism.

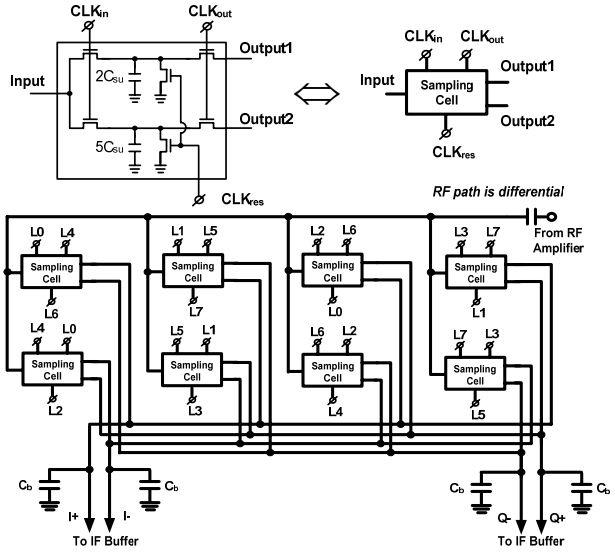

Figure 4. Switched-capacitor (SC) core circuitry of the harmonic-rejection sampling downconverter, with the clock scheme L0-L7 shown in Figure 2.

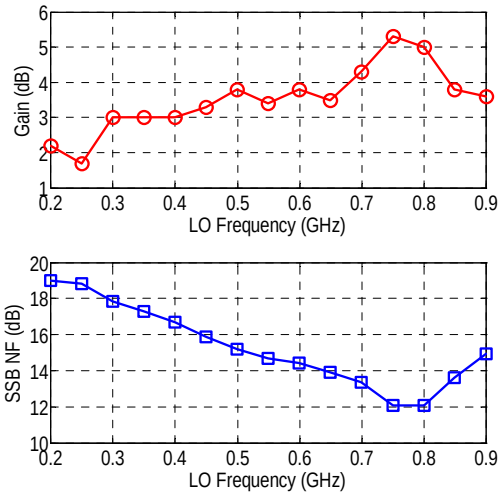

Figure 5. Gain and noise figure over the RF band. Both gain and noise data are measured at 1MHz IF.

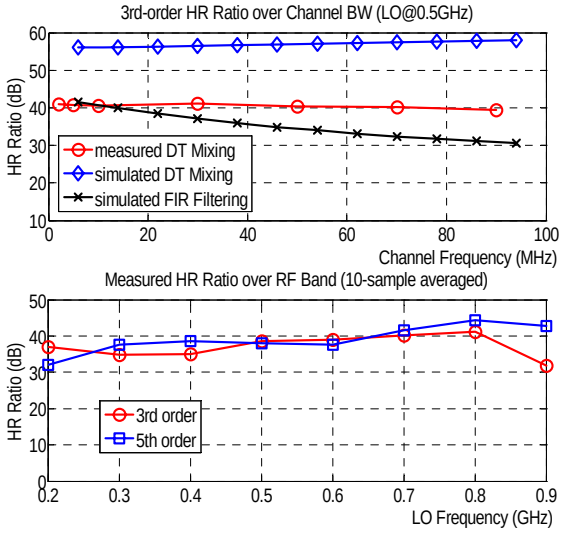

Figure 6. Harmonic rejection (HR) ratio over channel and RF band.

Frequency Range (GHz)	0.2-0.9
Gain (dB) @ 1MHz IF	Min: 1.7 Max: 5.3
SSB NF (dB) @ 1MHz IF	Min: 12 Max: 19
IIP3 (503M & 504M)	+11dBm
IIP2 (503M & 504M)	+43dBm
1/f noise corner	250KHz
IF bandwidth @ 700MHz LO	10MHz

VDD	1.2 V
Current consumption (mA)	RFA & Buffer: 5.3
	Clock generator: 7.8@0.2GHz LO 10.6@0.9GHz LO
Power	< 20 mW

Harmonic rejection ratio (10-sample averaged,σ=5dB)	
3rd-order (LO: 0.2-0.9G)	Min: 32dB Max: 41dB
5th-order (LO: 0.2-0.9G)	Min: 32dB Max: 44dB

Figure 7. Measured key parameters.

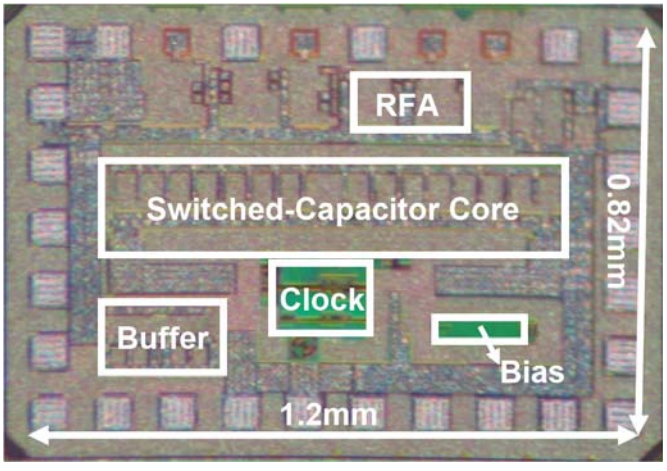

Figure 8. Micrograph of the chip fabricated in 65nm CMOS. The 0.36mm2 active area includes all the blocks shown in Figure 2 and the bias current sources.

III. Conclusion

This paper presents the first wideband receiver based on sampling downconversion [11]. We proposed a DT mixing architecture for sampling receivers to achieve wideband image rejection and wideband harmonic rejection, i.e. wideband interference rejection. This architecture exploits the true phase-shift property of mixers, solving the narrowband property in traditional sampling receivers due to the use of delay to approximate phase shift. Applying harmonic rejection to voltage sampling also improves its noise figure. Using DT mixing architecture, RF sampling for software-defined radio receiver becomes feasible.

Acknowledgment

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