A CMOS compatible process for improved RF performance on highly doped substrates

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Abstract

In this paper we present a CMOS compatible process for CMOS-grade wafers in order to create specific areas where radio frequency (RF) devices can be implemented without the high losses associated to this substrate. The process is based on refilling of deep trenches, which allows the local replacement of the silicon substrate by silicon nitride, which has very good RF properties (tan δ = 5-9 10^{-4}). The trenches are in the order of 30 μm deep and 2 μm wide, leaving a space of 2 μm in between where the silicon still remains. In this way, half of the lossy substrate is replaced by silicon nitride. We will present measurement results which indicate that the RF performance of CMOS-grade wafers can be significantly improved, as well as a careful study of the most relevant fabrication parameters and the consequences for the final RF performance of the substrate. An additional advantage of this new technique is the possibility of using it as a pre-CMOS process, thus allowing monolithic integration of CMOS electronics and RF and microwave components.

Introduction

The enormous growth of wireless and portable applications has led to strong demands for high-performance monolithic low-cost passive components in RF and microwave integrated circuits (ICs). However, some traditional microwave passive components like transmission lines and filters are difficult to integrate on the same chip with the RF and microwave circuits due to the high substrate losses associated with standard low-resistivity CMOS-grade silicon substrates. As a result, most RF and microwave components are realized on special substrates like AF45 glass [1, 2] or quartz [3]. Because of the strong need for monolithic integration with electronics, several techniques have been developed to allow the realization of low loss RF devices on standard silicon. These techniques include the use of dielectric layers like polyimide [4] and benzocyclobutene [5], the use of polysilicon patterned ground shields [6], the use of silicon bulk-micromachining to remove the substrate locally under the RF components [7-9], and the use of surface-micromachined suspended metal structures at a distance of several tens of micrometers above the silicon surface [10, 11]. However, all these techniques impose restrictions on the device structures that can be realized. The best results are obtained with the freely suspended structures [7-11], but such free hanging structures are rather delicate, vulnerable to shocks and vibration and difficult to package. Most recently, we proposed a novel technique where the silicon substrate is locally replaced by a thick block of silicon nitride below the transmission line [12]. Here we present a simplified approach, where not the whole top part of the substrate is replaced by silicon nitride, but only half of it, using refilling of deep and thin trenches. In this way, almost half of the fabrication steps are avoided, making this approach significantly easier and cheaper (see Fig. 1).

Measurements on a coplanar waveguide (CPW) on top of these structures have shown that the RF performance of the substrate increases significantly. Although better results can be obtained when a complete silicon nitride block is created (where almost performances as good as for dedicated glass wafers can be achieved [12]), optimization of this new technique by increasing the width of the trenches or tuning their orientation with respect to the transmission line, have shown important improvements.

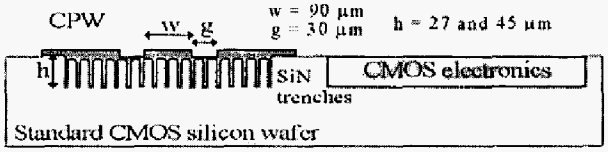


Fig. 1: Cross section of a standard CMOS silicon wafer with silicon nitride trenches for monolithic integration of a coplanar waveguide (CPW) and CMOS electronics.

Fabrication

Silicon nitride layers are usually grown by low-pressure chemical vapor deposition (LPCVD). However, the maximum achievable layer thickness is in the order of 2 micrometers, which is too thin for use as intermediate layer between RF components and the silicon substrate. We developed a fabrication process based on refilling of deep trenches, which allows the creation of trenches refilled with silicon nitride in highly doped, standard silicon wafers. The process was successfully tested on <100> highly p-doped silicon wafers. Fig. 2 shows a summary of the fabrication process.

The process starts with the deposition of a thin layer of silicon nitride (100 nm). This layer is patterned creating a large number of parallel rectangles. The length of the rectangles defines the length of the resulting silicon nitride columns. The width and spacing between the rectangles are of the order of 2 μm. Next, deep trenches are created by anisotropic etching of the silicon substrate using deep reactive ion etching (DRIE). Then, the silicon nitride layer, which acted as a mask, is removed and a new silicon nitride layer is deposited. Due to the excellent conformal step coverage during LPCVD deposition, the trenches are completely filled by a deposition of 1 μm of silicon nitride. Low-stress, silicon-rich silicon nitride (SiRN) is chosen in order to minimize curvature of the silicon wafer due to residual tensile stress. Then, a 1 μm thick aluminum layer was deposited by sputtering and patterned in order to build a 630 μm long CPW which will be used for characterizing the RF properties of the

treated substrate. Dimensions of the CPW are shown on Fig. 1.

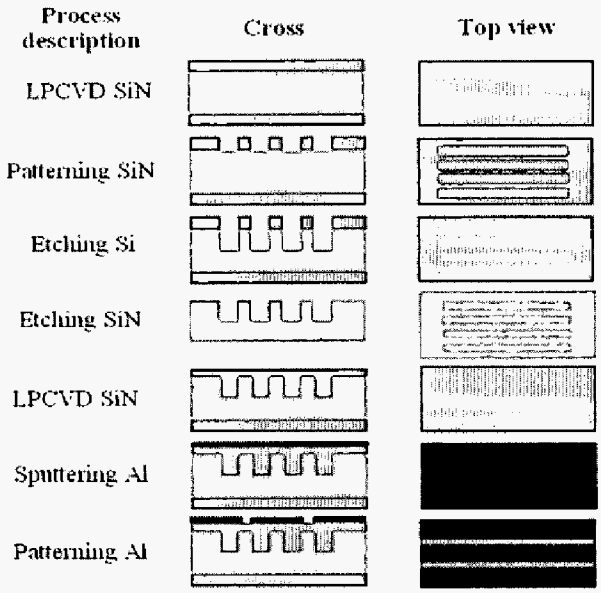
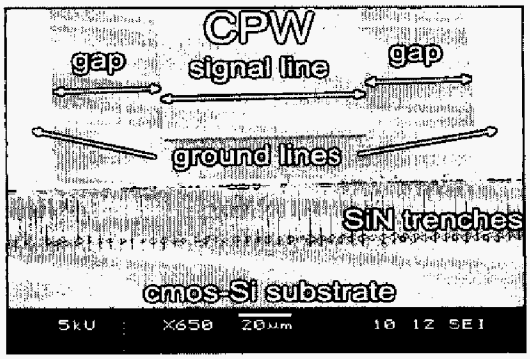


Fig 2: Fabrication process scheme for silicon nitride columns embedded in standard silicon substrates.

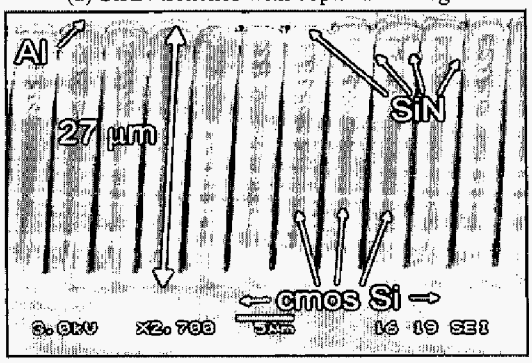
Fig. 3 shows SEM pictures of a cross section of a typical fabrication result. As we can clearly see on the close-up, the trenches are in this case 27 µm deep, resulting into columns of 2.5 µm wide silicon nitride and 1.5 µm wide silicon. From the picture we can see that the etching of the silicon by DRIE gave a slightly negative profile, since the trenches are wider at the bottom than at the top. This resulted in vacuum cavities at the bottom of the trenches, since the top level was closed by silicon nitride first, blocking the deposition for the rest of the trench. Nevertheless, no negative effects are expected from this on the mechanical and RF performance.

By tuning the parameters in the etching of the silicon and the deposition of the silicon nitride, different depths and widths can be achieved. In order to compare its effect, two different depths, 27 µm and 45 µm, and two different widths of the silicon nitride columns, 2.5 µm (resulting on 1.5 µm wide silicon columns) and 1.8 µm (resulting on 2.2 µm wide silicon columns) were fabricated.

Another free parameter during the fabrication is the orientation of the trenches with respect to the transmission line. To study its influence, two different orientations were made, parallel and perpendicular (0 and 90 degrees with respect to the transmission line respectively).



(a) SiRN trenches with coplanar waveguide.



(b) Close-up of refilled trenches.

Fig 3: SEM pictures showing the cross section of a 30 µm deep silicon nitride columns on highly doped silicon wafer

Measurements

In order to characterize the RF performance of the CMOS grade silicon wafer treated by this new technique, on-wafer S-parameter measurements were performed in a frequency range up to 50 GHz with an HP 8510C network analyzer. To obtain a quick overview of the CPWs' properties, we used a commercially available implementation of the LRM+ calibration technique, which can be considered superior to standard techniques like e.g. the short-open-load-thru (SOLT) calibration. Recently, LRM+ has shown promising results on silicon in a broad frequency range[13].

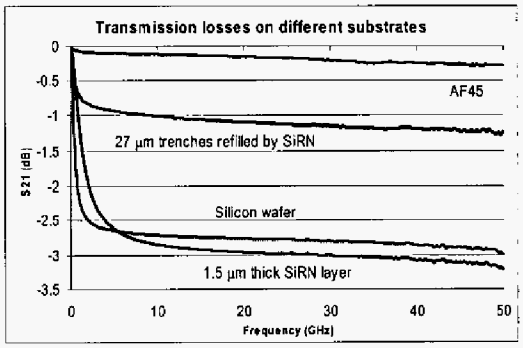


Fig 4: Measured transmission losses (S_{21}) in dB, as a function of frequency for CPWs on standard CMOS-grade silicon wafers, wafers with 1.5 µm silicon nitride, with 27 µm deep silicon nitride trenches, and AF45 glass substrates.

Fig. 4 shows the results obtained by a silicon wafer treated with 27 μm deep trenches refilled by silicon nitride together with the results for a CPW directly on silicon, on silicon with a 1.5 μm thick SiRN layer deposited on top and on low-loss AF45 glass (dedicated substrate for RF circuits).

As can be observed from the graph, losses in the order of 3 dB are measured for the silicon wafer, and similar results are obtained by depositing 1.5 μm thick silicon nitride layer on top silicon substrate. Much lower losses are obtained with a silicon wafer after the trench refilling process, with a gain of almost 2 dB. In this case, trenches are 27 μm deep and 2.5 μm wide, resulting in 1.5 μm wide silicon columns in between. Although further study is necessary in order to reach as good results as dedicated glass substrates, very promising results are shown.

Losses dependence as a function of the depth of the silicon nitride trenches were studied by comparing two different thicknesses. Fig. 5 shows results from two different substrates after the fabrication of silicon nitride columns with identical orientation (parallel to the CPW) and width (resulting on 2.5 μm for silicon nitride and 1.5 μm for silicon), but difference depths (27 μm and 45 μm). There is only a slight difference between the two substrates, therefore it may not be necessary to make very deep trenches. Most losses seem to occur close to the surface of the wafer.

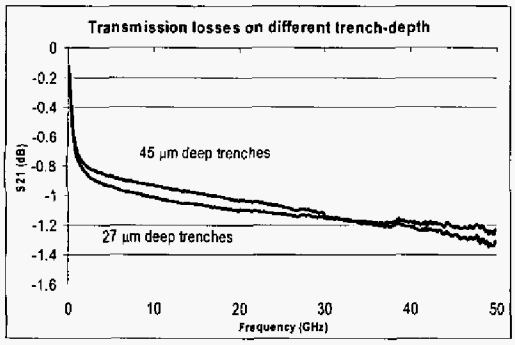


Fig 5: Measured transmission losses (S_{21}) in dB, as a function of frequency for CPWs on standard CMOS silicon wafers with 27 μm and 45 μm deep silicon nitride trenches.

In Fig. 6 two substrates with trenches with very similar depth (27 and 28 μm) and the same orientation (parallel to the CPW), but different trench width are compared. The difference in the trench width resulted in 2.5 μm for silicon nitride and 1.5 μm for silicon in one case, and 1.8 μm for silicon nitride and 2.2 μm for silicon in the other.

From Fig. 6 we can see a strong dependence between the relative amount of silicon left below the transmission line and the transmission losses. Therefore, further study and fabrication effort are required in this direction in order to optimize the RF properties of the substrate.

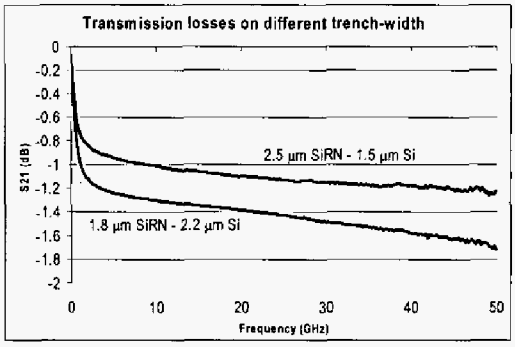


Fig 6: Measured transmission losses (S_{21}) in dB, as a function of frequency for CPWs on standard CMOS silicon wafers with two different relative amount of silicon left.

Another important aspect which requires a careful analysis is the orientation of the silicon nitride trenches with respect to the transmission line. Although similar RF properties could be expected since there is the same amount of silicon under the transmission line, measurements done with two different relative orientations (parallel and perpendicular) lead us to the conclusion that the losses depend heavily on the orientation. The corresponding results are presented in Fig. 7, where 0.4 dB less losses can be observed in the case where the trenches are parallel to the transmission line. The SEM picture of the substrate with parallel trenches was shown on Fig. 3, and the SEM picture of the substrate with perpendicular trenches is shown on Fig. 8.

This difference in the transmission losses due to the orientation can be explained by looking at the direction of the electric field. When trenches are perpendicular to the CPW, there are paths where electric field only travels through the conducting silicon, ending with high transmission losses. But when trenches are parallel to the transmission line, the electric field has to cross alternatively silicon and silicon nitride (which is an isolating material). Therefore, electrically-induced current losses are significantly reduced.

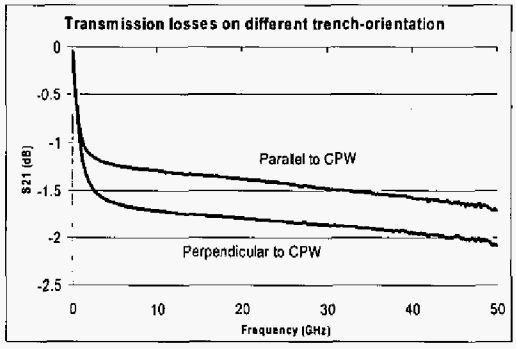


Fig 7: Measured transmission losses (S_{21}) in dB, as a function of frequency for CPWs on standard CMOS silicon wafers with parallel and perpendicular silicon nitride trenches.

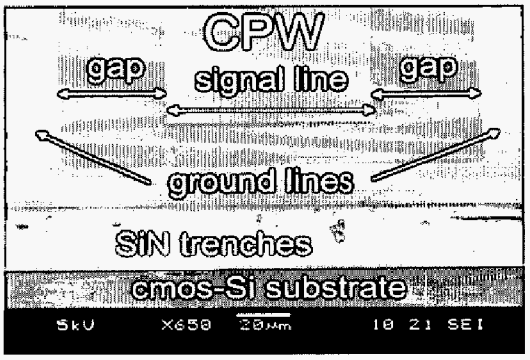


Fig 8: SEM pictures showing the cross section of perpendicular silicon nitride columns.

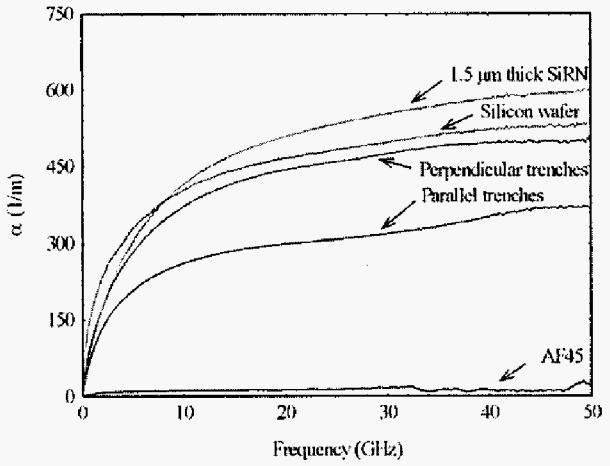


Fig 9: Attenuation constant (α) in 1/m, as a function of frequency for various CPWs.

As a first result of a more detailed study, Fig. 9 shows the attenuation constant α as measured for some of the CPWs discussed previously. α was calculated as the real part of the propagation constant γ, which was measured with a Multiline-TRL calibration [14] on CPWs of different lengths. The curves in Fig. 9 confirm the results obtained as measurements of the transmission losses for the single length of 630 µm (see Figs. 4-7). Current investigations are concerned with a full characterization of the various test structures, including the extraction of the frequency-dependent characteristic impedance. This will eventually lead to a better understanding of the substrate loss mechanisms in the different silicon nitride fabrication alternatives discussed.

Conclusions

In summary, we have presented a fabrication process, which allows fabrication of deep silicon nitride columns in standard silicon wafers. Measurements on coplanar waveguides have demonstrated the improvement of RF properties on CMOS-grade silicon wafers where the substrate has been treated by this technique. Very promising results have been shown by studying different fabrication parameters and the effects on the final RF performance. Further fabrication development focused on minimizing the amount of silicon left could lead us close to the low transmission losses reported from complete silicon nitride blocks [12]. Using the process as pre-CMOS process allows the monolithic integration of high-performance RF and microwave devices with CMOS electronics.

Acknowledgments

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