Advances in Silicon Phased-Array Receiver IC's

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Abstract — **Phased-Arrays are increasingly used, and require Silicon implementations to result in affordable multi-beam systems. In this paper, CMOS implementations of two novel analogue beamforming multi-channel receivers will be presented. A narrow-band highly linear system exploiting switches and capacitors in advanced CMOS is presented, implementing a fully passive switched capacitor vector modulator exploiting a zero-IF I/Q mixer. This technique is not applicable to very wideband phased-array receivers. These systems require true-time delay beamforming, which is implemented in the second CMOS implementation. An innovative gm-RC implementation of a true-time delay cell is exploited in a four-channel beamforming receiver with more than 1.5 GHz bandwidth, in a standard 0.13 um CMOS process. Professional phased-arrays can often not live with the dynamic range limitations imposed by these implementations. To that end a SiGe implementation of an integrated receiver was realized targeting a digital beamforming phased-array. Dynamic range and flexibility of use were the main driving factors. Alltogether, these results show large progress with respect to the feasibility of Silicon-based phased-array front-end implementation for commercial as well as professional phased-arrays.**

Index Terms — **Phased-Array, beamforming, integrated receiver, CMOS, BiCMOS.**

I. INTRODUCTION

Phased-arrays are becoming omnipresent. With initial developments in science (astronomy) and defence (radar), the development of low-cost microwave technologies has opened the use for a multitude of applications. Different beamforming schemes are used. In the early days, free-space beamformers with ferrite phase-shifters were used [1]. For current sub-THz power generation systems, this technique is *en vogue* again, and their building blocks are being demonstrated [2]. Analogue, RF, phase-shifter based beamformers have been the workhorse for Active Electronically Scanned Arrays, as often found in a military context. These systems have relied for more than 20 years on advanced III-V MMIC's, where the current state-of-art is a two-chip solution with a core chip and a high power amplifier, both in different flavours of GaAs or GaN [3,4]. Wide-band systems, such as astronomical arrays or electronic warfare receivers cannot live with this narrow-band approximation of a time-delay by a phase-shifter and resort to true time-delays for their anaalogue, RF beamformers. Finally, there is a major trend in the direction of digital beamforming. Unattractive as this may be from the perspective of power consumption and local oscillator distribution network

requirements, the flexibility it presents is found to be a driving force in beamforming technology.

In this paper, advances in the different domains are presented in perspective. First, a 65 nm CMOS receiver IC is presented that is particularly useful for narrow band communication systems. Secondly, a 0.13 um CMOS IC aimed at very wideband systems is presented, that integrates very much time delay on a tiny surface. Finally, a 0.35 um BiCMOS receiver IC is described that is particularly useful for professional digital-beamforming applications and performs exceptionally well in terms of dynamic range.

II. BEAMFORMING-RECEIVER IMPLEMENTATIONS
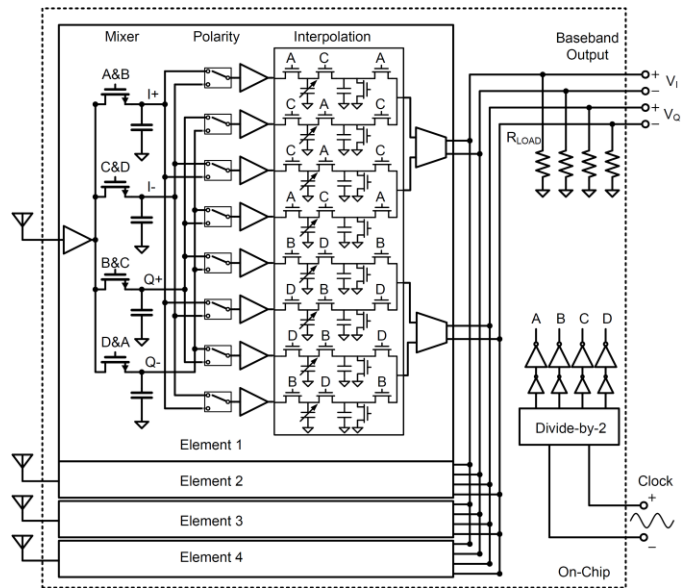
A. Narrow-Band Beamforming Receiver

Figure 1 Four-element zero-IF receiver architecture.

In a narrowband communication standard, the time delay for beamforming can be approximated by a phase shift in a narrow frequency band. A straight-forward design approach that uses classical filter design to build the correct phase response is usually unsuitable for integrated systems, due to the poor integration of on-chip coils and limited operating frequency of active filters. Instead, it is more useful to explore alternative ways of producing a phase shift. With CMOS technology

being optimized for digital processing, which takes place in the discrete-time domain, there is a lot to gain in implementing discrete-time phase shifters.

A 4-element phased array receiver front end, shown schematically in Figure 1, was implemented in 65nm LP CMOS, utilizing a switched-capacitor vector modulator [5]. Each element is input matched over a wide RF bandwidth with a common-gate input stage. Downconversion takes place with a zero-IF image-reject 25% duty cycle passive mixer, making available differential In-phase and Quadrature baseband signals. Interpolation takes place between the I and Q signals with a tunable switched capacitor network, effectively forming a vector modulator phase shifter. Polarity switches are present to access the full 360 degrees of phase shift.

The vector modulator output voltages are then converted to current with a transconductance stage and summed in the current domain, by flowing into the common load resistors R_{load} to provide the baseband output voltages. The clock for the mixer and vector modulator is provided by dividing a differential off-chip master clock by two to generate a 4-phase 50% duty cycle LO.

In the limited voltage supply that is available in advanced CMOS, switched-capacitor circuits can tolerate larger signal voltage swings than their transconductance counterparts. This expresses itself in high linearity figures for this front end. Moreover, the phase shift in the proposed vector modulator only depends on capacitor ratios, which are accurately controlled in the process technology.

The realized implementation occupies an active area of $0.44mm^2$ with 5 bit phase control in the vector modulator and achieves an rms systematic phase and gain error of 1.4 degrees and 0.4dB respectively. Applications in crowded frequency bands, like the 2.4 GHz ISM band are enabled by the high -1 dBm IIP3. Moreover, a spatial interference rejection >20dB through pattern nulling was demonstrated, to further lower the linearity requirements on the baseband receiver part.

B. Wide-Band Beamforming Receiver

Integrated time-delay cells have been proposed based on the approximation of transmission line segments with integrated LC lumped elements [6]. These, however, require bulky on-chip inductors. A gm-RC or gm-C all-pass delay circuit [7,8] can produce a given amount of delay in a much smaller area.

Recently an improved gm-C delay cell [9] was proposed that realizes an accurate integrated time-delay over a wide (1-2.5GHz) frequency band, at an acceptable power dissipation. Features of this time-delay cell include an accurately adjustable delay, low delay variation versus frequency and an accurately controllable unity gain. The DC-coupled nature allows for cascading cells without DC-blocking capacitors. The circuit works down to low supply voltages and exploits current re-use to limit dissipation. Comparison to [7,8] in the same technology shows a better delay approximation over a wider bandwidth, especially because floating capacitors are avoided, removing the most significant parasitic poles. The remaining parasitic pole at the output was shifted up by inductive peaking via active inductors.

With these wideband time delay cells, a 4-element phased array receiver front-end as shown in Figure 2 was designed in 0.14 μm CMOS. The four received signals are first amplified by an LNA with differential output, which takes care of a broadband 50Ω matching to reduce mutual coupling between adjacent antenna elements. The LNA is followed by a delay chain which is subdivided in fine and coarse delay cells, of which several are cascaded. The desired delay in path i is coarsely selected via control signals $C_{i,0}..C_{i,4}$, which actives one particular V-I converter. The delay is then adjusted by setting the delay of the fine-control bits. The output signals of the four active V-I converters (one per channel) can now be added in the current domain, in which the effective beamforming takes place. The summed signals are down-converted in a mixer.
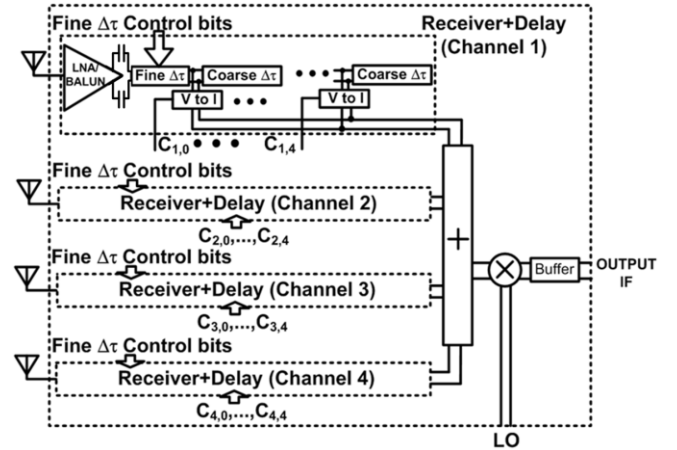

Figure 2: Block diagram of the 4-channel IC

The main feature of the realized RFIC, its time-delay, was characterized over all coarse and fine delay setting combinations over a wide frequency range. For a bandwidth of more than 1.5 GHz (1-2.5 GHz), the delay variation is less than 10 psec. Note that this is achieved without calibration. At the same time, the gain variation is as low as <0.4dB.

Compared to other designs, the occupied area is an order of magnitude smaller than results from literature, whilst the integrated delay is significantly larger [9]. The same holds for the delay flatness. This flatness is comparable to the resolution, but for more delay and at a lower frequency. Gain-variation is also better. Note that these results are obtained without calibration. Delay steps are uniform and monotonously increasing, which facilitates easy control and avoids intricate lookup tables and calibration schemes.

C. Digital Beamforming Receiver

A Silicon-Germanium single chip receiver has been developed by Thales Netherlands and TNO for S-band phased

array radars with 2-D digital beamforming, using several 1000 receivers per system. Such a system with 4 antenna faces is currently built for the RNLN Offshore Patrol Vessels.

The complete receiver chain from the S-band RF input up to the low-IF output has been integrated on a single SiGe chip, together with a digital control circuit, which allows full control of all receiver settings via a simple serial control interface [10]. The low-IF output can directly drive modern high speed ADCs with a high fidelity differential signal. For radar applications strict requirements apply with regard to selectivity, which can't be realized on chip. Therefore the receiver chip is operated with two external high-Q IF filters.

The receiver chip has been realized in the 0.35μm SiGe BiCMOS process of Austria MicroSystems (AMS), in two iterations. The chip is packaged in a 9x9 mm QFN-64 package. The integration of the receiver functionality on a single chip provides several important advantages for the application in a phased array with one receiver per antenna element and 2-D DBF:

- Lower component count and relief of space constraints that are encountered in the design;
- Space is created to place the ADC adjacent to the receiver chip, contributing to the EMI resistance of the receiver.
- Better amplitude and phase matching within the instantaneous and more repeatable receiver performance than with a discrete implementation.

The receiver chip architecture is shown in figure 3. It is a super heterodyne receiver which can be split into four main parts: the S-band down converter (SDC) on the left, the first IF amplification block (IFB) in the middle, the IF processing block (IFP) with second down conversion, amplification, limiting, filtering and ADC driver on the right and the digital control circuitry (DCC) with serial interface on the bottom side.
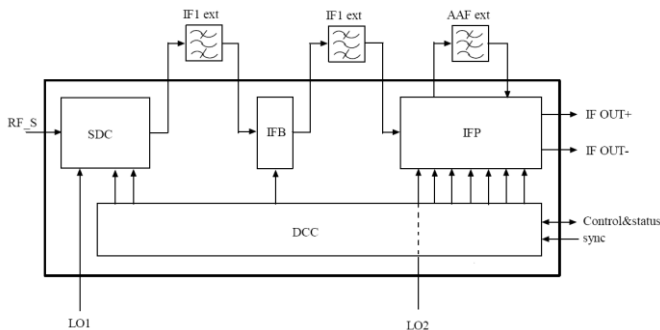

Figure 3: Receiver chip architecture

The SDC block consists of a two stage Low Noise Amplifier (LNA), an image reject filter and a Gilbert-cell mixer. The LNA is combined with a balun to convert from single-ended to differential. The receiver chip is designed completely differential except for the S-band RF input and both LO inputs. The remaining IF interfaces are all differential. One important reason for making the design differential is due to the high receiver integration level in combination with the high on-chip

gain which is required to amplify the weak incoming RF signals to ADC input levels. This puts a high demand on the isolation between building blocks especially around the IF filtering.

To reduce off-chip components as much as possible, an active anti-alias low-pass filter is integrated in the IFP block [11]. The anti-alias filter consists of three sections to have sufficient suppression at higher frequencies. If another filter characteristic is required it is still possible to select an external anti-alias filter via the serial interface.

III. CONCLUSION

Three very different state-of-art integrated phased-array receivers have been described. Depending on the application, RF phase-delay based, time-delay based and digital beamforming will continue to find their place in real systems. The technology and designs continue to develop at a very high pace.

REFERENCES

[1] D. Parker, D.C. Zimmerman, "Phased arrays - part II: implementations, applications and future trends" IEEE Trans. Microwave Theory & Tech., 50th anniversary issue, March 2002.

[2] O. Inac, B. Cetinoneri, M. Uzunko, Y. A. Atesal, and G. M. Rebeiz, "Millimeter-Wave and THz Circuits in 45-nm SOI CMOS" 2011 IEEE Comp.Semic. IC Symp. Dig., October 2011.

[3] F.E. van Vliet, A. de Boer, "Fully-Integrated Core chip for XBand Phased-Array T/R modules." In: IEEE Microwave Theory and Techniques Symposium (MTT-S) Digest, 6-11 June 2004, Fort Worth, TX, USA, pp. 1753-1756.

[4] G. van der Bent, A.P. de Hek, A. Bessemoulin and F.E. van Vliet, "Low-Cost High-Efficient 10-Watt High-Power Amplifier, COMCAS2009, 9-11 november 2009, Tel Aviv,Israel

[5] M.C.M. Soer, E.A.M. Klumperink, B. Nauta, F.E. van Vliet, "Spatial Interferer Rejection in a Four-Element Beamforming Receiver Front-End with a Switched-Capacitor Vector Modulator", IEEE Journal of Solid-State Circuits, vol. 46, pp. 2933-2942, dec. 2012.

[6] Ta-Shun Chu.et.al, "A 4-Channel UWB Beam-Former in 0.13μm CMOS using a Path-Sharing True-Time-Delay Architecture", IEEE J Solid State Circuits, pp.2834 –2850, 2007.

[7] J. Buckwalter, A. Hajimiri, "An active analog delay and the delay reference loop", RFIC Dig Tech, pp:17-20,2004

[8] P. Horowitz, "The art of electronics", Cambridge University press, 1989

[9] S.K. Garakoui, E.A.M. Klumperink, B. Nauta, F.E. van Vliet, "A 1-2.5 GHz Phased Array IC based on gm-RC All-Pass Time Delay Cells", ISSCC Dig. Tech. Papers, pp. 80-81, Feb. 2012.

[10] W. de Heij, A. de Boer, A.P. de Hek, F.E. van Vliet, "A Silicon- Germanium Single Chip Receiver for S-Band Phased Array Radars,", EuRAD 2011, Manchester, September 2011.

[11] Stefano D' Amico, Matteo Conta, Andrea Baschirotto, A 4.1-mW 10-MHz Fourth-Order Source-Follower-Based Continuous-Time Filter With 79-dB DR, IEEE Journal of Solid-State Circuits, vol. 41, December 2006.