Dependable Digitally-Assisted Mixed-Signal IPs Based on Integrated Self-Test & Self-Calibration

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Abstract

Heterogeneous SoC devices, including sensors, analogue and mixed-signal front-end circuits and the availability of massive digital processing capability, are being increasingly used in safety-critical applications like in the automotive, medical, and the security arena. Already a significant amount of attention has been paid in literature with respect to the dependability of the digital parts in heterogeneous SoCs. This is in contrast to especially the sensors and front-end mixed-signal electronics; these are however particular sensitive to external influences over time and hence determining their dependability. This paper provides an integrated SoC / IP approach to enhance the dependability. It will give an example of a digitally-assisted mixed-signal front-end IP which is being evaluated under its mission profile of an automotive tyre pressure monitoring system. It will be shown how internal monitoring and digitally-controlled adaptation by using embedded processors can help in terms of improving the dependability of this mixed-signal part under harsh conditions for a long time.

Keywords: dependability, availability, reliability, safety, self-test, self-calibration, self-repair, aging, mixed-signal testing

1 Introduction

Mixed-signal and analogue cores in heterogeneous SoCs are increasingly required to operate for a long time in a highly dependable manner[1] despite harsh environmental conditions. This is a result of the increasing wide application of these SoCs in safety-critical systems, like in medical, automotive and security applications [1]. Dependability has several attributes which have to be included in our designs, like *reliability*, *maintainability, availability* and *safety* [2 - 4].

The vast digital parts in these heterogeneous SoCs nowadays, like embedded (multi)processors, have already received quite some attention with regard to dependability [5, 6]. However, the dependability of the front- and back-end mixed-signal (MS) / analogue cores and sensors / actuators is rarely discussed. As an example, Figure 1 shows a typical set-up of a sensor, e.g. for temperature, and its front-end analogue / MS electronics. As the improvement of the performance of analogue as well as mixed-signal circuits is increasingly accomplished by digital means [7], it will be assumed in this paper that the front-end blocks have digital programming capabilities, for instance programmable gain, in combination with the usage of (an) embedded processor(s) for control (Figure 1, double arrows).

The dependability issues hold most for sensors & actuators, because of their required (direct) interaction with the environment; but also the front- and back-end electronics are of interest because of their higher susceptibility to parameter changes in comparison with digital circuits. Furthermore, sensors are often completely integrated with the front-end electronics. Although very little information can be found on the dependability of MS circuits, it is one of the most critical parts in this respect [8]. This makes currently an overall grading of the dependability of a heterogeneous SoC in a safety-critical application like e.g. automotive, nearly impossible.

The current industrial strategy to cope with this problem is not tailored towards a SoC design approach, based on reusable IPs. In this strategy, an IP like an OpAmp in a chip has often already been completely redesigned to be reliable (robust) under the expected application and lifetime conditions. This is normally accomplished via following specific design rules (e.g. for NBTI aging) or the usage of *IP-internal*, normally analogue, compensation/calibration techniques.

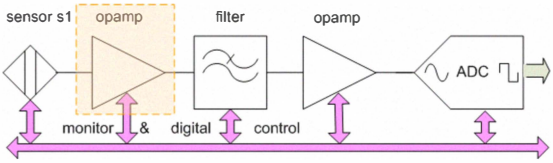

Figure 1: Generic setup of a sensor and a digitally programmable analogue / mixed-signal front-end.

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We present a new approach, which is better suited for IP-based SoC design and more close to future design practices using monitoring and digital controlling of IPs and the vast availability of embedded processors.

In this paper, a viable SoC approach to construct dependable MS-IPs and hence dependable SoCs is provided. As an example IP, a digitally-assisted operational amplifier (Figure 1, boxed-in) will be used.

First, the basic principles of dependability in our context will be briefly stated. Next, the concept of the expected mission profile [9] of a SoC / IP will be discussed. Our new approach for dependability at SoC level, using digitally-controlled MS-IPs, embedded processor(s) and two Infrastructural IPs (IIP), is discussed in paragraph three. As an example, a TPMS (Tyre Pressure Monitoring System) SoC used in automotive applications will be considered. One IP, an OpAmp for amplifying the temperature-sensor output, will be treated in more detail. Reliability simulations, assuming certain dominant reliability mechanisms under its mission profile are carried out to illustrate the aging influence on the behaviour of key parameters. These consequences will subsequently be observed and counter measured by using the digital programming capabilities of the circuit; or in worst case replacement via internal resources, under control of the embedded processor(s). Finally, some conclusions are provided.

2 Dependability of Mixed-Signal IPs

Dependability is the extent to which a system can be relied upon to perform its intended functions under defined operational and environmental conditions at a given instant of time or given interval [2]. With regard to the dependability of analogue / mixed-signal integrated circuits very few publications have appeared [8]. This is partly because usually only the reliability aspect of MS circuits is considered or in combination with robust design [10]. However, dependability is more than just reliability [2-4]. Without treating dependability in depth, important attributes in our case are:

1) Reliability,
2) Maintainability
3) (Un-) availability and Safety.

Reliability of a system can be specified as a number after a certain life time, e.g. 0.9876 after 15 years; this indicates that 1.24 percent of the systems are expected to fail after 15 years.

In the case of an embedded IP, *maintainability* and repair in the classical sense is still not feasible. However it is possible in the sense that faults in an IP can be internally detected, might be internally compensated, or if not feasible, the IP could be isolated / bypassed and replaced by similar internal resources via electronic rerouting.

The *unavailability* can be indicated in time (s) in a year or after a fault event; it is the time over lifetime during which the system is being repaired (and hence unavailable). Because of our automatic electronic nature of this process, the unavailability can be very low, for instance 10ms [6].

Safety is the occurrence or risk of injury, loss and danger to persons, property or the environment. Safety can be described, among many others, by a percentage; e.g. in safety-critical systems, safety should be 100%, meaning that under no condition any risk should exist. For instance, the output of an IP should go to a predefined safe value (halt) in the case of a non-repairable fault.

Hence, in the ideal case, the reliability of a fully dependable system should be 1 (100%) until the specified lifetime (e.g. 15 years), is never unavailable (0s) and features a 100% safety.

The conditions under which a SoC during its lifetime is expected to being subjected to, is normally referred to as its *mission profile* [11]. This profile obviously heavily depends on the application, which is usually unknown to a SoC-IP designer. One can distinguish between environmental (e.g. Temperature, Relative Humidity, Pressure) and operational (e.g. Voltage, Current, Power) conditions of the SoC. The automotive arena is well known to have tough conditions in both. In addition, reliability as well as safety plays a very important role. Furthermore, a car should not require a maintenance visit for *electronic* repair. For the sake of simplicity we will confine ourselves in this paper to the temperature in the mission profile only, and hence exclude a number of failure mechanisms.

Within a temperature mission profile, different aging mechanisms that jeopardize the reliability of a CMOS IP can be dominant in certain temperature/operating ranges. The most common are Negative-Bias Temperature Instability (NBTI) effect, Positive-Bias Temperature Instability (PBTI), Hot Carrier Injection (HCI), Electron Migration (EM) and Time-Dependent Dielectric Breakdown (TDDB). To go into more details of these mechanisms is beyond the scope of this paper. An excellent overview and explanation of these mechanisms and related formulas have been presented in reference [12]. To use these aging effects for evaluation in a circuit simulator like Spectre, tools like RelXpert [13] or proprietary tools like PRESTO [14] are available. This requires the translation of these effects (e.g. NBTI and PBTI) into the *component* simulation model levels, and verification for a specific technology as discussed for instance in reference [14]. In other words, for instance RelXpert will drive Spectre for lifetime and degradation computations. As a result it will generate a new netlist

allowing an "aged" simulation. A number of publications have appeared on reliability simulation of analogue / MS circuits [16, 21, 22].

This information will be used later on, in evaluating the aging behaviour of our OpAmp by circuit simulation, and conclude where counteractions have to be taken.

3 The SoC System Approach Towards Dependability

For semiconductor companies dealing with safety-critical systems, often the dependability flow is one of strict following *rules*. This can be e.g. by following the design guideline book with respect to the different dependability threats. In this way a robust MS design is forced for a *particular* application / mission profile.

If a fabless design company is developing a SoC-IP, the application area / mission profile of the SoC is unknown in advance. Our chosen strategy is to use the (sometimes already available) digital programming capabilities of MS circuits and observation extensively and/or enhance these capabilities if required. This basically moves the SoC dependability issues where they belong, with the SoC system designer who is well aware of the actual application area of the SoC. Furthermore, by providing a link to the embedded processors, which will be massively available on-chip in future, SoC systems, many scenarios can be handled in a flexible manner via embedded *software* programming.

This is favoured over a complete dedicated redesign of the analogue / MS parts to accomplish a robust design over the final mission profile, or the (expensive) standard insertion of spare resources.

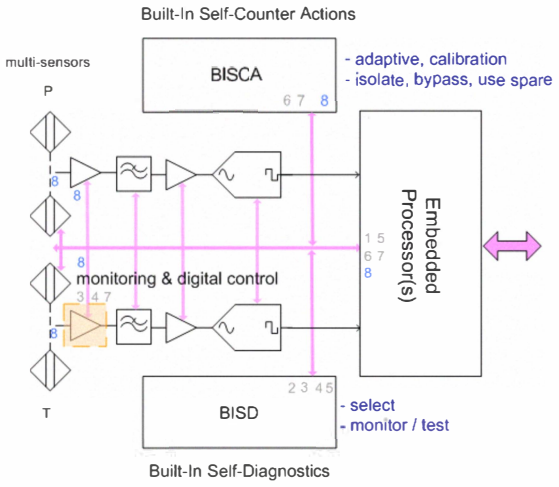

Figure 2: System set-up of the dependable IP-SoC concept

Figure 2 shows the basic elements of our approach in a SoC. It consists of two infrastructural IPs (IIP), and general embedded processor(s). The *BISD* (Built-In Self-Diagnostics) IIP takes care of selecting an IP via a connection (e.g. bus) and monitoring the required parameter(s) for an input signal for aging and hence to accomplish a diagnosis. Also direct monitoring of aging is an option, e.g. via on-chip NBTI [16] or HCI [17] monitors; this requires a different approach which will not be further discussed. Monitoring by selftest and calibration is very IP dependent and hence they will be discussed in the paragraph dealing with the OpAmp.

The *BISCA* (Built-In Self-Counter Actions) IIP takes care of controlling the chosen parameters from the BISD to compensate for the aging degradation. In some cases, it will be decided that compensation is outside the controlling range, and hence an isolate, bypass, spare resource procedure can be applied *if* the SoC infrastructure provides this option. In Figure 2, the multi-sensor system is equipped with two parallel processing paths, which means in this case time-multiplexed duplicate resources are available. Of course the programming of resources is still flexible to take account in the case of a different sensor. This fits very well in the strategy of providing a reusable MS-IP and use digital programming for tailoring it to a specific application in a SoC.

In future, the combination of the BISD and BISCA into one IIP, the Dependability Manager, is feasible, similar to what has happened in the digital case [6].

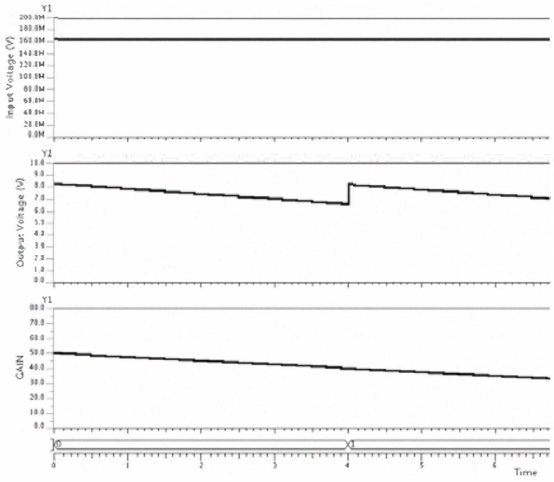

Figure 3: ADVance VHDL-AMS simulation of temperature sensor with gain programmable OpAmp (Figure 2)

The dependability flow is illustrated by numbers in Figure 2. The embedded processor starts communicating (1) with the BISD to start up (2) the dependability procedure. The BISD starts communicating (3) with the specific IP over a bus, being our OpAmp (boxed-in). Next, it delivers the observed parameter to the BISD (4). It provides the results (5) to the embedded processor, which *decides* to take the proper action if required and starts up the communication (6) with the BISCA. Here the digital codes are generated for the calibration (7) or bypass

action of the IP (8). The latter involves in that case the additional (time-multiplexed) use of the top OpAmp (8) via multiplexers to reroute pads. A (second) verification round will check that the counteraction was successful.

To illustrate the basic concept shown in Figure 2, a simple simulation example of a temperature sensor is provided, connected to a digitally controlled OpAmp. This VHDL-AMS simulation can be seen in Figure 3. At the top, the output voltage of the temperature sensor is shown at a constant (internally generated) temperature. In the next graph, the gain of the OpAmp is monitored via the output voltage in the BISD. Now the simulation assumes a reduction in gain due to aging as shown in the third graph. The embedded processor observes the output deviates from the reference value and hence it instructs the BISCA to apply a specific digital code from the BISCA (Figure 3, bottom signal) to the OpAmp to compensate for this loss. As can be seen in the second graph from the top, this results in adaptation of the gain, and hence restoration of the original output voltage. The required actions of the BISD and BISCA combined with the embedded processor are included in a program. As simulator, the Mentor ADVance tool (Questa ADMS) has been used.

It is unlikely that all influences of the mission profile and resulting reliability degradation of MS circuits can always be compensated by digital self calibration. In those cases regular fault-tolerant techniques will be required. The approach is scalable and can be extended to more IPs. The dependability costs would not include the existing embedded processors, or the existing digital calibration options in IPs. So basically, the cost of the busses, the BISD and BISCA and adaptations in IPs would have to be included. The BISCA can be a cheap LUT-based circuit, or part of the processor. The costs of the BISD strongly depend on the signal generation requirements. 15% of the SoC costs seem reasonable, assuming no spare IP resources are included.

It is a different approach from making an MS circuit robust, as our method is generic. The time required for reprogramming is essentially related to the availability/unavailability of the circuit.

4 The Target System: TPMS

In our current CATRENE project[1], temperature would be the first variable to be measured dependably with a sensor; several potential temperature sensors were investigated in the demanding automotive applications. An interesting application is the Tire Pressure Monitoring System (TPMS) [18]. It directly affects the safety (tyre blow-out, burst) of a car (6% of accidents) and hence requires a highly dependable design. In addition there is a clear reliability (wear) as well as maintainability (SoC inside tyre) issue.

The basic set-up of the TPMS *inside* the tyre is shown in Figure 4, which is not essentially different from any generic wireless multi-sensor system. Overall control is carried out by the micro controller unit (MCU). The small battery can be 3V, and the RF transmitter operates at the designated frequencies, e.g. 434MHz. The receiver part and display in the cabin are not shown and will not be dealt with.

Normal tyre pressure is between 30 and 34 psi, but this depends on the ambient/tyre temperature. During the day it can easily change 5 psi due to *ambient* temperature changes.

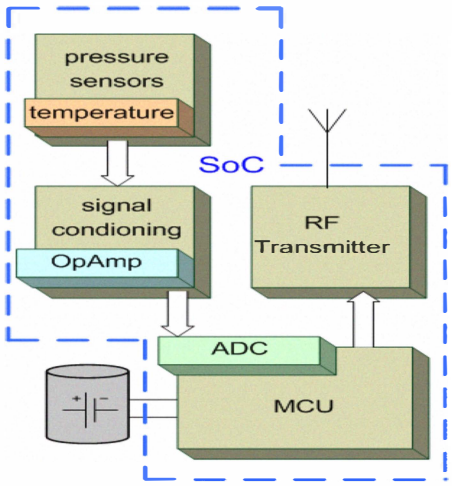

Figure 4: Basic set-up of a Tyre Pressure Monitoring System (TPMS) SoC *inside* the tyre.

The temperature range *in* a tyre can be up to 85^0C under normal driving operation and 110^0C under exceptional conditions [19]. Under inflation of 8 psi already reduces the tyre lifetime with 20%, while more has direct effects on car control (e.g. tracking, stopping). Batteries (Figure 4) can operate up to 10 years, P can be 60psi and the RH can be up to 100%. Because of the important pressure temperature relationship, the temperature measurement is very important. The required temperature sensitivity should be 1^0C from -45^0C until 130^0C, with a stability of 2^0C over its lifetime. In this paper, we will look at the temperature OpAmp combination and its change over the TPMS mission profile.

A safe evaluation mission profile is 15 years (min. 10 years) under 125^0C (min. 110^0C). An example of a commercial TPMS device is the Freescale MPXY8300 [20].

5 Design, Verification and Aging of a Simple OpAmp IP

As an example, the reliability of a digitally-assisted OpAmp (Figures 1, 2, 4) has been investigated via simulation. From the conventional reliability degradation mechanisms, discussed in paragraph 2,

only the aging mechanisms NBTI and PTBI have been used. This is because it is very difficult or expensive to have the disposal of models for advanced processes. Several other publications in the past have discussed the search for finding the weak key parameters in specific analogue / mixed-signal IPs in designated CMOS processes [21, 22].

As Figure 4 shows, one of the IP blocks in the TPMS SoC is an OpAmp required for signal conditioning of the temperature sensor. Figure 5 shows the basic set-up at transistor level of a very simple gain amplifier based on reference [23]. It has to amplify the signal from the temperature sensor to a level which can be conveniently handled by the succeeding ADC. Two stages have been used for obtaining sufficient gain for the sensor output. It has a differential input of two PMOSTs, and single-ended output.

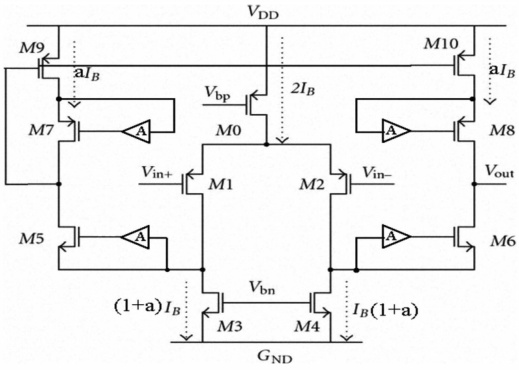

Figure 5: Transistor scheme of a simple two-stage CMOS operational amplifier [23].

The circuit has been designed in Cadence Virtuoso using a 65nm CMOS technology. Some of the simulated key parameters of the OpAmp are the DC gain (66 dB), the offset (86µV) and the bias (645 µA). These Spectre simulations have been carried out under normal conditions and no aging models have been used for components.

In the aging simulations of the OpAmp, the mission profile has been assumed conform to be expected in the TPMS application (paragraph 2). The previous key parameters of the OpAmp have been evaluated in this way. The offset and bias hardly changed. The gain has somewhat increased after aging. In the next paragraph, it is explained how this gain can be monitored *externally* (outside the IP, but inside the SoC*)*, and which kind of means are available to change the parameter to within the tolerances of acceptable performance by external (digital) signals.

6 Observation and Calibration of the OpAmp

6.1 Measuring the gain

The next step is to measure the gain and provide this data to the BISD, either in analogue or digital form. The latter will require a conversion and is hence more costly. In Figure 6, it is shown how this parameter is measured.

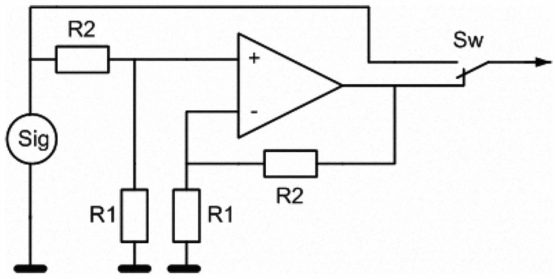

Figure 6: Observation of gain in the OpAmp

The open loop gain of the OpAmp is normally difficult to measure, since its large gain can easily saturate its output. To avoid this situation, the input signal amplitude is needs to be lower than several hundreds of micro-volts. Such a small signal is difficult to generate and kept accurate. There are several alternatives to measure the open loop gain. One approach [24] is shown in Figure 6. The Op-amp is configured as a feed-back amplifier with large feed back (R2/R1) factor. The small input signal, e.g. pulse, is generated via a voltage divider with the same ratio. The output first measures the input amplitude and subsequently (Sw control) the output amplitude. The output is divided by the input to get the close loop gain. With the known feed back factor, the close loop gain can be easily calculated.

6.2 Digitally changing the Gain

The gain of our OpAmp can be tuned by changing the bias current. For the folded cascode OpAmp, the gain is reverse proportional to its bias current, if the bias current ratio between the differential pair and the cascode is kept constant. This is usually the case, because the bias currents of the differential pair and the cascode are both derived from same current mirror.

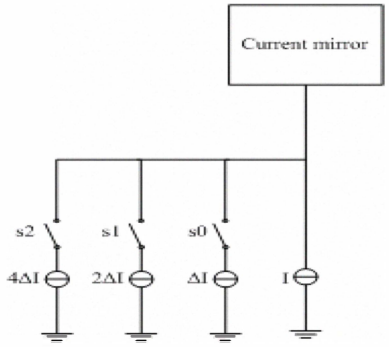

Figure 6: Scheme of the programmable OpAmp gain

The bias current can be tuned using the step tuning circuits shown in Figure 6. The three switch *s1, s2, s3* and additional step-tuning current sources are added to the original bias current source. By carefully selecting the values of I and ΔI, the gain can be

chosen among 2^3=8 levels. Although the gain can be increased by decreasing the bias current, the design freedom is limited. This is because a very small bias current will increase the noise and offset. Furthermore, the bandwidth is also decreased if a small bias current is used, and thus may cause stability problems.

In the embedded processor, it is already stored what the effective variation range is of a parameter in the IP. If the measured data is outside this range, than the replacement procedure is started immediately.

8 Conclusions

In this paper we have discussed an approach to dependable design of a digitally-assisted mixed-signal SoC, by analyzing the dependability of an OpAmp IP under its mission profile conditions, and utilizing the digital programming capabilities for calibration and repair and monitoring and the availability of embedded processor(s).

9 Acknowledgements

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