Silicon Nanowire Fabrication Using Edge and Corner Lithography

Hadi Yagubizade, Erwin Berenschot, Henri V. Jansen, Miko Elwenspoek, *Member, IEEE*,
and Niels R. Tas

Abstract—This paper presents a wafer scale fabrication method of single-crystalline silicon nanowires (SiNWs) bound by $\langle 111 \rangle$ planes using a combination of edge and corner lithography. These are methods of unconventional nanolithography for wafer scale nano-patterning which determine the size of nano-features to be formed. The pattern formed by conventional microlithography determines the location. The presented method is based on the low etch rate of $\langle 111 \rangle$ -planes. Initially, using edge lithography, nanoridges with $\sim 71^\circ$ angle with the wafer surface and bound by $\langle 111 \rangle$ -planes are fabricated. Thereafter, corner lithography is used. The fabricated SiNWs can be isolated from the substrate by oxidation of the thin silicon base.

I. INTRODUCTION

OVER the last decade, there has been an increasing interest in single-crystalline SiNWs as nanomechanical resonators [1] for sensing and signal processing applications with different detection techniques [2]. The low-cost fabrication of single-crystalline SiNWs still is a challenging issue.

Edge [3, 4] and corner lithography [5, 6] have been developed for fabrication of sub-micron features without the need for expensive or low throughput conventional nanolithography. Edge lithography has been applied for fabrication of 2D-confined features like nanoridges [3, 6], nanochannels [7], single-crystalline silicon nanotetrahedra [8] and corner lithography for 3D nanowire frames [5] and silicon nitride pyramid with nano-apertures [6]. In this paper, the combination of edge and corner lithography for fabrication of single-crystalline silicon nanowires (SiNWs) is presented.

Most of the proposed top-down fabrication methods of SiNWs are based on electron beam [9] or scanning probe lithography [10] on silicon-on-insulator wafers followed by thermal oxidation. Thermal oxidation has been used to reduce the dimension and nonuniformity of the SiNWs, but it

applies a considerable stress to SiNW [9, 11, 12]. Isolating SiNWs from the substrate and controlling final dimensions without using long thermal oxidation process is still a considerable issue.

This paper presents a new fabrication method of low stressed SiNWs using short thermal oxidation steps with fully controllable final dimensions on a standard $\langle 111 \rangle$ silicon wafer rather than on a silicon-on-insulator wafer. The fabricated SiNWs are insulated from the substrate by an innovative undercut procedure.

II. FABRICATION SCHEME

Fig. 1 shows the fabrication scheme of SiNW on a $\langle 111 \rangle$ silicon wafer. The fabrication started with low pressure chemical vapor deposition (LPCVD) of silicon nitride layer (~ 550 nm), Fig. 1(a). Then a layer of positive photoresist (Olin 907/17) was spin coated and optically exposed. The resist was developed using Olin OPD 4262 resist developer and followed by a postbake of 30 min at 120°C . The silicon nitride was patterned by RIE using the photoresist as mask, Fig. 1(b). After a 1% hydrofluoric acid (HF) dip to remove the native oxide and contaminants in RIE step, the silicon was etched in 25% KOH at 75°C , Fig. 1(c). Silicon nitride retraction etching was performed in 50% HF leaving a thin layer of ~ 50 nm thick [4]. After a standard cleaning and a 1% HF dip to remove the oxide that has been formed during the standard cleaning, the exposed silicon part was dry oxidized at 950°C to perform Local Oxidation of Silicon (LOCOS) using silicon nitride as the mask, Fig. 1(d). Then the silicon nitride was stripped in hot phosphoric acid. By using the LOCOS mask, silicon was etched by 25% TMAH at 70°C which has very good selectivity between silicon oxide and silicon [4, 6]. As seen in Fig. 1(e), the nanoridge with acute ($\sim 71^\circ$) and obtuse ($\sim 109^\circ$) angles was formed which give the opportunity to apply corner lithography [6]. After stripping the LOCOS, 100 nm silicon nitride was deposited by LPCVD (conformal deposition), Fig. 1(f). By using timed-etch process, deposited silicon nitride was etched isotropically in 50% HF. This is a timed-etch process. Around 1.30 times over-etching has been done. Finally, only a small residue of silicon nitride remains in the acute angle. The remaining silicon nitride was used to cover and protect the acute angle corner of the ridges during next oxidation step. After a standard cleaning and 1% HF dip, the silicon nanoridge was dry oxidized at 950°C , Fig. 1(g). The silicon nitride was removed in hot phosphoric acid and subsequently the silicon was etched by 25% TMAH at 70°C , Fig. 1(h).

Manuscript received June 28, 2010. This work was supported by the Dutch Technology Foundation STW.

H. Yagubizade, E. Berenschot, H. V. Jansen and N. R. Tas are with Transducers Science and Technology Group, MESA+ Institute for Nanotechnology, University of Twente, P.O. Box 217, NL-7522 NH, Enschede, the Netherlands (phone: +31-53-4894373; fax: +31-53-4893343; e-mail: h.yagubizade@utwente.nl; j.w.berenschot@utwente.nl; h.v.jansen@utwente.nl; n.r.tas@utwente.nl).

M. Elwenspoek is with Transducers Science and Technology Group, MESA+ Institute for Nanotechnology, University of Twente, P.O. Box 217, NL-7522 NH, Enschede, the Netherlands and Freiburg Institute for Advanced Studies (FRIAS), University of Freiburg, Albertstrasse 19, D-79194 Freiburg, Germany. (e-mail: m.c.elwenspoek@utwente.nl).

Fig. 1. Fabrication scheme of SiNW using edge and corner lithography.

After stripping LOCOS, Fig. 1(i), the fabricated nano-ridges are dry oxidized at 950°C for 45 minutes, Fig. 1(j).

III. RESULTS AND DISCUSSION

A. Fabricated Structures

In Fig. 2, a scanning electron microscopy (SEM) picture of the undercut single-crystalline silicon nanoridge with LOCOS as a mask, (Fig. 1(h)) is shown. In Fig. 3, a SiNW of approximately 48 nm wide and a height of 248 nm with a 37 nm layer silicon oxide around it and isolated from the silicon substrate is shown.

Note that the initial microscale features have a left and a right edge. Fig. 4 shows both sides of the fabricated structures after the corner lithography step (both sides of the features of Fig. 1(g)). Fig. 5 shows a SEM picture of the opposite side of Fig. 2.

Fig. 2. Scanning electron micrograph of the silicon nano-ridge as schematically shown in Fig. 1(h).

Fig. 3. Scanning electron micrograph of oxidized silicon nano-ridge as schematically shown in Fig. 1(j).

B. Designing and the Final Dimensions of the SiNW

In this fabrication method the width of the nanoridges and therefore nanowires depend on the pull-back size in the retraction etching process. Therefore the minimum initial thickness of the silicon nitride layer is a critical parameter to lead to the proper final dimensions of SiNWs. The height of the nanoridges and nanowires is determined by silicon etching steps in $\langle 111 \rangle$ -planes (Figs 1(c) and 1(e)) therewith because of the lateral etching, these steps will also influence the final width of the nanoridges and subsequently nanowires. 25% TMAH was chosen because it has a good selectivity with respect to silicon oxide. In the silicon etching step after corner lithography (Fig. 1(h)), the size of the opening is an important parameter as well. This size depends on the size of the residual silicon nitride after corner lithography (Fig. 1(g)). This step is described in more detail in the section D. As seen in Fig. 1(h), after silicon etching, a thin layer of silicon remains as the base. In this paper, we continued with the remained base to isolate the single-crystalline silicon from the substrate by thermal oxidation (Fig. 1(j)). There is another option: By continuing silicon etching till the whole base is etched, SiNW separated from the substrate with three sides covered by LOCOS and an accessible bottom side can be achieved.

Fig. 4. After corner lithography cross section of both sides of microscale patterns by optical lithography.

Fig. 5. Scanning electron micrograph of the right side (undesired) silicon nano-ridge as schematically shown in Fig. 4.

As we described, in this fabrication process the final dimensions of SiNW depend on several parameters to obtain the proper dimensions.

C. Silicon Nitride Retraction Etching and Uniformity

Silicon nitride retraction etching has been done after step c in the fabrication scheme, Fig. 1. This step is shown in Fig. 6 in more detail. A thick silicon nitride retraction etching sequence has been shown in Fig. 6(a). Line $C - C'$ plays most important rule in the retraction etching step. Because the final result will end up at line $D - D'$ which is an almost exact image of line $C - C'$. Subsequently local uniformity of patterns depends on uniformity of silicon etching step before the retraction etching. As seen in Fig. 6(b), if there is local nonuniformity in patterning of silicon nitride caused by mask roughness, the final result of silicon etching (line $C - C'$) will lead to local uniformity after the silicon etching step. The reason is the slow etching in $\langle 111 \rangle$ -direction [13]. Line $B - B'$ shows the boundary of $\langle 111 \rangle$ -planes which the anisotropic nature of the KOH etchant tends to remove other planes than the slow etching in $\langle 111 \rangle$ -planes.

Nonuniformity of silicon nitride deposition will not lead to nonuniformity in retraction etching and just depend on pull-back size of the silicon nitride.

D. Corner Lithography

Corner lithography process (Fig. 1 (f) and (g)) was started with depositing a silicon nitride layer with a desired thickness (t) and subsequently back etched. This is a timed-etch process. In the etching step, silicon nitride layer in the whole planer surfaces is etched and based on the angles on the corners still a small residual of the silicon nitride remains. As seen in Fig. 7, the amount of the residual silicon nitride in the acute angle ($H_1 = 0.78t$) is more than the residual silicon nitride in the obtuse angle ($H_2 = 0.23t$). For

Fig. 6. Retraction etching steps in hot phosphoric acid, (a) Cross section while retraction etching, (b) Top view before retraction etching, (c) Top view after retraction etching.

removing all the residual silicon nitride from both sides, 1.78 times over-etching is required. Therefore the total over-etching time can be selected between 1.23 and 1.78 times to control the dimensions of the silicon nitride in the acute angle. Therefore to have a residual silicon nitride just in the acute angle, the etching process was continued till the time that the whole residual silicon nitride in obtuse angle was etched. At the end 0.55 times the initial thickness of the deposited silicon nitride layer remained. By considering the nonuniformity we typically aim at a reminder H_1 of 0.5 times the deposited silicon nitride layer.

Fig. 7. Corner lithography with initial thickness t .

IV. CONCLUSION

We presented a new wafer scale fabrication scheme for silicon nanowires on a standard <111> silicon wafer using initially edge and subsequently corner lithography. The thickness of the first deposited layer of silicon nitride is the most important parameter to determine the maximum width of the silicon nanowire. In this paper, a 550 nm thick initial silicon nitride was used leading to SiNWs of about 48 nm in width and 248 nm in height. SiNWs were isolated from the substrate by a thin layer of silicon oxide base. Using this new method the fabrication of SiNW with tuneable final dimensions is possible. All these options can form a relatively cheap wafer scale fabrication of single-crystalline silicon nanowires without the need for dedicated nanolithography tools.

ACKNOWLEDGMENT

The authors would like to thank Dr. Leon Abelmann for his helpful discussions.

REFERENCES

- [1] X.M.H. Huang, X.L. feng, C.A. Zorman, M. Mehregany and M.L. Roukes, "VHF, UHF and microwave frequency nanomechanical resonators," *New Journal of Physics*, vol. 7, 2005, 247.
- [2] K.L. Ekinci, Y.T. Yang, X.M.H. Huang, and M.L. Roukes, "Balanced electronic detection of displacement in nanoelectromechanical systems," *Appl. Phys. Lett.*, vol. 81, 2002, pp. 2253-2255.
- [3] J. Haneveld, E. Berenschot, P. Maury and H. Jansen, "Nano-ridge fabrication by local oxidation of silicon edges with silicon nitride as a mask," *J. Micromech. Microeng.*, vol. 16, 2006, pp. S24-28.
- [4] Y. Zhao, E. Berenschot, H. Jansen, N. Tas, J. Huskens and M. Elwenspoek, "Sun-10 nm silicon ridge nanofabrication by advanced edge lithography for NIL applications," *Microelectronics Engineering*, vol. 86, 2009, pp. 832-835.
- [5] E. Sarajlic, E. Berenschot, G. Krijnen and M. Elwenspoek, "Fabrication of 3D nanowire frames by conventional micromachining technology," *Transducers '05 [Digest of techn. Papers 13th Int. Conf. on Solid-State Sensors, Actuators and Microsystems]*, pp. 27-29.
- [6] E. Berenschot, N.R. Tas, H.V. Jansen and M. Elwenspoek, "3D-nanomachining using corner lithography," *In Proceedings of the 3rd IEEE International Conference on Nano/Micro Engineered and Molecular Systems, Sanya, China*, January 2008, pp. 729-732.
- [7] N.R. Tas, J.W. Berenschot, P. Mela, H.V. Jansen, M. Elwenspoek and A. van den Berg, "2D-Confined Nanochannels Fabricated by Conventional Micromachining", *Nano Lett.*, vol. 2, 2002, pp. 1031-1032.
- [8] J.W. Berenschot, N.R. Tas, H.V. Jansen and M.C. Elwenspoek, "Chemically anisotropic single-crystalline silicon nanotetrahedra," *Nanotechnology*, vol. 20, 2009, pp. 475302(7pp).
- [9] G. Pennelli and M. Piotta, "Fabrication and characterization of silicon nanowires with triangular cross section," *J. Applied Physics*, vol. 100, 2006, pp. 054507.
- [10] J.T. Sheu, J.M. Kuo, K.S. You, C.C. Chen and K.M. Chang, "A new fabrication technique for silicon nanowires," *Microelectronics Engineering*, vol. 73-74, 2004, pp. 594-598.
- [11] M. Najmzadeh, D. Bouvet, P. Dobrosz, S. Olsen and A.M. Ionescu, "Investigation of oxidation-induced strain in a top-down Si nanowire platform," *Microelectronics Engineering*, vol. 86, 2009, pp. 1961-1964.
- [12] K.E. Moselund, P. Dobrosz, S. Olsen, V. Pott, L. De Michielis, D. Tsamados, D. Bouvet, A. O'Neill and A.M. Ionescu, "Bended Gate-All-Around Nanowire MOSFET: a device with enhanced carrier mobility due to oxidation-induced tensile stress," *In Proceedings of the IEEE Int. Elect. Devices Meeting (IEDM 2007)*, 2007, pp. 191-194.
- [13] R. E. Oosterbroek, J. W. Berenschot, H. V. Jansen, A. J. Nijdam, G. Pandraud, A. van den Berg and M. C. Elwenspoek, "Etching methodologies in <111>-oriented silicon wafers," *J. Microelectromec. Sys.*, vol. 9, 2000, pp. 390-398.