ETCHING TECHNOLOGY FOR MICROCHANNELS

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ABSTRACT

Various ways of fabricating channels in silicon are discussed. Some new channels are presented: the GPSIC's and the LPCVD covered channels. Also some attention is paid to the problem of making connections of these channels to the outside world.

1. INTRODUCTION

In microsystem technology, different types of connections between devices are needed. These can be divided into three groups: mechanical, electrical, and fluidic connections. Fluidic connections mostly consist of channels with diameters of about 30 μm or more. Apart from connecting different devices, these channels can also be used as separation columns in chromatography, in inkjet print heads or as heat exchangers for cooling computer chips. Transparent channels can be used in optical detectors.

In order to get some idea of the many possible ways to fabricate microchannels, in this article a review of the current state of technology for fabricating microchannels for μ -fluidic purposes using micromachining techniques is presented, together with some new techniques recently developed in our laboratory. We will also pay some attention to connections of these channels with the outside world.

2. OVERVIEW

2.1 Silicon etching

The etching of silicon can basically be done in four ways: wet anisotropic, wet isotropic, dry anisotropic and dry isotropic.

For wet anisotropic etching, basic solutions of KOH in water are mostly used. The shape of the etched structures is determined by the slow-etching (111) planes¹.

For wet isotropic etching aqueous acidic solutions containing HF and HNO₃ are necessary. The composition of the solution determines the final shape of the channel². Isotropic etching of silicon is a diffusion limited process, so in principle the only restriction concerning the shape of the structures that are to be etched is that they will always have round corners.

For dry etching, a plasma etching machine is used. By varying the etching conditions, the shape of the channels

can be varied from perfectly isotropic to exactly straight. Also positive or negative tapering is possible.³

Figure 1 The first step in making a channel in silicon

The basic approach for constructing channels in silicon is almost always as depicted in figure 1: the silicon (in this case {100} oriented) is covered with a mask material, the mask material is patterned, and the silicon is etched using one of the methods described above. The channel on the left of the picture is etched

isotropically, the middle anisotropically using RIE etching, and the channel on the right is etched anisotropically in a KOH solution. After etching there is a number of ways to proceed, depending on the desired channel configuration. We will discuss various methods to construct channels from different materials, highlighting the work that has recently been done in our laboratory.

2.2 Closure by bonding of another wafer on top of the channel

The easiest way of proceeding from the situation sketched above is the closing of the channel by bonding a glass or silicon wafer on top of it. This is a very simple method and has therefore been used many times in analytical applications^{4,5,6,7}. A further development in this method is the use of two wafers, in each of which one half of the channel is etched. After bonding, a channel with the desired shape (e.g. with a circular cross-section) is obtained^{8,9,10}. In this case the etching processes have to be carefully controlled to avoid differences in diameter of the channels on both wafers. There is also the possibility of misalignment during bonding.

Advantages of the bonding approach are its simplicity and the possibility to coat the channel or fill it with for example a packing material for chromatographic purposes before the second wafer is bonded on top of it. Disadvantages are the possible formation of microvoids at the bonding interface (in the worst case parallel channels can be connected by these voids). These voids can occur due to particles, and also because of the high

temperatures in which most bonding processes take place (450 - 1100 °C, depending on the bonding technique). The pressure in closed spaces can then get very high, and the air trapped inside those spaces presses the wafers apart. This can be avoided by bonding the wafers in vacuum. One also has to consider that materials with which the channel is filled or coated prior to bonding have to be able to withstand the high temperatures that occur in the next manufacturing processes.

2.2.a LPCVD coated channels

Figure 2 Channel of which the wall is coated by growing a silicon nitride layer. Part of the surrounding silicon has been etched away

Figure 3 Channels with a half-circular cross-section (●), coated with silicon nitride. Part of the top silicon wafer is etched away to show the coating of the channels. The flat silicon nitride wall of the rightmost four channels has been peeled off.

If the channels that are constructed propagate to the edge of the wafer and are thus open on one or both ends, they can be coated with a silicon oxide or silicon nitride layer using a LPCVD process. Possible microvoids are filled by the coating material, and dead volumes are eliminated. This was done in our laboratory for straight channels of 4.5 cm length with a half-circular cross-section (●) and a largest diameter of 96 μm that were open on both ends. We used TEOS and LPCVD silicon nitride as coating materials. A layer of 2 μm thickness was deposited on the wafers containing the channels. The thickness of the coating on the channel wall depends on the distance from the opening. The thickness of the wall seems to decrease exponentially with increasing distance from the channel opening. At a distance of 1.5 cm from the entrance, the silicon nitride layer thickness was 62 nm, as estimated from SEM pictures. We found silicon nitride over the whole length of the channel. In the case of TEOS, the thickness of the coating decreases faster; at a distance of 1.5 cm from the channel opening, the layer thickness was only 31 nm. At longer distances no TEOS was found. Examples of channels coated with silicon nitride are shown in figures 2 and 3.

2.2.b Ground Plate Supported Insulating Channels (GPSIC)

Figure 4 Process scheme for making GPSIC's

For electrophoresis applications, microchannels made in insulating materials are needed. One way to produce the channel is to etch it in one or two glass wafers and bond these on top of each other^{7,10}. This method has the disadvantage that in glass only isotropically etched channels can be made. Therefore we developed the GPSIC method. The production process is depicted in figure 4.

First the channel is etched in silicon. The etching process can be isotropic or anisotropic as described in the introduction of this chapter. The mask material is removed and the channel is covered with two thin layers of LPCVD silicon nitride (50 nm) and silicon oxide (TEOS, max. 600 nm) respectively. The silicon oxide is needed to be able to bond the wafer anodically to a glass wafer (a wafer covered with silicon nitride can not be bonded anodically). After bonding, the silicon wafer containing the channels is etched away using an isotropically etching solution, leaving the free standing

silicon nitride. The etch-back can also be done using an anisotropic etching solution. In this case an extra layer of polysilicon has to be applied before applying the silicon nitride and -oxide layer, to prevent the appearance of 'left-over' silicon in corners due to the anisotropic etching. Examples of GPSIC's are shown in figure 5 and 6.

The GPSIC process leaves channels with a user-determinable shape (they can be etched isotropically or anisotropically, using an etching solution or RIE etching), which are transparent, so they can be used in an optical detection system. They can be cooled very easily due to the thin walls. The thin walls are also a disadvantage: they can break very easily.

Figure 5 Cross-section of a GPSIC. The ground plate is a HOJA SD-2 glass wafer. The channel consists of a 600 nm thick layer of TEOS and a 50 nm thick layer of LPCVD silicon nitride

Figure 6 GPSIC. On the right side of the picture the silicon wafer in which the channels were etched is left intact

2.3 Closing by layer deposition

The bonding process suffers from certain disadvantages. The wafers that are to be bonded have to be very smooth and clean. Some materials (for instance silicon nitride) are very difficult to bond. Further problems are the formation of microvoids, and alignment problems. To avoid bonding, the channel can also be closed by depositing a layer that closes small holes and this way seals the channel. This can basically be done in two ways: closing holes in the mask material and etching channels buried beneath the surface of the wafer.

2.3.a Closing holes in the mask material

In this case the channel is not defined in the mask material by a long slit, but by a sequence of holes. During etching the mask material gets underetched and the channel is formed. After formation of the channel the mask material is not removed, but a layer of silicon oxide or nitride is deposited on it, which closes the channels. Because of its simplicity and the fact that only standard steps of VLSI processes are used, this approach has been used by Chen and Wise in making an inkjet print head¹¹. They used the flat surface of the channel to accommodate electrode structures for the heaters and interconnect leads. Kaplan and Holm *et al* used this process in chemical analysis systems^{12,13}.

The top layer can be made from transparent materials, which makes these channels applicable in for instance optical detectors for spectrometers. However, due to stress in the thin covering membrane, it can crack easily. Another problem can be that the material that is used to close the channel covers its walls also.

2.3.b Burying channels beneath the wafer surface

Figure 7 The process scheme that French *et al* used for constructing insulated monocrystalline silicon islands

To avoid bonding as well as the fragile covering of the channels described above, we developed a method to etch channels beneath the surface of the wafer. Our procedure is related to the method used by French *et al*¹⁴ to make isolated resistor islands for use in a single crystal silicon piezoresistor (figure 7). They etched narrow trenches (2 μm wide, 10 μm deep) crossing each other perpendicularly in the plane of a silicon wafer, using a RIE process. After that they immersed the

wafer in a KOH solution to yield channels that were partly buried beneath the surface. To insulate the islands that appeared, they oxidized the silicon until a thick layer of oxide was formed.

Figure 8 Production scheme for etching a buried channel. The channel can be etched isotropically as well as anisotropically

Our method is as follows⁹ (figure 8): First, a deep, very narrow trench (typically 100 μm deep, 4 μm wide) is etched using RIE etching. After that, the surface of the wafer is covered with a layer of silicon nitride. This nitride also covers the walls and the bottom of the

trench. Then the silicon nitride in the bottom of the trench is etched away using RIE etching, leaving the bare silicon. Next, the wafer is etched using one of the methods described in the beginning of this chapter. The nitride is removed by etching in 50% HF. The last step consists of the deposition of a thick layer on the wafer, that covers the walls of the channel, and also of the trench. The layer is deposited so thick that it closes the trench. The materials that can be used for the layer are silicon oxide, silicon nitride, and polysilicon. In our case we used LPCVD silicon nitride.

Apart from the absence of bonding, this process has also the advantage that in principle, channels crossing each other at different levels can be made. This can be done in two ways: the simplest is to etch the next channel on the other side of the wafer. If for both channels the same side of the wafer is used, the deepest laying channel has to be coated with polysilicon. This can later be etched away to make room for the second channel that travels in another direction above the deeper laying channel (figure 9).

Figure 9 Buried channels traversing each other

GPSIC's can also be constructed using the buried channel etching method. For this, after closing the trench with silicon nitride, a layer of silicon oxide has to be deposited to facilitate bonding to a glass wafer. After bonding, the silicon wafer can be etched away, leaving the free-standing channels.

Disadvantages of the buried channel etching method are its complexity and the fact that special equipment is necessary, e.g. a RIE with high density source and cryogenic cooling.

2.4 Laser-induced etching

The anisotropic etching of (111) surfaces takes place at a very slow rate. This phenomenon is widely used for making structures in monocrystalline silicon. In {111} oriented silicon wafers, normally no structures can be

etched using the anisotropic etching process. In order to be able to etch this type of wafer, Alavi *et al*^{15,16,17} used laser light to locally melt the silicon, thereby destroying its crystalline structure. After the laser treatment, they etched the silicon anisotropically in KOH solutions, leaving channels that can be partly buried beneath the wafer surface. These channels can only be closed by bonding, however, because of the large opening at the top (100 μm or larger).

3. CONNECTIONS TO THE OUTSIDE WORLD

In most cases the microchannels will in some way have to be connected to the outside world. Most of the times connections are made by etching a hole in the wafer from the backside, and gluing a fused silica tube into it⁸. Manz⁵ clamped his entire HPLC column between two plastic holders with tubes in it which connected also to the channel through holes in the backside of the wafer. In many cases connecting via holes in the backside of the wafer seems to be the only way, especially with fragile channels like those described in section 2.3.a or the GPSIC's. Connections for the buried etched channels can easily be made in the process that is used to define the channels. A large circular opening, connected to the trench is etched. After the covering of the trenches and the large openings, the channels are etched and closed. The large openings can not be closed in this manner, and can be used to insert a capillary in (figure 10).

Figure 10 When buried channels are used, a connection to the outside world can be made by incorporating a large hole in the design

A connection perpendicular to the plane of the wafer is not always satisfactory, due to the large dead volume that is introduced. The most beautiful connection that can be made is a cavity parallel to the plane of the wafer in which a fused silica capillary can be inserted. The inner opening of the capillary then coincides with

the channel. In this case no dead volumes need be introduced. Strandman *et al*¹⁸ made such connections by etching grooves in a {100} wafer with some aligning structures that clamped and centered optical fibres in the grooves. This approach may also be applicable for the aligning of capillaries in microchannels. The capillaries can be glued to seal the entrance, or, if high temperatures are involved in the operation of the device (for example in a gas chromatography column, $\pm 300^\circ\text{C}$), glass with a melting temperature higher than the operating temperature can be used.

4. CONCLUSIONS

A review into the current state of channel-fabricating technology has been presented. These can be divided in two groups: technologies involving bonding, and technologies not involving bonding. In the case of bonding, microvoids can be filled using the new LPCVD covering technique recently developed in our laboratory.

Another new technique we developed, the GPSIC technique, seems promising in the fabrication of electrophoresis channels.

The connections to the outside world mostly used today have the disadvantage of the introduction of large dead volumes. They are also not applicable for use at high temperatures. The clamping structures made by Strandman *et al* for the positioning of optical fibres may also be used for connecting capillaries to a micro fluidic system.

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