## 21.3 A 65nm CMOS 1-to-10GHz Tunable Continuous-Time Low-pass Filter for High-Data-Rate Communications

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As of today, the highest cut-off frequency low-pass continuous-time analog filters are in the frequency band of 1 to 3GHz [2,4-6], targeting applications like UWB communications or hard disk drives. Nevertheless, bands much higher, of about 10GHz, are to be addressed in the near future. This paper demonstrates an active low-pass filter tunable from 1 to 10GHz in 65nm CMOS, which is to our knowledge the highest ever cutoff frequency reported.

In this work the Gm-C topology is adopted for its merits at high frequencies. In this technique, two critical parameters should be accounted for: the accuracy of the Q factors of the pole pairs (for correct transfer function) and parasitic capacitances (for maximal cut-off frequency). The former point is influenced by the phase shift of the integrators compounding the filter in the neighborhood of the filter's edge frequency. This phase error is due to two antagonistic effects which are the integrator's finite DC gain and its high-frequency poles/zeros. The gm-C integrator in Fig. 21.3.1 [1] performs a minimized phase shift due to the absence of internal nodes hence getting rid of high-frequency poles responsible for phase lead with respect to the ideal -90°, and a negative resistance technique boosting the DC gain which is responsible for phase lag. Due to the absence of internal nodes, the integrator's unity-gain frequency and DC gain can be tuned with $V_f$ and $V_g$, respectively. In the early 90's, this method allowed achieving cutoff frequencies of 100MHz in 3µm CMOS, while here we investigate its limits in 65nm CMOS.

The gyrator synthesis method, starting from a doubly terminated LC-ladder prototype, is used for its simplicity, modularity and for gate-drain capacitances cancellation which otherwise would generate zeros responsible for additional integrator phase shift. The node B in Fig. 21.3.1 shows a voltage swing 1.8× higher than the other nodes, thus the 4 transconductors gm4, gm5, gm6 and gm7 are doubled and the capacitor is multiplied by 4. This allows halving the voltage peak at the internal node, keeping the $C_{gd}$ cancellation effect, and being able to absorb a parasitic capacitance 4× higher at this node compared with a non-scaled version. To compensate the 6dB inherent loss of a doubly terminated prototype and also by foreseeing some insertion loss due to process back-end, the input transconductor is multiplied by 3 instead of the conventional factor of 2.

At the transconductor level and in order to minimize parasitic capacitances, the 4 inverters implementing common-mode feedback and negative resistance (inverters b, c) are dimensioned at the minimum size that still guarantees common-mode (CM) stability. CM stability for this filter topology requires to size the inverters such that (gmb+gmc) ≥ 0.66 gma. This theoretical limit (0.66) is verified by simulation; however, during the design a margin of 10% is taken into account. It should be noticed that traditionally in the transconductor gma~gmb~gmc, this means that our optimization allows more than 120% parasitics capacitance saving at each node which roughly doubles the highest achievable operation frequency and saves power. Also, shorted negative feedback transconductors simulating the resistors in the passive prototype are replaced by bare inverters for the same reason of reducing parasitic capacitance and power dissipation.

For the 3rd-order LPF as a rule of thumb, the integrator DC gain (or gm/go of a transconductor) needs to be ~100 and the effective parasitic pole has to be a factor of ~100 above the filter cutoff frequency. We aim here for 10GHz cutoff frequency so the effective parasitic pole of the transconductor should be in the range of 1THz. This requires extensive modeling and design of all parasitic effects, including non-quasi-static transistor modeling. At the complete layout level, extensive use of electromagnetic simulator is adopted, as each parasitic R,L,C effect has an important impact on the filter transfer function.

Minimizing the interconnect resistance and complying with electro-migration (EM) industrial reliability rules imposes the use of wide tracks and stacking of metallization layers. An optimized inverter structure is shown in Fig. 21.3.2 where a 3-pmos 2-nmos structure turned out to be the optimum from inductance minimization point of view. The PMOS and NMOS transistors are interleaved to enhance even more EM reliability. Also, ground shielding techniques borrowed from electromagnetic compatibility engineering and a ground network has been adopted to allow electrons to pick their return path, naturally choosing the one which cancels out connection inductance at high frequencies.

All these layout techniques have the drawback of increasing the capacitive effects. We could however achieve a cutoff frequency of 10GHz at the typical supply voltage condition using only the parasitic capacitances for all the integration capacitances. Filter operation above 8GHz necessitates a tuning voltage $V_f$ >1.2V. It has nevertheless been carefully checked that no thin oxide device in the design is overpassing the reliability voltage breakdown limits on any junction.

For measurement sake, an inverter-based buffer is appended at the output of the filter, and an impedance matching network is plugged at the input and output. A reference path, including the same buffers and matching network is as well integrated on chip, in order to de-embed the filter transfer function. The chip micrograph is shown in Fig. 21.3.7; it occupies an active area of 0.01mm² in an LP 65nm CMOS.

Measurements show S-parameters that correspond exactly to the ideal passive LC prototype (see Fig. 21.3.3). The Q-tuning is performed manually, it shows 1dB gain, 1.2dB ripple, a notch is observed at around 8× the cutoff frequency probably due to a coupling between signal lines via dummy fillers which had not been completely extracted. Varying $V_f$ shows a large tuning range from 0.6 to 10GHz.

The filter measured performances are provided in Fig. 21.3.6 for several cut-off frequency operation modes, and are compared with relevant state-of-the-art. The IIP3 measurements are reported for the edge-of-the-band signal tones (25MHz spacing), while the noise measurements are performed over the filter pass-band using a wide-band instrumentation amplifier at the output. All the presented figures are de-embedded with respect to the input and output access elements by taking into account the additional measurements on the reference path.

The obtained measured performance in terms of noise and linearity, even at the record cut-off frequency of 10GHz, well outstands the existing state-of-the-art. The generic power per pole per Hz figure of merit permits to compare the different implementations. For the same energy efficiency as the work presented in [3], the presented work exhibits ~5× larger cut-off frequency for the same noise behavior and a edge-of-the-band IIP3 of 15dBc better. From an applicative perspective, in the case of 10GHz high-data-rate optical links, an SNR of 36dB is requested which the presented work out-performs with a margin of 9dB.

This paper has demonstrated the feasibility and robustness of up to 10GHz LP CT filters in deep submicron CMOS processes, with excellent noise and linearity behavior and with a continuous cut-off frequency tuning capability of over a decade.

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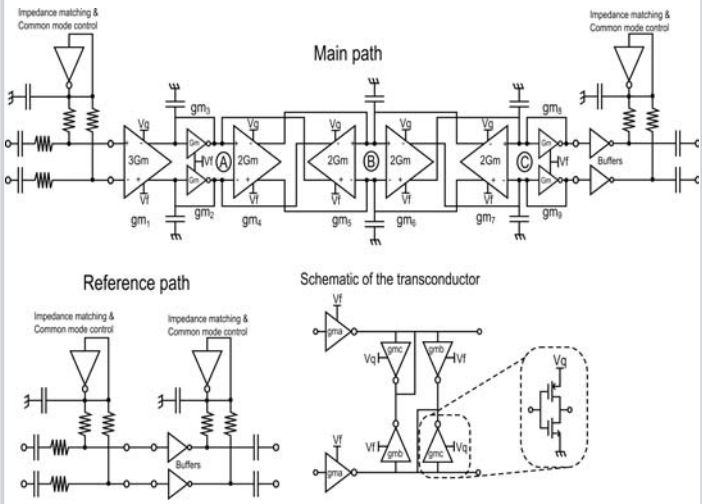


Figure 21.3.1: Gm-C filter implementation (main path, top), reference path (bottom left) and transconductor schematic (bottom right).

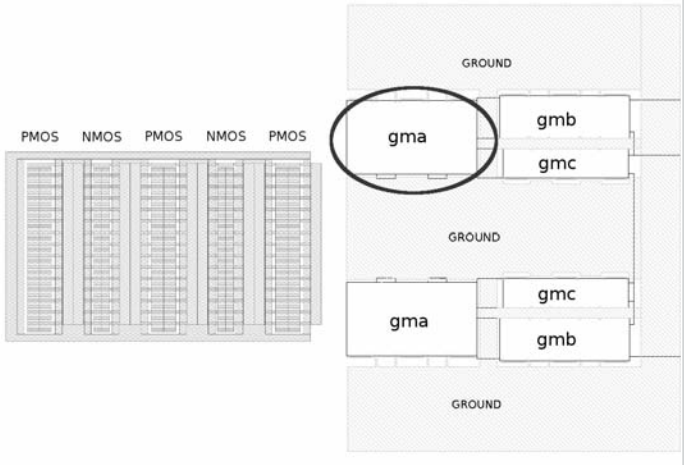


Figure 21.3.2: Partial layout floor plan of a single inverter (left) and transconductor (right).

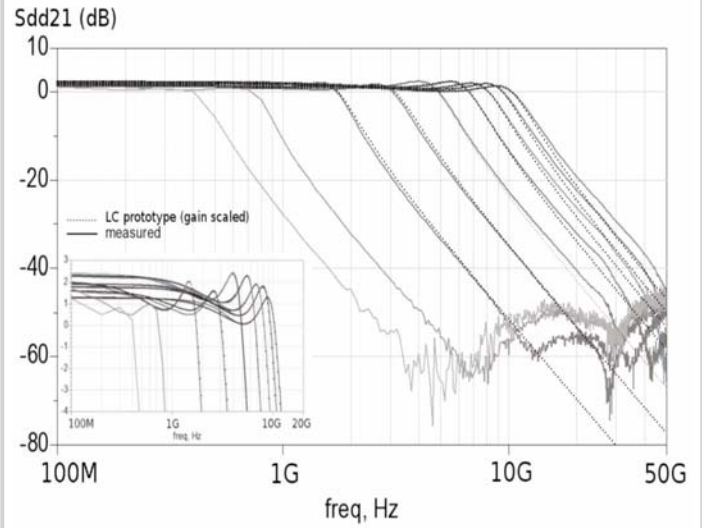


Figure 21.3.3: Measured differential S parameters (solid) and comparison with the ideal LC prototype filter (dashed).

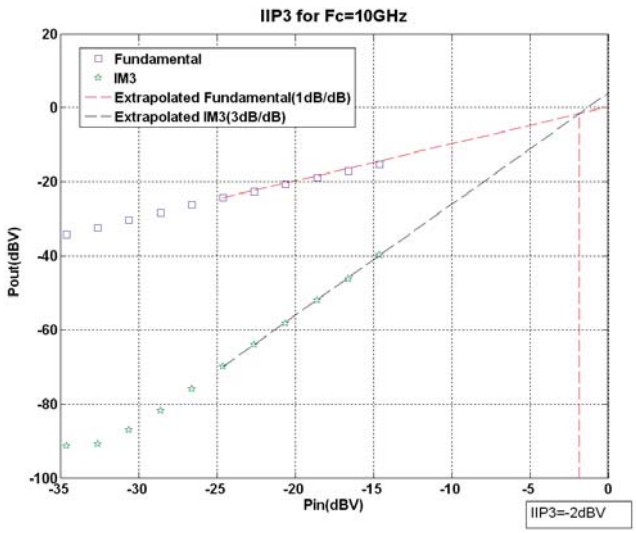


Figure 21.3.4: Measured filter IIP3 for Fc = 10GHz (edge-of-the-band tones with spacing 25MHz).

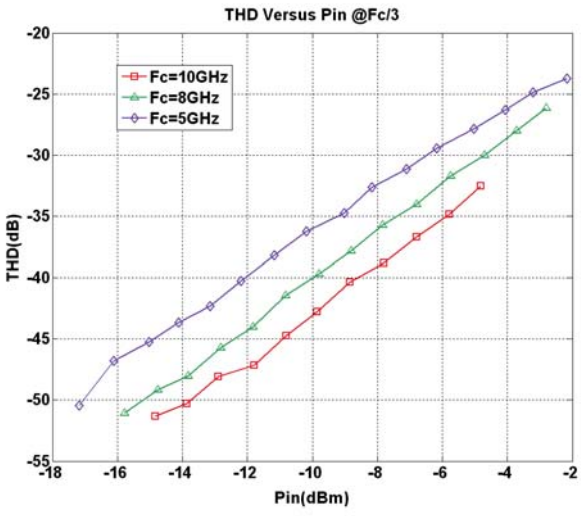


Figure 21.3.5: Measured Total Harmonic Distortion at Fc/3 for Fc = 5, 8 and 10GHz.

| Parameter | This work Fc=4.7GHz | This work Fc=7.9GHz | This work Fc=10GHz | [3] | [4] | [5] | [6] |
|---|---|---|---|---|---|---|---|
| Process | 65nm CMOS | 65nm CMOS | 65nm CMOS | 40nm CMOS | 0.18µm SiGe | 65nm CMOS | 0.18µm CMOS |
| Vdd (V) | 1 | 1.2 | 1.4 | 1.1 | 3.3 | 1.2 | 1.8 |
| Topology | Gm-C | Gm-C | Gm-C | Sallen-Key biquad | Gm-C | Gm-C | Active-RC |
| Type | Chebychev | Chebychev | Chebychev | Butterworth | | Chebyshev | Elliptic |
| Order | 3 | 3 | 3 | 5 | 6 | 5 | 5 |
| Fc\|-3dB (MHz) | 4700 | 7900 | 10000 | 1760 | 3000 | 275 | 500 |
| In-band gain (dB) | 2.7 | 2 | 1.3 | 0 | --- | 9 ... 43 | 0 |
| Input PSD (nVrms/√Hz) | 6.61 | 5.92 | 5.02 | 6 | --- | 7.8 | 18 |
| In-band IIP3 (dBVp) | -3 | -2.5 | -2 | -18 | -2.85 | -12.5 | 13.5 |
| THD @ xx Vpp diff input | -45dB@ 160mVpp | -45dB@ 200mVpp | -45dB@ 264mVpp | | -40dB @ 0.9Vpp | | -40dB @ 1.73Vpp |
| SNR (dB) | 39 | 42 | 45 | | | | |
| Total Power (mW) | 19 | 60 | 140 | 21 | 300 | 36 | 90 |
| Power per pole per Hz (mW/GHz) | 1.34 | 2.53 | 4.66 | 2.38 | 16.66 | 26.18 | 36 |
| Active area (mm²) | 0.01 | 0.01 | 0.01 | 0.0392 | 0.17 | 0.21 | --- |

Figure 21.3.6: Measured filter performances for several cut-off frequencies and comparison with state-of-the-art.

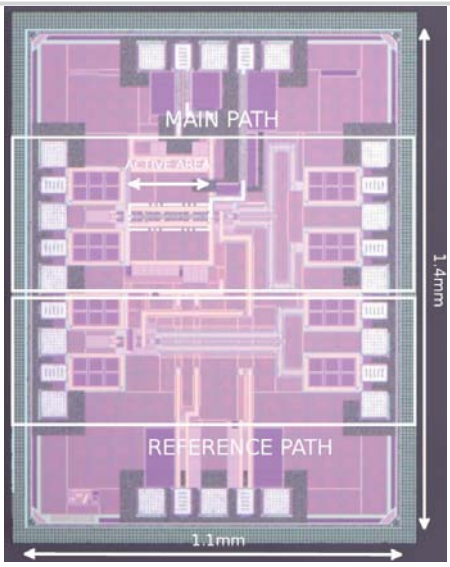


Figure 21.3.7: Chip micrograph.


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