Load-Mismatch Sensitivity of Class-E Power Amplifiers

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Abstract—Class-E RF Power Amplifiers (PAs) are very power efficient under nominal operating conditions. Due to incorporating two tuned tanks, the dependency on the load impedance is however relatively large, resulting in e.g. load dependent output power, power efficiency, peak voltages and peak (and average) currents which can lead to reliability issues. This paper presents load-pull analyses for class-E RF power amplifiers from a mathematical perspective, with analyses and discussions of the effects of the most common non-idealities of class-E PAs: the limited loaded quality factor (Q_{loaded}) of the series filter, switch on-resistance, limited quality factor of the dc-feed inductor, load-mismatch dependent switch conduction loss and the limited negative voltage excursions (due to e.g. the reverse conduction of the switch transistor for negative voltage excursions). The theoretical findings are backed up by extensive circuit simulations and load-pull measurements of a class-E power amplifier implemented in 65 nm CMOS technology. The PA provides 18.1 dBm output power and 72% efficiency at 1.4 GHz under nominal operating condition employing an off-chip matching network.

Index Terms—Class-E PA, constant efficiency contours, constant power contours, load-mismatch, load-pull, power amplifiers (PAs), reliability and degradation, safe operating region.

I. INTRODUCTION

SWITCHED-MODE power amplifiers (SMPAs) have shown great potential for power efficient amplification of RF signals in the past years [1]. Most types of SMPAs incorporate a number of resonant tanks both to ensure e.g. zero-voltage switching (ZVS) and zero-slope switching (ZSS) conditions and to ensure waveform shaping of the output signal [1]–[4]. SMPAs are usually designed for nominal operating conditions where they hence reach optimum performance.

For non-nominal load conditions, the resonant tanks in the SMPAs may get detuned which leads to degraded performance in terms of output power and power efficiency. Closely related to this, detuned tanks result in non-nominal voltage excursions across the switch and non-nominal currents through the switch that may lead to increased degradation of the switch. For RF power amplifiers, typically load-mismatch due to a changing antenna environments is the major external effect causing non-nominal operating conditions [5]–[7].

The sensitivity of the class-E PAs to circuit components variations was studied in [8], [9]. In [8], [9], from a load-mismatch point of view, the effect of the load-mismatch was investigated for very specific cases of having mismatch (only) on the real part or (only) on the imaginary part of the PA load,

separately. However, under load-mismatch and for high voltage standing wave ratios (VSWRs) both the real and the imaginary parts of the PA load (simultaneously) can heavily change. The study provided by [8] was also employed by [10], [11] to mathematically analyze outphasing class-E PAs. However, the derivations are for specific cases of class-E PAs, assuming an infinite and ideal dc-feed inductor, an ideal lossless switch and 50% duty cycle while no reliability related issues were addressed.

Some of the well-known non-idealities on the actual implementation of the class-E SMPAs were studied previously. The effect of the switch conduction loss on the performance of the class-E PAs can be found in e.g. [12]–[14]. The work in [12] aims at designing class-E PAs with sufficiently low maximum voltages and sufficiently high efficiencies with optimizing the switching conditions while [13], [14] study the effect of the switch conduction loss for specific switching conditions (ZVS and ZSS in [13] and ZSS only in [14]). The limited negative voltage excursions across the switch was briefly discussed in [8] for the specific cases of class-E PAs. The work in [15], [16] utilize a parallel diode to (intentionally) shunt negative voltage excursions across the switch when changing the real part of the load from its nominal value to zero. However, the work in [15], [16] holds for a limited range of the loads (only real loads in the range of zero to the nominal value) for a class-E amplifier designed with infinite dc-feed inductor operating at low frequencies (below several MHz). The effects of the limited Q_{loaded} on the design equations of a class-E PA can be found in [17], however, again, for a specific switching conditions (ZVS and ZSS).

In [18], we used the load-pull contours of the ideal class-E PAs to (mathematically) generalize the theory of the outphasing class-E PAs and to improve the back-off efficiency of such PAs. There, only the results of ideal load-pull analyses for a (very) limited area of the class-E PA loads (on the Smith chart) were discussed without providing the derivations of the contours. This manuscript presents mathematical analyses of the effect of load-mismatch on the behavior, performance and reliability of class-E SMPAs, complemented by simulation and measurement results. In the mathematical analyses in this manuscript, the class-E amplifiers are kept as general as possible, hence with arbitrary finite dc-feed inductor, arbitrary duty cycle and arbitrary switching conditions (ZVS and ZSS are not required to be satisfied for the nominal load) and also including the most common non-idealities in actual class-E PA implementations. The non-idealities include the loss of the dc-feed inductor (represented by the quality factor of

the inductor), the conduction loss of the switch, the limited loaded quality factor of the output series filter (Q_{loaded}), limited negative voltage excursions across the switch and the dependency of the switch conduction loss on the load-mismatch.

The objectives of this work include, firstly, developing a basic yet general theoretical model to study the load-mismatch sensitivity of class-E PAs and, secondly, providing the theory behind the load-pull contours employed in the outphasing class-E PA work in [18]. The model is not limited to any specific frequency, output power level, technology nor to any specific class-E design parameters. This basic model provides a(n initial) picture of the load-mismatch effects by providing load-pull-like representation of various performance and reliability related metrics of a class-E PA. We (re)normalize voltages, power levels, currents and use Smith chart representations to be as independent from frequency, power and technology as possible. The presented general model is followed by a case study utilizing the model to study load-mismatch effects on a class-E PA. For the case study, practical class-E design parameters are assumed and from there the impact of changing the so-called relative resonance frequency q and the duty cycle scaling factor d [19], are discussed. Non-idealities further impact the class-E behavior. In contrast to [8], [12]–[14], [17], the impact of the most dominant non-idealities are analyzed for load-mismatch with VSWRs up to 20 using theoretical derivations and simulations and for VSWRs up to 10 in measurements. Finally, load-pull measurement results on a class-E PA implemented in 65 nm CMOS technology confirm our model and analyses of the impact of the non-idealities.

The switch in class-E PAs is usually implemented with one or multiple transistors. The maximum voltage that the transistor can handle (determined by the technology) puts a limit on supply voltage V_{DD} [12]. The size of the transistor and the metal routings are designed by finding the best compromise between the area (parasitics), power efficiency and electromigration rules, see e.g. [20], [21]. To achieve high output power, power efficiency and life-time, V_{DD} and the transistors are typically designed to marginally handle the maximum switch voltage and the maximum switch current. In that case, higher-than-nominal values for the switch voltage (leading to e.g. oxide breakdown in CMOS technology) and for the switch current (leading to e.g. electromigration) cause reliability issues [22]–[24]. These reliability issues can be alleviated by inducing design margins at the cost of e.g. lower output power and a lower power efficiency. The load-pull-like representation of the reliability related metrics of a class-E PA in this current work allows to optimize design margins to handle specific mismatch conditions and as a result allows to define a safe operating area for the class-E PA on the Smith chart.

There are numerous papers on the derivation of the design equations of the class-E PAs and the changing of the design parameters on the performance and the reliability of the class-E PAs. Design equations for the arbitrary finite dc-feed inductor, arbitrary duty cycle and ZVS and ZSS conditions can be found in e.g. [19]. [14], [25]–[28] derive similar equations but for a more relaxed switching conditions; only ZVS or ZSS

is satisfied. The effect of changing the design parameters d and q on the design equations was discussed in [29] for ZVS and ZSS conditions and [20] studied the effect of changing d for ZVS condition. Under load-mismatch conditions the ZVS and ZSS conditions, both are violated. Therefore, to be able to mathematically study load-mismatch effects, new mathematical design equations for general/arbitrary switching conditions were derived similar to [12] but now also including the loss of the dc-feed inductor as well as the switch conduction loss. The outline of this paper is described below.

Section II presents a brief recap on the basics of class-E SMPAs. The mathematical foundation underlying the results in Section II is extended in Section III, to be able to mathematically derive the effects of load-mismatch on the performance of class-E SMPAs. Section IV presents the analyses of the effects of load-mismatch, presented in load-pull plots, on output power, power efficiency and on the switch voltage and switch current. For the theoretical part in this section, infinite loaded quality factor for the series tank (Q_{loaded}) is assumed [19]. This section includes simulation results and discussions of the effect of a finite Q_{loaded} for the series tank, assuming $Q_{\text{loaded}} = 5$ under nominal load condition.

Section V combines the load-pull effects on maximum switch voltage and current from Section IV to determine safe operation region for class-E PAs. The impact of a few non-idealities that occur in actual SMPA circuit implementations is discussed in Section VI. Finally, load-pull measurement results of a class-E PA implemented in 65 nm CMOS technology at 1.4 GHz are given in Section VII. The overall conclusions are summarized in Section VIII.

II. CLASS-E POWER AMPLIFIER BASICS

Class-E PAs are switched-mode RF amplifiers, that in a simplified form consist of a switch and two LC -tanks. In Fig. 1(a), the MOS transistor with its square wave input signal implements the switch, while L and C form the primary resonance tank and where L_0 and C_0 form the band pass filter (second tank) tuned to the transmit band.

The switch transistor is driven by (ideally) a square wave signal defined as [19]

$$S \triangleq \begin{cases} \text{on}; & 0 < \omega_0 t < d\pi \\ \text{off}; & d\pi < \omega_0 t < 2\pi \end{cases} \quad (1)$$

where d is a real number in the interval $[0, 2]$ and $d = 1$ corresponds to 50% duty cycle and where ω_0 is the driving square wave angular frequency. For conventional ZVS and ZSS class-E PAs [30], [31], parameters α respectively β in Fig. 1(b) are zero. In general ZVS or ZSS conditions do not need to be satisfied leading to non-zero α and β , which are defined as [14], [25]:

$$v_C \left(\frac{2\pi}{\omega_0} \right) = \alpha V_{DD} \quad (2)$$

$$\frac{dv_C}{dt} \left(\frac{2\pi}{\omega_0} \right) = \beta \omega_0 V_{DD} \quad (3)$$

where v_C is the drain (switch) voltage and V_{DD} is the supply voltage ¹.

¹In this paper the analysis is conducted at a constant supply voltage.

Fig. 1. (a) Single Ended Class-E PA. (b) Normalized switch (transistor) voltage to V_{DD} and normalized switch current to the average supply current I_0 for a class-E PA using a lossless switch.

For ideal class-E operation, the load impedance $R + jX$, the (angular) signal frequency ω_0 , supply voltage V_{DD} and output power level P_{out} and a number of properties of the Class-E PA itself must be well chosen. PA properties to be well chosen include duty cycle d , switch on-resistance R_{on} and component values.

For general switching conditions, the relations between all class-E PA parameters are formulated in e.g. [12] in so-called the K-design set, see Table I. In [12], all K -values in the K-design set are non-linear functions of parameters q , d , m , α and β . The parameters q , d and m are respectively the relative resonance frequency of the LC -tank, the duty cycle scaling factor as defined in Fig. 1 and the relative switch on-resistance:

$$q = \frac{1}{\omega_0 \sqrt{LC}} \quad (4)$$

$$m = \omega_0 R_{on} C \quad (5)$$

TABLE I
K-DESIGN SET.

$K_L = \frac{L\omega_0}{R}$	$K_C = \omega_0 RC$	$K_X = \frac{X}{R}$	$K_P = \frac{RP_{out}}{V_{DD}^2}$
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The first part of this paper mathematically describes the effects of load impedance mismatch on the behaviour of class-E PAs, in terms of reliability, output power and efficiency. For this, a nominal class-E PA is subjected to non-nominal load impedance conditions. To do this in a mathematical way, the parameters q , d , m , α , β and also the quality factor of the dc-feed inductor L (Q_L), are taken as the inputs to the K-design set and a full $K = K(q, d, m, Q_L, \alpha, \beta)$ design set was derived in a similar way as in [12]–[14], [19], [20], [25]

but now geared towards load-pull style analyses. To include the parameter Q_L in the analysis, we assume a resistance r_L in series with inductor L , shown in Fig. 1(a), where $Q_L = \frac{L\omega_0}{r_L}$. For an ideal dc-feed inductor L we have $r_L \rightarrow 0$ and hence $Q_L \rightarrow \infty$. The full derivation of the K-design set is not the topic of this paper and only a short review in the context of load-mismatch is given in Section III.

III. NON-ZVS AND NON-ZSS CLASS-E PA

To satisfy a pre-determined switching conditions of a class-E PA (e.g. ZVS and ZSS), a specific (nominal) load should be presented to the PA [14], [19], [25]. As a result of a non-nominal load, the switching conditions change. In this section we consider class-E PAs with an arbitrary switching condition.

The switching conditions of the non-ZVS and non-ZSS class-E PA are shown in Fig. 1 and are mathematically given in (2) and (3). For simplicity, a few assumptions are made similar to the approach in e.g. [13]. Firstly, the switch on-resistance R_{on} is assumed to be constant while the off-state resistance is assumed to be infinite. Note that real power losses are only due to non-zero R_{on} , non-zero r_L and discharging capacitor C at the switching moment. Secondly, a high loaded quality factor for the series filter $L_0 - C_0$, i.e. $Q_{loaded} = \frac{L_0\omega_0}{R} \rightarrow \infty$, is assumed in the theoretical analyses, for which the load current, i_R in Fig. 1, can be assumed to be sinusoidal, i.e. $i_R = I_R \sin(\omega_0 t + \varphi)$.

A full mathematical derivation of the switch voltage $v_C(t)$ for $\omega_0 t \in [d\pi, 2\pi]$ (denoted as $v_{C,off}(t)$) and for $\omega_0 t \in [0, d\pi]$ (denoted as $v_{C,on}(t)$) can be readily derived by performing KCL at the switching node v_C and using the continuity of the capacitor voltage v_C and the inductor current i_L at the switching moments. The switch current for the time period that the switch is closed, $\omega_0 t \in [0, d\pi]$, can then be written as $i_s(t) = \frac{v_{C,on}(t)}{R_{on}}$. With the definition of p as

$$p = \frac{\omega_0 L I_R}{V_{DD}}, \quad (6)$$

it can be shown that

$$\frac{v_{C,on}}{V_{DD}} = c_1 e^{s_1 \omega_0 t} + c_2 e^{s_2 \omega_0 t} + \frac{m}{m + \frac{1}{q^2 Q_L}} + A p \sin(\omega_0 t + \varphi) + B p \cos(\omega_0 t + \varphi) \quad (7)$$

$$\frac{v_{C,off}}{V_{DD}} = c'_1 e^{s_r \omega_0 t} \cos(s_i \omega_0 t) + c'_2 e^{s_r \omega_0 t} \sin(s_i \omega_0 t) + 1 + A' p \sin(\omega_0 t + \varphi) + B' p \cos(\omega_0 t + \varphi) \quad (8)$$

where $s_r = \frac{-1}{2Q_L}$, $s_i = q\sqrt{1 - \frac{1}{4Q_L^2 q^2}}$ and where, s_1 , s_2 , A , B , A' and B' can be written as a function of q , m and Q_L while $c_{1,2}$, $c'_{1,2}$, p and initial phase φ depend on all K-design set parameters q , d , m , Q_L , α and β (not shown here for length reasons).

A. K-design set summary

The power delivered by the supply voltage is ideally fully dissipated in the load. However, a non-zero switch on-resistance, limited Q_L and non-ZVS conditions give rise

to extra power dissipation, making up losses. Denoting the average supply current as I_0 , i.e. $\langle i_L(t) \rangle = I_0$, and denoting the output power and loss power respectively as P_{out} and P_{Loss} , then in equation,

$$V_{DD}I_0 = P_{out} + P_{Loss} \quad (9)$$

$$P_{out} = \frac{1}{2}RI_R^2 \quad (10)$$

$$I_0 = \frac{\omega_0}{2\pi} \int_0^{2\pi} i_L(t) dt = \frac{\omega_0}{2\pi} \int_0^{2\pi} i_s(t) dt \quad (11)$$

$$P_{Loss} = \frac{\omega_0}{2\pi} \left(R_{on} \int_0^{2\pi} i_s^2(t) dt + r_L \int_0^{2\pi} i_L^2(t) dt \right) \quad (12)$$

For an ideal switch with $R_{on} = 0$ ($m = 0$) and an ideal dc-feed inductor with $Q_L \rightarrow \infty$, (12) reduces to the power loss due to discharging capacitor C :

$$P_{Loss}|_{m=0, Q_L \rightarrow \infty} = \frac{\frac{1}{2}C(\alpha V_{DD})^2}{\frac{2\pi}{\omega_0}} = \frac{\omega_0}{4\pi} C(\alpha V_{DD})^2 \quad (13)$$

Using (9) and (12) along with the definition of q and K_L in Table I, K_L can be obtained as

$$K_L = \frac{\pi m p^2 q^2 / \omega_0}{\int_0^{2\pi} \frac{v_{C,on}(t)}{V_{DD}} - \left(\frac{v_{C,on}(t)}{V_{DD}} \right)^2 dt - \int_0^{2\pi} r_L R_{on} \left(\frac{i_L(t)}{V_{DD}} \right)^2 dt} \quad (14)$$

where $v_{C,on}(t) = R_{on} \cdot i_s(t)$ is the switch voltage during the on-state and i_L is the supply current, shown in Fig. 1. Equation (14) can be explicitly rewritten into $K_L(q, d, m, Q_L, \alpha, \beta)$. K_C can then readily be derived from the definition of q as

$$K_C(q, d, m, Q_L, \alpha, \beta) = \frac{1}{q^2 K_L(q, d, m, Q_L, \alpha, \beta)}. \quad (15)$$

Substituting $I_R = \sqrt{\frac{2P_{out}}{R}}$ into (6) then yields

$$K_P(q, d, m, Q_L, \alpha, \beta) = \frac{p^2(q, d, m, Q_L, \alpha, \beta)}{2K_L^2(q, d, m, Q_L, \alpha, \beta)} \quad (16)$$

K_X was derived in [13] as

$$K_X = \frac{V_X}{V_R} \quad (17)$$

where V_X and V_R are two quadrature Fourier components of the switch voltage. Following a similar approach as in [13] yields an expression for K_X that depends only on K-design set parameters.

B. Waveform maxima

The switch current in the time interval of $0 < \omega_0 t < d\pi$ is obtained from $i_s(t) = \frac{v_{C,on}(t)}{R_{on}}$ where, $v_{C,on}$ is given in (7). The maximum switch current, I_{smax} , can be written as

$$I_{smax} = \frac{V_{DD}}{R_{on}} f_{I_1}(d, q, m, Q_L, \alpha, \beta) \quad (18)$$

where f_{I_1} is a function of K-design set parameters (not shown here for length reasons). Using (4), (5) and (6), (18) can be

rewritten as to obtain the maximum switch current normalized to I_0 :

$$\frac{I_{smax}}{I_0}(d, q, m, Q_L, \alpha, \beta) = \frac{f_{I_1}(d, q, m, Q_L, \alpha, \beta)}{m p q^2 f_{I_2}(d, q, m, Q_L, \alpha, \beta)} \quad (19)$$

where $f_{I_2} = \frac{I_0}{I_R}$ depends only on K-design set parameters and can be derived from (11) along with the definition of q and p which is not shown here for length reasons.

An expression for the switch voltage in the time interval of $0 < \omega_0 t < 2\pi$ is given in (7) and (8). Straightforward calculus yields the location of the maximum and the minimum of the switch voltage. The maximum and the minimum in the normalized switch voltage can then be written as a function of K-design set parameters which are not shown here again for length reasons.

C. Efficiency

The drain efficiency is given by $\eta = 1 - P_{Loss}/(V_{DD}I_0)$. Using (4), (6), (12) and $f_{I_2} = \frac{I_0}{I_R}$, this relation can be written as

$$\eta = 1 - \frac{\omega_0 \int_0^{2\pi} \left(\frac{V_{C,on}(t)}{V_{DD}} \right)^2 + r_L R_{on} \left(\frac{i_L(t)}{V_{DD}} \right)^2 dt}{2\pi m p q^2 f_{I_2}(d, q, m, Q_L, \alpha, \beta)} \quad (20)$$

which only depends on the K-design set parameters. For an ideal switch, with $R_{on} = 0$, and an ideal dc-feed inductor, with $Q_L \rightarrow \infty$, (20) can be simplified to

$$\eta = 1 - \frac{\alpha^2}{8\pi p q^2 \left(\frac{\pi d^2}{8p} - \frac{d}{4} \sin(\varphi) + \frac{\cos(\varphi) - \cos(d\pi + \varphi)}{4\pi} \right) + \alpha + \pi \beta d} \quad (21)$$

D. Non-ZVS and non-ZSS class-E summary

The previous 3 subsections showed that the performance of class-E PAs is affected by K-design set parameters d, q, m, Q_L, α and β . Parameters d, q, m and Q_L are typically fixed by design, as are parameters α and β assuming the nominal load impedance. Due to load impedance (antenna) mismatch, parameters α and β change which in effect will deterministically change the performance of the class-E PA according to the relations listed in the previous 3 subsections. In depth analyses of these load-pull effects for class-E PAs are described in the next section.

IV. ANTENNA LOAD-MISMATCH EFFECTS ON CLASS-E PERFORMANCE

A. Effects on PA load

Without loss of generality, we assume a class-E PA that is designed for a certain set of nominal conditions ($\alpha = \alpha_{nom}$ and $\beta = \beta_{nom}$) with arbitrary d, q, m and Q_L . For this class-E PA, there is a specific nominal K design-set with elements $K_{L,nom} = \frac{L\omega_0}{R}$, $K_{C,nom} = \omega_0 RC$, $K_{X,nom} = \frac{X}{R}$ and $K_{P,nom} = \frac{RP_{out,nom}}{V_{DD}^2}$ where $Z_{nom} = R + jX$ is the nominal load impedance for the nominal output power $P_{out,nom}$ with nominal efficiency η_{nom} .

Fig. 2. A lossless reciprocal matching network transforms the antenna impedance Z_A , represented by its nominal value $Z_{A,nom} = 50 \Omega$ to the PA load Z , represented by its nominal value $Z_{nom} = R + jX$.

This nominal load impedance Z_{nom} is typically transformed into a nominal $Z_{A,nom} = 50 \Omega$ antenna impedance using a matching network, see e.g. Fig. 2. For simplicity reasons, in this paper a lossless reciprocal matching network is assumed. The reflection coefficient at the antenna feed point due to changing antenna impedance is then $\Gamma_{Z_A} = \frac{Z_A - Z_{A,nom}}{Z_A + Z_{A,nom}}$. Any mismatch at the antenna (cross section AA in Fig. 2) will change the PA load Z . For normalization purposes, we rewrite Z as

$$Z = kR + j(X + k'R) \quad (22)$$

where $k > 0$ and k' are two real numbers and for the nominal load condition $k = 1$ and $k' = 0$ ($Z = Z_{nom} = R + jX$). We introduce an impedance Z' at cross sections BB in Fig. 2:

$$Z' = Z - jX \quad (23)$$

$$\Gamma_{Z'} = \frac{Z' - R}{Z' + R} \quad (24)$$

For lossless reciprocal matching networks it can be shown, e.g. [32], that

$$|\Gamma_{Z'}| = |\Gamma_{Z_A}|. \quad (25)$$

Note that this relation implies that — after renormalization of the reference impedance from $Z_{A,nom}$ at the antenna plane to R at cross section BB in Fig. 2 — each constant- $|\Gamma_{Z_A}|$ circle maps onto a constant- $|\Gamma_{Z'}|$ circle with the same radius in a Smith-chart.

Using (23), (24) and (25) along with the definition of VSWR at cross section AA in Fig. 2 as $\text{VSWR}_{Z_A} = \frac{1 + |\Gamma_{Z_A}|}{1 - |\Gamma_{Z_A}|}$,

$$\text{VSWR}_{Z_A} = \frac{\sqrt{(k+1)^2 + k'^2} + \sqrt{(k-1)^2 + k'^2}}{\sqrt{(k+1)^2 + k'^2} - \sqrt{(k-1)^2 + k'^2}} \quad (26)$$

For any positive real number a , the range of k and k' ($k - k'$ surface) and as a result the range of the PA loads Z for which $\text{VSWR}_{Z_A} \leq a$ follows straightforwardly from (26).

B. K-design set

The load impedance seen by the class-E PA is defined in (22). The values of the K-design set elements under mismatch

conditions, K_L , K_C , K_X , K_P , can now be calculated as a function of k and k' (and hence VSWR_{Z_A}) as follows

$$K_L = \frac{L\omega_0}{\text{Re}(Z)} = \frac{L\omega_0}{kR} = \frac{K_{L,nom}}{k} \quad (27)$$

$$K_C = \omega_0 \text{Re}(Z)C = k\omega_0 RC = kK_{C,nom} \quad (28)$$

$$K_X = \frac{\text{Im}(Z)}{\text{Re}(Z)} = \frac{X + k'R}{kR} = \frac{K_{X,nom}}{k} + \frac{k'}{k} \quad (29)$$

$$K_P = \frac{\text{Re}(Z)P_{out}}{V_{DD}^2} = k \frac{P_{out}}{P_{out,nom}} K_{P,nom} \quad (30)$$

where P_{out} and $P_{out,nom}$ are the output power under mismatch and nominal conditions, respectively. The values of α and β corresponding to this K-design set under mismatch conditions determine the performance of the PA with load-mismatch. With the above equations, these α and β are functions of k and k' and can be calculated from e.g. (27) and (29) by solving

$$K_L(q, d, m, Q_L, \alpha, \beta) = \frac{K_{L,nom}}{k} \quad (31)$$

$$K_X(q, d, m, Q_L, \alpha, \beta) = \frac{K_{X,nom}}{k} + \frac{k'}{k} \quad (32)$$

where the K-design set equations are summarized in the previous section. Having the values of α and β , all performance parameters of the PA are known. Hence, for a specific range of antenna load impedances, properties such as output power, efficiency and maximum switch voltage and current follow.

C. Case study: high power, high efficiency Class-E PA under antenna load-mismatch conditions

For high output power and high efficiency, a class-E PA is conventionally designed to have $q = 1.412$, 50% duty cycle ($d = 1$), ZVS ($\alpha = 0$) and ZSS ($\beta = 0$) [19]. We assume a lossless reciprocal matching network that matches the nominal load impedance for this PA to a nominal antenna impedance. The nominal K-design set elements and the nominal PA performance metrics $P_{out,nom}$, η_{nom} , the maximum switch voltage and the maximum switch current at nominal conditions are shown in Table II for two different values of switch on-resistance, as defined in (5), and Q_L . The performance of the class-E PAs for the two different switch on-resistances and two different Q_L s as listed in Table II are examined below.

Due to the complexity of the equations (31) and (32), a closed form equations for α and β are not derived in this work (if they can be derived at all). Instead, for the design parameters in Table II, we use graphical representations and discuss the effect of the parameters m and Q_L . Using a numerical solver to solve (31) and (32), constant α and β contours for $\text{VSWR}_{Z_A} < 20$ are shown in Fig. 3 where each Smith chart corresponds to a different value for m and Q_L . In all Smith charts, the center points correspond to the nominal load impedance and (for this case study) to $\alpha = \beta = 0$. For illustration purposes, the circles for $\text{VSWR}_{Z_A} = 2$, $\text{VSWR}_{Z_A} = 5$, $\text{VSWR}_{Z_A} = 10$ and $\text{VSWR}_{Z_A} = 20$ are also shown in Fig. 3.

Fig. 3 shows that for a loss-less switch and $Q_L \rightarrow \infty$ the value of α can change between -7 and 7 for $\text{VSWR}_{Z_A} \leq 10$,

TABLE II
DESIGN PARAMETERS AND PERFORMANCE METRICS FOR DIFFERENT SWITCH ON-RESISTANCES AND Q_L S.

	$m = 0$	$m = 0.05$	$m = 0.05$
	$Q_L \rightarrow \infty$	$Q_L \rightarrow \infty$	$Q_L = 25$
$K_{L_{nom}}$	0.73	0.7	0.65
$K_{C_{nom}}$	0.68	0.72	0.77
$K_{X_{nom}}$	0	0.09	0.11
$K_{P_{nom}}$	1.36	0.977	0.91
η_{nom}	100%	80.3%	72.8%
$\frac{V_{C_{max,nom}}}{V_{DD}}$	3.65	3.29	3.18
$\frac{I_{s_{max,nom}}}{I_{0,nom}}$	2.65	2.68	2.69

Fig. 3. Constant α (black) and β (grey) contours for the different values of m and Q_L in the $\Gamma_{Z'}$ plane (cross section BB in Fig. 2).

while the value of β is in the range of -2.3 to 21. This implies that ZVS and ZSS conditions are heavily violated with increasing $VSWR_{ZA}$. With increasing the switch loss (increasing m) and dc-inductor loss (reducing Q_L) the ranges of α and β reduce.

Below, the effect of load-mismatch on output power, efficiency and maximum switch voltage and current are presented. This is done using the theory in the previous sections that assumes a loaded $Q_{loaded} \rightarrow \infty$, and is backed up by circuit simulations using ideal components where we used a simple LC filter (L_0 and C_0 in Fig.1(a)) at the output with $Q_{loaded} = 5$ to demonstrate the effect of a limited loaded Q filter. At much higher Q_{loaded} , simulation results and theoretical results match exactly.

In the simulations, a simple series RLC network was used

TABLE III
COMPONENTS VALUES AND SIMULATED OUTPUT POWER FOR $q = 1.412$, $d = 1$, $R = 20 \Omega$, $V_{DD} = 1.2$ V AND $\frac{\omega_0}{2\pi} = 1.4$ GHz.

	L	C	X	R_{on}	$P_{out,nom}$
$m = 0, Q_L \rightarrow \infty$	1.7 nH	3.9 pF	0	0	19.9 dBm
$m = 0.05, Q_L \rightarrow \infty$	1.6 nH	4.1 pF	0.2 nH	1.4 Ω	18.5 dBm
$m = 0.05, Q_L = 25$	1.5 nH	4.4 pF	0.25 nH	1.3 Ω	18.2 dBm

to create the load-mismatch for the PA. Then, in the equation $Z' = kR + jk'R$, given by (23), for any load-mismatch (any k and k') the real part of the PA load at all harmonics of the operating frequency is the same while for the inductive (capacitive) mismatch, the imaginary part of the load scales up by n (down by n) at the n^{th} harmonic. Appendix A deals with the effect of PA impedance at the harmonics of the operating frequency on the PA performance in more detail.

Components values, shown in Fig. 1, are calculated according to K-design set elements in Table II for $R = 20 \Omega$, $V_{DD} = 1.2$ V and $\frac{\omega_0}{2\pi} = 1.4$ GHz and are listed in Table III.

1) *Output power*: Using (30), the output power of the PA under load-mismatch conditions normalized to $P_{out,nom}$ is

$$\frac{P_{out}}{P_{out,nom}} = \frac{1}{k} \frac{K_P}{K_{P_{nom}}} \quad (33)$$

With (22) and (26), load-pull output power contours can be derived; these contours are shown in Fig. 4 with solid lines for two values of m and Q_L . Fig. 4(a) shows that for a lossless switch ($m = 0$) and ideal dc-feed inductor, for $VSWR_{ZA}$ up to 10 the output power can change by almost ± 10 dB. Increasing m from 0 to 0.05, Fig. 4(b), for $Q_L \rightarrow \infty$ changes this variation from about -8.5 dB to +2.4 dB. Reducing Q_L to 25 further reduces this range (Fig. 4(c)). Simulation results with ideal components and assuming $Q_{loaded} = 5$ for the nominal load impedance are shown in Fig. 4 with dashed lines. Note that e.g. at the right hand side of the Smith charts the Q_{loaded} is much lower than in the nominal case. Fig. 4 demonstrates good agreement between the theory and the simulation results.

2) *Efficiency*: Load-pull power efficiency contours obtained from (20) are shown in Fig. 4(d-f) by solid curves. It can be seen that power efficiency drops from 100% to about 35% for $m = 0$, $Q_L \rightarrow \infty$ and $VSWR_{ZA} = 10$. The power efficiency reduction using a lossy switch can be even worse: for $VSWR_{ZA} = 10$ and $m = 0.05$ the efficiency can be reduced to less than 25%.

Two important observation can be made from Fig. 3 and 4. Firstly, the load-pull contour for $\alpha = 0$ shows that it is possible to sweep output power while keeping the efficiency high (100% in case of a lossless switch and an ideal dc-feed inductor). Secondly, ZVS and ZSS conditions do not necessarily provide maximum efficiency in case of a lossy switch [12]. Fig. 4(e) shows that by choosing the right values for α and β for $m = 0.05$ and $Q_L \rightarrow \infty$, the power efficiency can be increased up to 88% where the efficiency is about 80% under ZVS and ZSS conditions.

Fig. 4. Load-pull contours for output power normalized to nominal condition (a-c) and efficiency (d-f), for different values of m and Q_L in the $\Gamma_{Z'}$ plane.

Fig. 4(e) and (f) show that reducing Q_L from ∞ to 25 reduces the efficiency for the both nominal and non-nominal loads; for $m = 0.05$ and the nominal load, efficiency is reduced from 80.3% to 72.8%. Having the load-pull contours for the output power, shown in Fig. 4(b) and (c), on top of the corresponding efficiency contours, shown in Fig. 4(e) and (f), shows that at 10 dB back-off, more than 80% efficiency can be obtained for $Q_L \rightarrow \infty$ while $Q_L = 25$ reduces the 10 dB back-off efficiency to slightly more than 40%.

Simulation results with ideal components and $Q_{\text{loaded}} = 5$ under nominal load condition are also shown in Fig. 4(d-f) with dashed curves. At the right hand side of the Smith charts the Q_{loaded} is much lower than in the nominal case, which yields significant transmission of higher harmonics. Because power efficiency is derived for the fundamental harmonic, there the power efficiency decreases with lower Q_{loaded} . For example for $m = 0$ and load-mismatch $\Gamma' = 0.82$ ($\text{VSWR}_{Z_A} = 10$) the calculated and simulated efficiencies are 66% and 56%, respectively. For $Q_{\text{loaded}} = 10$ the power

Fig. 5. Maximum switch voltage of class-E PA normalized to V_{DD} for different values of m and Q_L in the $\Gamma_{Z'}$ plane.

transmission at the second and third harmonics is lower and the simulated efficiency increases to 60% and for $Q_{\text{loaded}} \rightarrow \infty$ the simulated efficiency approaches the calculated 66% efficiency.

3) *Maximum and minimum switch voltage:* When the switch is off ($d\pi < \omega_0 t < 2\pi$), the maximum switch voltage contours² are shown in Fig. 5. For $\text{VSWR} = 10$, $Q_L \rightarrow \infty$ and $m = 0$, the switch voltage increases from nominally $3.65V_{DD}$ up to $13V_{DD}$. A lossy inductor and/or a lossy switch reduces this high maximum voltage (at the cost of power and efficiency); with $Q_L = 25$ and $m = 0.05$, the switch voltage increases up to (slightly more than) $5V_{DD}$ for $\text{VSWR} = 10$. Calculated time domain switch voltage waveforms for three different cases are also shown in Fig. 5. Simulation results assuming a nominal $Q_{\text{loaded}} = 5$ are represented by dashed curves in Fig. 5: using $Q_{\text{loaded}} = 5$ slightly increases the maximum switch voltage compared to using $Q_{\text{loaded}} \rightarrow \infty$.

Fig. 5 also shows that for some load impedance ranges, the switch voltage reaches negative values (up to $-10V_{DD}$ for $m = 0$). The theoretical and simulated minimum switch voltage for 2 different cases are shown in Fig. 6. In circuit implementations, this may e.g. forward bias parasitic diodes which in turn may inject current into the substrate, yields significant gradients in the substrate potential across the chip and yielding latch up risks that may destroy the PA operation [33], [34] when improperly handled. Circuit solutions such as used in e.g. [35] may be used to reliably handle these large negative voltages at the cost of circuit complexity and power efficiency. Section VI deals in more detail with the effects of (unintentionally - due to load-mismatch) forward biasing of e.g. parasitic diodes on the behavior of SMPAs.

4) *Maximum and average switch current:* When the switch is on ($0 < \omega_0 t < d\pi$), the maximum switch current normalized

²It is a common practice to normalize maximum switch voltage to the supply voltage V_{DD} .

Fig. 6. Minimum switch voltage of class-E PA normalized to V_{DD} for different values of m and Q_L in the $\Gamma_{Z'}$ plane.

to the maximum switch current at nominal load condition³ can be written as

$$\frac{I_{smax}}{I_{smax,nom}} = \frac{\frac{I_{smax}}{I_0}}{\frac{I_{smax,nom}}{I_{0,nom}}} \frac{I_0}{I_{0,nom}}. \quad (34)$$

In (34), $\frac{I_{smax}}{I_0}$ under mismatch conditions follows from (19), $\frac{I_{smax,nom}}{I_{0,nom}}$ is listed in Table II and $\frac{I_0}{I_{0,nom}}$ is the ratio of the average switch/supply current (note that $\langle i_s(t) \rangle = \langle i_L(t) \rangle = I_0$) under mismatch conditions to that at the nominal load condition. Using $\eta = \frac{P_{out}}{V_{DD}I_0}$ it follows that

$$\frac{I_0}{I_{0,nom}} = \frac{P_{out}}{P_{out,nom}} \frac{\eta_{nom}}{\eta} \quad (35)$$

The $\frac{I_{smax}}{I_{smax,nom}}$ load-pull contours using (34) and (35) are shown in Fig. 7. For small m and non-zero voltage switching ($\alpha \neq 0$), the maximum current occurs at $t = 0^+$. Fig. 7(a) shows the maximum switch current neglecting current spikes at the switching moment. Antenna load-mismatch with VSWR = 10, can increase the maximum switch current up to (almost) 3 times that under nominal load conditions. This ratio increases for a higher Q_L or a lower m ; up to 9 times for $m = 0$ and $Q_L \rightarrow \infty$. The normalized current spike at switching, in Fig. 7(b), shows that for $m = 0.05$ and $Q_L = 25$ the switching moment current can be 15 times as high as the maximum switch current in the nominal load condition. This ratio can be even higher for smaller values of m . Simulation results with $Q_{loaded} = 5$ under nominal load condition are shown in Fig. 7 as dashed curves.

The load-pull contours for the average switch/supply current under load-mismatch conditions normalized to that under nominal conditions are obtained from (35) and shown in Fig. 8 for $m = 0.05$ and $Q_L = 25$. The difference between the theoretical results and the simulation results at the right hand side of the Smith chart is due to the much lower Q_{loaded} at this region of the Smith chart compared to the nominal load condition. It can be seen that toward the left side of the Smith chart, the average switch/supply current increases. For $m = 0$ and $Q_L \rightarrow \infty$, the ratio can be up to 10 for VSWR = 10.

³To keep the analysis independent from the output power, the maximum switch current is normalized to that at nominal load condition.

Fig. 7. (a) Maximum switch current of class-E PA, neglecting the switching moment, normalized to nominal condition. (b) Switching moment current normalized to the maximum switch current at nominal condition. For both plots $m = 0.05$ and $Q_L = 25$.

Fig. 8. Average switch/supply current of class-E PA normalized to that at nominal load condition for $m = 0.05$ and $Q_L = 25$.

V. RELIABILITY ISSUES AND SAFE OPERATING REGION

For a transistor operating in a class-E PA and designed to marginally handle the nominal switch voltage and switch current, high voltage or current stress will drastically reduce the life time [36]. Figs. 5 and 7 already showed that under load-mismatch conditions both the switch voltage and switch current can increase significantly with respect to the nominal load condition. A discussion into reliability and safe operating areas for class-E PAs is shown below.

Two load-pull contours both of maximum switch voltage normalized to V_{DD} and of maximum switch current normalized to that at nominal load condition are shown in Fig. 9 with solid and dashed lines, respectively. For this plot, it is assumed that the nominal PA is designed to have $q = 1.412$, $d = 1$, $m = 0$, $Q_L \rightarrow \infty$ and $\alpha = \beta = 0$, similar to the case study in section IV-C. Fig. 9 also shows two greyed regions. The inner (light grey) region is bounded by the $V_{cmax} = 3.65V_{DD}$ contour and the $I_{smax} = I_{smax,nom}$ contour; this region represents the impedances for which the maximum switch voltage and current are lower than those for the nominal load, corresponding to the safe operating region with 0% design margin. Adding 10% margin in both V_{cmax} and I_{smax} adds

the dark grey region to the previously described safe operating region for 0% design margin. To prevent device performance degradation and life time issues, the impedance outside of the greyed areas should be avoided. Since the switch current at the switching moment depends heavily on the technology used and on the exact waveform of the driving voltage, it is not taken into account for the safe operating region, otherwise the safe operating region would have been smaller. Including the switch conduction loss (non-zero m) and dc-feed inductor loss (limited Q_L), the safe operating region can be extended at the cost of output power and efficiency, as discussed in section IV.

Fig. 9. Solid contours show maximum switch voltage normalized to V_{DD} and dashed contours show maximum switch current normalized to that at the nominal condition (for $m = 0$ and $Q_L \rightarrow \infty$). The light grey area denotes the safe operating region with 0% safety margin. The dark grey area corresponds to the extra safe operating region for 10% design margin.

The performance and the reliability related parameters of class-E PAs under load-mismatch conditions were shown for $q = 1.412$ and $d = 1$. It is possible to adjust duty cycle d or parameter q to satisfy ZVS and/or ZSS conditions at different frequencies [37] or at different output power levels [29]. The next section shows the effect of load-mismatch for different duty cycles and a short discussion on the effects of different q parameter.

A. Effects of the parameters d and q

Output power and efficiency contours for a class-E PA (which is initially designed) for $d = 0.75$ and $d = 1.4$ are shown in Fig. 10, for $q = 1.412$. The corresponding load-pull contours for a 50% duty cycle ($d = 1$) were shown in Fig. 4. In Fig. 10 it is assumed that $m = 0$, $Q_L \rightarrow \infty$ and that $\alpha = \beta = 0$ for the nominal load condition.

It can be seen that the shape of the power and efficiency contours is not much affected by the value of d but that the contours do rotate counterclockwise for increasing d . Simulation results with $Q_{\text{loaded}} = 5$ for the nominal load impedance are shown as dashed curves in Fig. 10. The relatively large differences between theory ($Q_{\text{loaded}} \rightarrow \infty$) and the simulations are due to a significant dependency of the harmonic content in the output signal to the load impedance (At much higher Q_{loaded} , simulation results and theoretical results match exactly). An in-depth analysis is not provided here for length reasons.

Fig. 11 shows the maximum normalized switch voltage and current for $d = 0.75$ and $d = 1.4$; the corresponding load-pull plots for $d = 1$ are shown in Fig. 5 and Fig. 7 respectively.

Fig. 10. (a,c) Normalized output power contours and (b,d) power efficiency contours for $d = 0.75$ and $d = 1.4$. The switch and the dc-feed inductor are ideal.

Fig. 11. (a,c) Maximum switch voltage normalized to V_{DD} and (b,d) maximum switch current normalized to that at nominal condition for $d = 0.75$ and $d = 1.4$. The switch is ideal ($m=0$) and $Q_L \rightarrow \infty$. The light grey area denotes the safe operating region with 0% safety margin. The dark grey area corresponds to the extra safe operating region for 10% design margin.

The grey areas again denote the safe operating regions with 0% (light grey) and 10% (light grey + dark grey) safety margin, that are enclosed by the corresponding maximum voltage and current contours. It can be seen that a higher d reduces the

safe operating region and rotates it counterclockwise.

Similar contours can be plotted for different values of q . It can be shown that the shape of the contours hardly changes except for a rotation: clockwise rotation for higher q [18]. These contours are not shown here for the length reason.

VI. IMPACT OF NON-IDEAL EFFECTS

The previous section presented load-pull analyses and the impact of load-mismatch on output power, efficiency and reliability, primarily from a mathematical point of view; these theoretical findings are exact for a loaded $Q_{\text{loaded}} \rightarrow \infty$. These theoretical findings were backed up by simulations that assumed a $Q_{\text{loaded}} = 5$ for nominal load condition, already showing the impact of finite Q_{loaded} . Other non-idealities that were already included were non-zero switch on-resistance, modelled by $m \neq 0$ and non-ideal dc-feed inductor, modelled by a limited Q_L . In this section, we briefly analyze the main remaining non-idealities from a load-mismatch point of view: a) reverse conduction of the switch (or shunting negative voltage excursions across the switch), b) load dependent switch conduction loss (m).

A. Shunting negative voltage excursions across the switch

To show the impact of the limitation of the negative excursion of the switch voltage, let us assume a class-E PA with ideal switch ($m=0$) and ideal dc-feed inductor that was studied in section IV.C. Fig. 6(a) shows load-pull contours for the minimum switch voltage. It can be seen that in theory the switch voltage can go to large negative values: e.g. to $-8V_{DD}$ for load-mismatch $\Gamma' = 0.82 \angle 151^\circ$ when $m = 0$ and $Q_L \rightarrow \infty$.

In actual circuit implementations, large negative voltage excursions across the switch transistor usually cannot occur due to two effects. Firstly, the parasitic diode across the switch (e.g. the drain-bulk diode in bulk CMOS technologies), such as shown in Fig. 12(a), is in forward for sufficiently negative voltages. Secondly, for sufficiently negative switch voltages the switch transistors typically goes into conduction forming e.g. a MOS diode for MOS switches (with source and drain interchanged). Both of these diodes can limit negative voltage excursions; usually one of the two is dominant (depending on V_{th}). The work in [15] explicitly adds an anti-parallel diode to prevent negative voltage excursions across the switch (at the switching moment) aiming to have (ideally) zero switching loss ($\alpha = 0$) under specific (real) PA load variations.

Assuming that the negative voltage excursions are hard-limited to e.g. $-0.5V_{DD}$ by one of the limiting mechanisms described above, the simulated switch voltage, with and without the limited negative voltage excursions (WLNE and WoLNE, respectively), for two load-mismatches $\Gamma' = 0.82 \angle 90^\circ$ and $\Gamma' = 0.82 \angle 151^\circ$ are shown in Fig. 12(b) and Fig. 12(c), respectively. In these figures, also output power levels and efficiencies are reported for the 4 cases. Three observations can be made. Firstly, the limitation on the negative voltage increases the effective duty cycle. Secondly, this can either reduce or increase power efficiency. Increased efficiency is due to reduced switching loss (smaller α) while

Fig. 12. (a) Switch model for positive and negative voltages. (b,c) Switch voltage, output power and efficiency for two different load-mismatches with limited negative excursions (WLNE) and without limited negative excursions (WoLNE).

the efficiency reduction results from conduction loss in the diode. Thirdly, the maximum switch voltage and output power (and therefore switch current) are influenced.

B. Load dependent switch conduction loss (m)

To simplify the analyses in sections III and IV, the switch conduction loss was assumed to be constant during the time period that the switch was closed. In section III, the switch current was shown to depend on the switching conditions (and as a result on the PA load). Also, in Fig. 8, the average switch current under load-mismatch conditions normalized to that at nominal load condition was shown to be load-dependent. This load-dependent average switch current results in a load-dependent average switch voltage across the switch during the time period that the switch is closed ($< v_{C,on} >$). Implemented by (MOS) transistors, the average switch on-resistance depends on both the drive (gate-source) voltage as well as on the switch on-voltage (drain-source voltage) [33]. Therefore, the switch on-resistance changes under load-mismatch.

For switches that employ a cascode structure with a fixed gate bias for the cascode device, the switch on-resistance change can be severe. In this case the increased average switch on-voltage of the bottom transistor reduces the average gate-source voltage of the cascode device which increases the average switch on-resistance. Accurate modeling of the average switch on-resistance is beyond the scope of this paper. However, for the switch we implemented, see section VII, the average switch on-resistance is estimated for different PA loads from circuit simulations.

C. Load-pull contours

Now, combining these findings with the results from sections IV and V-A yields the effect of load variations on SMPA behavior from a theoretical point of view, including shunting negative voltage excursions and including the load-dependent m . For that purpose, the simplified model shown in Fig. 1(a) is considered with $d = 1$ and $m = 0.05$ for nominal conditions as starting point. Then, the effective duty cycle and the effective m are estimated by fitting the load-pull simulations of the implemented PA in 65 nm CMOS technology to the corresponding theoretical counterparts resulting from our model; for a limited yet enough number of PA loads, the parameters m (in the range of 0.05 to 0.1 with 0.005 step) and d (in the range of 1 to 1.4 with 0.025 step) were adjusted in our theoretical plots to have the best match between the simulated performance metrics (power and efficiency) and reliability related metrics (switch voltage waveform) of the implemented PA and these metrics as resulting from the theory. The resulting effective d and m contours are shown in Fig. 13(a) and (b), respectively.

In Fig. 13(a), it was assumed that the negative voltage excursions are hard-limited to e.g. $-0.5V_{DD}$ (corresponding to the contour $d_{\text{eff}} = 1$). In the lower part of the Smith chart (below the contour $d_{\text{eff}} = 1$), the minimum switch voltage is higher than $-0.5V_{DD}$ and hence the effective duty cycle is equal to the nominal duty cycle $d = 1$. Towards the upper left corner on the Smith chart, the switch voltage tends to go more negative, see Fig. 6, resulting in the effective d contours in Fig. 13(a). With the results from section V-A, this yields anti-clockwise rotation of power, efficiency and maximum voltage and current contours in only the parts on Smith chart where $d_{\text{eff}} > 1$.

The effective m contours are shown in Fig. 13(b). Toward the upper and left side of the Smith chart the effective m increases due to increased losses with longer forward biasing of the parasitic diode (or reverse conduction of the switch with a higher loss in reverse mode) and increased average switch current, shown in Fig. 8. At the right and lower part of the Smith chart (below the contour $m_{\text{eff}} = 0.05$), the effective m is equal to its nominal value $m = 0.05$.

These effective d and m contours yield the load-pull plots in Fig. 13(c-f). In the load-pull plots, the solid curves are for the SMPA including the limited negative voltage and the load-dependent m ; the dotted contours assume fixed parameters $d = 1$ and $m = 0.05$ for all the PA loads, already shown in section IV.C. Fig. 13(c) and (d) show that, toward the upper left corner of the Smith chart, the power contours with considering the limited negative voltage rotate in counter-clockwise direction and the efficiency is higher than for the case that $d = 1$ and $m = 0.05$. Toward the left side of the Smith chart, the increased switch condition loss reduces the output power as well as the efficiency compared to case where m is fixed at 0.05.

Fig. 13(e) and (f) show that the anti-clockwise rotation of the contours reduces both the maximum switch voltage and the average current toward the upper left corner on the Smith chart which results in an extended safe operating region. Also, the reduced maximum switch voltage at the left side of the

Fig. 13. Load-pull contours with (solid contours) and without (dotted contours) taking the limited negative voltage and load-dependent m effects into account: (a) estimated d when negative switch voltage is hard-limited to $-0.5V_{DD}$, (b) estimated m , (c) normalized output power, (d) efficiency, (e) maximum switch voltage normalized to V_{DD} , (f) average switch/supply current normalized to that under nominal condition.

Smith chart for solid contours is due to the increased switch conduction loss. Since, in the simulation of the implemented class-E PA as well as in the measurements, distinguishing between resistive and capacitive current of the switch is not possible, no contours for the maximum switch current are shown.

VII. MEASUREMENTS

Finally, to show the correspondence between theoretical findings, simulations of idealized SMPAs and measurements of an actual SMPA, this section presents measurement results of a circuit implemented in a standard 65 nm CMOS technology. The schematic of the class-E PA and driver⁴ stage are shown in Fig. 14. The switch is implemented as a cascode structure employing a 1.2 V device as the switch transistor and a thick oxide 2.5 V device as the cascode allowing switch voltages

⁴Using two cascaded inverters as the driver stage, the input matching is fairly isolated from the output mismatch effects.

Fig. 14. (a) Schematic of the designed PA, the driver stage, matching network and measurement setup. (b) All PA load settings for the measurements at cross sections AA and BB at 1.4GHz.

up to 4 V. The PA is designed for $q = 1.412$, $d = 1$ and $\alpha = \beta = 0$ under nominal load condition $R_L = 20 \Omega$. The feed inductance $L \approx 1.5$ nH (see Table III) is implemented by 2 parallel bond-wires to provide a high quality factor ($Q_L \approx 25$). The tank capacitance $C \approx 4.4$ pF at the switching node was implemented with the drain-bulk and gate-drain capacitances of the NMOS transistor. Also, a switch-capacitor network was added to the switching node to (fine) tune the drain capacitance to the required value. The output filter (L_0 - C_0) and the matching network (L_m - C_m) are implemented on the PCB; the total required inductance $L_0 + L_m \approx 14$ nH is partly implemented by bond-wire inductances and partly by an off-chip discrete component. The matching network steps the 50 Ω antenna load down to 20 Ω . The output filter provides a loaded quality factor $Q_{loaded} \approx 5$ under nominal load condition. The output of the matching network is connected to a Maury load tuner, capable of providing VSWR up to 40 at cross section AA. Due to the loss of the connector cable, the matching network and the output filter, the VSWR is limited at cross section BB to 6.15 and 10 at the left and right hand sides of the Smith chart, respectively. All PA load settings for the measurements at cross section BB, are shown in Fig. 14. For each of these settings the output power, efficiency and time domain switch voltage are measured. Our presented load-pull contours are based (interpolated) on these settings.

Measured load-pull contours for normalized output power are shown in Fig. 15(a) together with theoretical contours for $m = 0.05$ and $Q_L = 25$ (with taking the limited negative voltage and the load-dependent m effects into account). Under nominal load condition the PA provides 18.1 dBm output power from a 1.2 V supply voltage at 1.4 GHz. Under load-mismatch, a good agreement between theoretical output power contours and measurements can be seen. The small difference for high VSWRs is due to increased sensitivity of

the measurements to parasitics.

Measured efficiency contours are shown in Fig. 15(b). Deviation of the measured contours from theoretical contours at the right hand side of the Smith chart is mainly due to the limited loaded quality factor of the output filter (see appendix A) which reduces the efficiency and also due to increased sensitivity of the measurements to parasitics at high VSWRs. However, the proposed theory can (quite) accurately predict the behavior of the class-E PA under load-mismatch.

Measured normalized switch voltage contours are shown in Fig. 15(c). The transient waveforms were measured using an N2803A active probe and a 80 GSa/s Agilent Oscilloscope. The inset at the right upper corner is measured under nominal load condition. Ignoring transient response of the probe, we have $\alpha \approx 0$ and $\beta \approx 0$. For this nominal load, the maximum normalized switch voltage is (almost) $3.4V_{DD}$ which results in ≈ 4 V maximum switch voltage for the 1.2 V supply voltage. Measured time domain voltage of the switch for four non-nominal loads are also shown in Fig. 15(c). In the lower part of the Smith chart α is positive and increases toward lower left corner. In the upper side of the Smith chart α is negative and reduces toward the left hand side; however reverse conduction in the switch limits the negative switch voltage. Because of the limited Q_{loaded} , the measured maximum switch voltage is slightly higher than the theoretical values but the theoretical model still is capable of predicting the behavior of the PA under load-mismatch. To prevent switch degradation (or break down) during measurements, the supply voltage was always tuned to have a maximum switch voltage 4 V for reliability and (hence) for reproducibility reasons. In post processing the measurements data, the V_{DD} was scaled to the 1.2 nominal value and it was assumed that $P_{out} \propto V_{DD}^2$ which is according to the theory.

Measured average supply/switch current contours are shown in Fig. 15(d). A good agreement between the measured contours and the theoretical counterparts can be seen. The chip photo and PCB are shown in Fig. 16.

VIII. CONCLUSIONS

Class-E PAs are typically designed for nominal conditions. However, e.g. antenna impedances are known to vary significantly due to changes in their EM-environment, leading to practical VSWR numbers which are high as 10:1. In this paper we presented mathematical load-pull analyses for class-E PAs complemented with simulations and measurements results.

It was shown that the performance of the PA as well as the reliability are heavily dependent on load-mismatch. This paper demonstrates that with load-mismatch, in large areas of the Smith chart the switch voltage and/or the switch current exceeds the nominal value which may cause serious reliability issues; the remaining area then is the class-E PA's safe operating area. Taking into account design margins to handle larger-than-nominal voltages and currents these safe operating areas on the Smith chart increase. Dependencies of the design set and safe operating area on the duty cycle d are also presented, giving e.g. options to rotate and extend the safe operating area on the Smith chart to adapt to the actual

Fig. 15. Measured load-pull contours at 1.4GHz (dotted contours) and theoretical contours (solid lines): (a) normalized output power, (b) efficiency, (c) maximum switch voltage normalized to V_{DD} and (d) average switch/supply current normalized to that under nominal condition.

Fig. 16. (a) Chip microphotograph. (b) Designed PCB setup.

load impedances. The theoretical findings were backed-up with circuit simulations including most common non-idealities of class-E PAs as well as load-pull measurements of a class-E

PA implemented in 65 nm CMOS technology at 1.4 GHz.

APPENDIX A EFFECT OF PA IMPEDANCE AT THE HARMONICS

The load tuner and the PA impedance settings at the fundamental harmonic were already shown in Fig. 14(b). In section IV.C a deterministic impedance at the harmonics of the operating frequency was assumed for each load-mismatch. However, measurements of the tuner impedance (at cross section AA in Fig. 14(a)) at the harmonics of the operating frequency reveal that for a mismatch with reflection coefficient amplitude $|\Gamma|$ at the fundamental harmonic, the amplitude of the reflection coefficient at the second and third harmonic can be in the range of $\leq |\Gamma|$. Assuming an arbitrary (and unknown) connection length (between the matching network and the antenna) $\angle \Gamma$ can be any arbitrary angle. Therefore, it would be more practical to assume that the PA load at second (and third) harmonic can occur at any place on the Smith chart. In our work the effects of the higher than third harmonic are negligible.

To examine the effects of the load current at the harmonics on the performance, we assume a load-mismatch $\Gamma = 0.82$ at the fundamental harmonic which is (close to) a worst case situation for sensitivity to harmonics among any mismatch yielding a VSWR ≤ 10 . Then, we sweep the PA impedance at the second and third harmonics across the Smith chart in the range $|\Gamma| \leq 0.9$ and then compare the simulated performance metrics with that of the calculated counterpart. For calculations (see section IV.C), an infinite Q_{loaded} was assumed (no load current at the harmonics). For simulations the circuit with the components (section IV.C) was employed. The loaded quality factor Q_{loaded} at the fundamental harmonic and for the nominal load was set to 5.

The results of these simulations (for the second harmonic) are shown in Fig. 17. Fig. 17(a), (b) and (c) show the relative error between the simulations and the theory for the output power, efficiency and normalized maximum switch voltage, respectively. The maximum relative error in the output power and the maximum switch voltage is 10% while the efficiency is more sensitive to the PA load at the second harmonic. It can be seen that maximum error occurs at the right lower corner on the Smith chart. In this region, the capacitive part of the load at the second harmonic nulls the effect of the inductive impedance of the series filter and as a result reduces the PA impedance at the second harmonic.

Changing the third harmonic for the same mismatch on the fundamental, similar plots can be obtained. The maximum relative errors on the output power, efficiency and the maximum switch voltage are lower than 1.5%. Similar plots can be generated for the other mismatches on the fundamental harmonic. For instance for the nominal load at the fundamental frequency, sweeping the PA load at the second harmonic in the range $|\Gamma| \leq 0.9$, results in atmost 8% error in the efficiency.

In conclusion, including harmonics in the load current would result in a much more complex model that adds a little accuracy in (especially) a few regions on the Smith chart. Such an extension of the model is, however, beyond the scope of this work.

Fig. 17. Relative error between the simulations and the theoretical results due to the PA load change at the second harmonic for the mismatch on the first harmonic with $\Gamma = 0.82$. (a) output power, (b) efficiency, (c) maximum switch voltage.

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