Molecular Monolayers for Doping Silicon:

From Doping Dose Control to Device Application

Liang Ye

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**MOLECULAR MONOLAYERS FOR DOPING
SILICON: FROM DOPING DOSE CONTROL TO
DEVICE APPLICATIONS**

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DISSERTATION

**to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
prof. dr. H. Brinksma,
on account of the decision of the graduation committee,
to be publicly defended
on Friday 15th of July, 2016 at 12.45h**

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Chapter 1

General introduction

1.1 Introduction

The semiconductor industry employs transistors that are made of a semiconductor material, predominantly silicon. The function of a transistor relies on the type of charge carriers, either electrons or holes, and their position and concentration in the device. Tuning the carrier type and amount in a semiconductor material can be realized by a process known as doping. By introducing impurities into the material either an excess of electrons or holes can be created in the material thus changing its electrical properties. Doping is one of the crucial steps in making electronic devices nowadays. The semiconductor industry predominantly relies on ion implantation to introduce dopants in silicon.

The advancement in semiconductor industry relies on the downscaling of devices towards nanometer dimensions for better performance and lower costs. In 1965 Gordon Moore predicted that the size of a transistor would shrink by half every 12 months.¹ Later on the time was adapted to 18 months. Since then the industry has been putting resources into research and development (R&D) to push the technology towards miniaturization at the pace set by Moore's law. In recent years, as the dimensions of the transistors pass sub-30 nm, technology challenges have arisen that prohibit the industry to keep up with this pace. For instance, according to the 2013 International Technology Roadmap for Semiconductors (ITRS)², for a 7 nm node, predicted to be reached in 2017, the junction depth X_j has to be 6.1 nm, but the technology to manufacture this is not yet available.

Alternatively, the industry is moving in recent years from a 2-D planar device architecture to 3-D to achieve better device performance. When focusing on doping,

it is difficult or impossible to achieve a homogeneous doping of 3-D structures by using the currently employed ion implantation, due to the structural damage caused by incident ions and by shadowing effects arising from the directional approach of the ions.

Monolayer doping (MLD) has been proposed by Javey *et al.*³ as an alternative to traditional doping techniques. This technique utilizes dopant-containing molecules, which are covalently bound to the silicon surface. This is followed by an annealing process to decompose the molecules and drive the dopants into the silicon. This results in a doped layer or junction at the silicon surface. The major advantage of MLD is that it is capable of ultra-shallow doping. A sub-5 nm junction has been demonstrated using MLD.⁴ Moreover, the technique avoids the crystal damage occurring during ion implantation and is capable of doping 3D structures without shadowing effects. Further developments to MLD have enhanced its capability of doping substrates in a versatile manner. Patterning techniques, such as nanoimprint lithography have been combined with the dopant monolayer formation to achieve localized doping by MLD.⁵

1.2 Aim of the research

In the research presented in this thesis, the versatility of MLD is extended by tuning the doping level using a variety of strategies. Being able to tune the doping level extends the potential of MLD in forming nanoscale devices. Furthermore, the fabrication of junction-less transistors using MLD is demonstrated, and a modified MLD process, namely monolayer contact doping (MLCD)⁶ using a different source monolayer, is explored as well in this research.

The thesis has been structured as follows:

In Chapter 2, a general review of the strategies that have been used to dope silicon is presented. The majority of the doping strategies can be divided into three categories: diffusion, implantation and in-situ incorporation of the dopants. These techniques, together with their advantages and limitations, are discussed.

Chapter 3 presents a method to tune the doping level in MLD by using mixed monolayers. The dopant adsorbate in MLD was mixed with an alkene molecule that lacks dopant atoms. By controlling the mixing ratio of the adsorbates, the doping level for both p- and n-type doping by MLD is tuned effectively. A variety of characterization techniques, including contact angle measurements, X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), and secondary ion mass spectrometry (SIMS), have been used to assess the tuning effects.

In Chapter 4, a carborane cluster was utilized as the dopant adsorbate to perform MLD. Each molecule in the carborane has ten boron atoms. This effectively boosts the boron doping level by 10 times. The relation between the resulting doping dose and the annealing conditions was investigated by evaluating the thermal budget of the annealing.

In Chapter 5, the MLD method has been utilized to fabricate bulk planar junctionless transistors (BP-JLTs). The challenge to fabricate BP-JLTs is the formation of an ultra-shallow doped layer on the silicon surface. This is achieved here by MLD. The formation of transistor devices was evidenced by various characterization techniques, and their properties were measured electrically to confirm the transistor functionality.

In Chapter 6, we modified the reported MLCD method for easier processing thus allowing the application of MLD on delicate device architectures. MLCD was first reported by Yerushalmi *et al.*⁶ and has been shown to dope silicon substrates without subjecting them to the wet chemistry involving MLD. This solves material

incompatibility issues on certain substrates, for example, when aiming for silicon devices on SOI wafers for which the use of fluoride etching is prohibited. We replaced the commonly used silicon source substrate by silicon dioxide and utilized the more accessible silane reaction to bond the dopant onto the silicon dioxide substrate. Characterization of the level of doping was performed, and compared to MLD on silicon. Moreover, the dopant concentrations on the source wafer is compared to that of the target after annealing. Furthermore, this modified MLCd method was applied to silicon nanowire devices to demonstrate the capability of doping delicate 3D nanostructures.

Finally, the main conclusions are described and an outlook for future research is given.

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Chapter 2

Doping of silicon

The semiconductor industry creates electronic devices fabricated on silicon wafers. Doping of silicon is one of the crucial steps to tune the electrical properties of the material. A great variety of doping techniques is available today. These techniques can be categorized into three major classes: diffusion, implantation, and in-situ incorporation of dopants. Over the past decades, these techniques have evolved to meet the increasing demands in semiconductor industry. For the down-scaling of electronic devices, shallower junctions with abrupt changes in dopant concentration are desired. And in photovoltaics emphasis is put on low costs, feasibility and scalability. In this chapter techniques for the doping of Si are reviewed and discussed.

2.1 Introduction

In the semiconductor industry, doping is the intentional introduction of impurities into the crystal lattice of a semiconductor material in order to tailor its electrical properties. Such impurities are also referred to as dopants. The dopant introduces additional electrical carriers, either holes or electrons, into the semiconductor material. Depending on the resulting majority type of carrier in silicon, holes or electrons, the dopant can be categorized as p-type or n-type, respectively. The most common p-type dopants for silicon are boron (B) and gallium (Ga) while phosphorus (P), arsenic (As) and antimony (Sb) are commonly used for n-type doping. The amount of dopant, or doping level in silicon can be varied from 10^{15} atoms per cm^3 for very light doping up to more than 10^{20} atoms per cm^3 for heavy doping. As a comparison, crystalline silicon has 5×10^{22} atoms per cm^3 .

The semiconductor industry is constantly pushing technology towards smaller dimensions for better performance and lower cost.¹⁻² As devices shrink down to smaller dimensions, the depth of the doping needs to be reduced accordingly. The major challenge within this field is to realize ultra-shallow doping with depths below 100, or even below 10, nm.

Solar cells are another booming area in which silicon doping plays a crucial role.³ Solar cells rely on a p-n junction to separate electrons and holes under incident light. The increasing awareness of climate change calls for switching from traditional fossil fuels to cleaner energy sources. Solar cells are promising candidates for renewable energy. Researchers in this area focus on increasing efficiency and lowering the fabrication costs of solar panels.

This chapter is focused on doping techniques available for the doping of silicon. Depending on the process by which the dopant atoms are introduced into the material, these doping techniques can be divided into three major categories:

diffusion, implantation, and in-situ doping. The diffusion-based doping approaches exploit thermal annealing to drive the dopants into the silicon. In implantation strategies, the dopant atoms are forced into silicon by bombarding it with high-energy dopant ions. In-situ doping strategies introduce the dopant atoms into the materials during their growth. Advantages, limitations and specific examples are described in detail below for all three approaches.

2.2 Diffusion-based doping approaches

Diffusion-based doping approaches utilize the diffusion of dopant atoms into a solid substrate to dope silicon. The doping procedure is schematically shown in Figure 2-1. With this approach, the dopants are first deposited on top of the silicon surface, commonly in the form of an oxide, and subsequently driven into the bulk of the silicon substrate by thermal diffusion employing high-temperature annealing. According to Fick's Law, the rate of solid-phase diffusion depends on the temperature and the concentration of dopant atoms at the surface.⁴ Therefore, special focus is on controlling the temperature and time of the annealing precisely to achieve good control over the level of doping. Typical temperatures for diffusion vary between 800 °C and 1100 °C, and time intervals span from a few minutes to a few hours. There is a large variety of strategies to bind the dopant precursors onto silicon surface, which contributes to the wealth of the diffusion approaches and allows a wide range of applications.

Figure 2-1 Doping by diffusion. The process starts with a clean substrate. (a) The dopant precursor is deposited onto the substrate. (b) High-temperature annealing drives the dopant into the substrate and finally, (c) the substrate is cleaned resulting in a doped Si substrate.

Contrary to the implantation methods that will be discussed below, diffusion processes do not cause damage to the crystal lattice of silicon. This avoids the necessity to repair the damage by a high-temperature annealing process. As discussed in Section 2.3.1, such a repair process can cause the dopant to diffuse further, which makes it challenging to achieve ultra-shallow doping. Moreover, the cost of a diffusion furnace is generally lower than that of an implantation instrument.

However, the consequence of the high-temperature annealing step is that it makes independent control of the doping concentration and the junction depth difficult, as both solubility and diffusivity of the dopant in silicon are dependent on temperature. Most diffusion-based doping techniques results in a dopant profile with the highest concentration at the surface. The inability to achieve more sophisticated dopant profiles limits the application of these techniques.

2.2.1 Solid-phase diffusion

Solid-phase diffusion (SPD) approaches are based on the straightforward deposition of dopant-rich solid material on the silicon surface, which serves as a source of dopant atoms during the thermal diffusion step. Typically, borosilicate glass (BSG) or phosphosilicate glass (PSG) are used. Takemura *et al.* have reported the use of BSG as a dopant source to dope silicon.⁵ The BSG was deposited using chemical vapor deposition and was also used as the sidewall to separate gate and source/drain electrodes. They achieved sub-100 nm junction depths with a steep profile. This controlled doping process led to an extension of the source/drain region of the MOSFET. Such a doping step needs to be localized between the source/drain and the channel region of the MOSFET. This localization was achieved by photolithographic patterning of the BSG. Following that work, Iwai and co-workers reported p- and n-MOSFETs with ultra-shallow source and drain doping using this technique.⁶⁻¹⁰ In their

work they demonstrated doped active areas of the devices with junction depths of 30-40 nm for boron doping and 10 nm for phosphorus doping.

A technique similar to SPD is solid source dotation (SSD),¹¹⁻¹² which is shown in Figure 2-2. In SSD, boron oxide or silicon pyrophosphate are typically used as the dopant source for p-type and n-type doping, respectively. The source wafer is placed close to the silicon wafer. Then they are loaded together into a thermal oxidation furnace. At high-temperature the dopant oxide evaporates from the source wafer and is incorporated into the oxide layer that is growing on the silicon surface. Drive-in of the dopant is achieved by further increase of the temperature in the furnace. The SSD method has been used for the doping of silicon nanowires and nano-pillars.¹³⁻¹⁴ Although the localization of doping seems to be challenging, given the dopant atoms are in the gas phase, some control over these processes has been achieved. Rohatgi *et al.* have reported simultaneous p- and n-type doping of the opposite sides of the target wafer in one furnace run using both types of source wafers and placing them at either side of the target.¹⁵ The source wafers were silicon wafers spin-coated with phosphorus or boron spin-on glass (see Section 2.2.2). The independent control of the p-type and n-type doping under the same annealing conditions was achieved by tuning the diluting ratio of the dopant in the spin-on glass. Sheet resistance in the range of 10 – 100 Ω/sq was achieved for both types of doping.

Figure 2-2 Schematic representation of the solid-source dotation process for boron doping. (a) The silicon substrate is put in close proximity to a boron oxide wafer. (b) Both are loaded into a thermal oxidation furnace, where the boron oxide evaporates and is incorporated into the oxide layer. (c) The temperature is further increased to drive in the dopant into the silicon. (d) After cooling down and cleaning, the doped Si substrate is formed.

2.2.2 Spin-on doping

Spin-on doping (SOD) is a widely used diffusion-based doping technique.¹⁶⁻¹⁹ In SOD, spin-on glass (SOG) is used as the dopant source and is applied onto the substrate by either spin coating or spraying. The SOG is composed of a silicate or organosilicon-based compound mixed with the dopant. An organic precursor containing dopant atoms can also be used. After applying the SOG and prior to the high-temperature drive-in of the dopant, a low-temperature annealing step is commonly used to evaporate the solution and harden the glass layer. The SOG can be made with different types of dopants including B, Ga, P, Sb and As. Because spin coating is a widely available process and is easy to incorporate, spin-on doping had become one of the popular doping techniques.

Iyengar *et al.*²⁰ and Tang *et al.*²¹ have reported the application of SOD for the development of photovoltaic devices. In their work, the SOG is used not only as the dopant source but also as an anti-reflection coating or passivation layer. This reduces the fabrication steps for solar cells, and overall lowers their fabrication cost. SOD has also been reported in the fabrication of the backside contact of silicon solar cells.²²

2.2.3 Monolayer doping

In recent years the downscaling of devices has driven efforts towards decreasing both the lateral dimensions and the depth of the doped area. With the diffusion processes discussed above, the amount of dopant in the source is considered infinite. As a result, the only way to control the areal dose is by changing the annealing temperature and time. This in turn affects the doping concentration and junction depth. At the same time, ion implantation (see below), which is widely used in industry, has difficulties achieving ultra-shallow doping of, e.g., less than 10 nm. Javey and co-workers have pioneered monolayer doping (MLD), shown in Figure 2-3, to address these challenges.²³ Initially, MLD utilizes a reaction known as hydrosilylation²⁴⁻²⁵ to

covalently bind dopant-containing alkene molecules onto a hydrogen-terminated silicon surface. The monolayer that is formed this way constitutes a finite and well-defined source of the dopant, controlled at the molecular level. The commonly used compounds to introduce dopants are allylboronic acid pinacol ester and diethyl 1-propylphosphonate for p- and n-type doping (Figure 2-3), respectively. A capping layer, normally SiO_2 , is then deposited on top of the monolayer. This prevents the dopant from escaping into the gas phase during the subsequent high-temperature in-diffusion step. During the high-temperature annealing the monolayer decomposes and the dopant atoms diffuse into the silicon. The whole process is completed by stripping off the capping layer with fluoric acid-based wet etching. Since its introduction, MLD has demonstrated the capability of producing ultra-shallow doping²⁶ and the doping of 3D structures.^{23, 27-28} Apart from annealing temperature and time, MLD provides another possibility to control the doping level in silicon by fine-tuning the amount of dopant through the monolayer.

Figure 2-3 Full-wafer scale MLD for boron or phosphorus doping.²⁶ © 2009 American Chemical Society.

Recently, monolayer contact doping (MLCD) was reported by Yerushalmi *et al.* as an extension of MLD.²⁹⁻³⁰ As shown in Figure 2-4, in MLCD the dopant compound is first grafted to a silicon wafer that acts as a source wafer. This source wafer is then

brought into contact with the wafer that needs to be doped, the target wafer. High-temperature annealing drives the dopant into both source and target wafer. The benefit of MLCD is that the target wafer does not have to go through the wet chemistry process to deposit the monolayer. This makes MLCD a favorable method to dope wafers that are incompatible with the wet-chemical hydrosilylation process. MLCD also offers the possibility to increase the dopant dose to a higher level.³⁰ Multiple source wafers and annealing steps can be used upon one target wafer to boost the doping level in this wafer.

Figure 2-4 Schematic representation of monolayer contact doping.³⁰ © 2012 American Chemical Society.

Monolayer doping of Si utilizes the covalent bonding between an alkene or alkyne and H-Si to deposit a dopant onto the substrate. Similar chemical bonding between germanium and an alkene or alkyne is also possible, which is known as hydrogermylation.³¹⁻³² Although MLD on germanium has been reported,³³ the majority of literature covering MLD is based on silicon. Other semiconductor materials could possibly be doped likewise, when suitable monolayer formation processes can be found.

2.2.4 Laser doping

Different from other diffusion techniques, the laser doping (LD) method uses a high-power laser to temporarily melt the silicon surface. Dopants are driven into the molten silicon. The silicon is then recrystallized, and incorporated dopants form a shallow doping layer. Because diffusion of the dopants takes place in liquid phase and the laser-induced melting-recrystallization process happens in a very short time, this allows a quick diffusion of the dopants in the molten silicon and a relatively slower diffusion in the solid silicon underneath. As a result, the dopants form a box-shaped junction in the silicon substrate – the concentration of dopant is constant down to a certain depth into the material and then suddenly drops to a low level. LD dates back to the 1980s when Lawson first reported this technique.³⁴ In that work the dopant (Ga) was first deposited onto the surface by evaporation. Very recently, a spin-on dopant³⁵ and a paste composed of highly doped silicon nanoparticles³⁶ have been reported as the dopant source.

The strong advantage of laser doping is that it uses a scanning laser beam which enables to achieve patterned doping without the need of lithography. Using this concept, LD has been widely used in recent years in the fabrication of solar cells.³⁷⁻³⁹ Patterned emitters, or selective emitters, have been fabricated using this way for higher-efficiency solar cells.⁴⁰

A modification of LD is the gas immersion laser doping (GILD).⁴¹⁻⁴⁴ With this technique, the silicon samples are put into a chamber filled with a dopant precursor gas. The dopants are being incorporated into silicon when the laser pulse melts a thin layer of silicon. The melting-recrystallization can be repeated several times to achieve the desired doping level. Ultra-shallow and high boron doping have been reported using BCl_3 as the precursor, while employing 200mJ XeCl laser pulses.⁴⁵

2.3 Implantation-based doping approaches

Implantation is a doping technique that is currently widely used in the semiconductor industry. This technique dates back to the 1950s when two US patents⁴⁶⁻⁴⁷ describing the use of high-energy ions to dope semiconductors were filed. In the early 1960s, ion implantation was reported for the fabrication of particle detectors⁴⁸ and p-n junctions.⁴⁹ Following these studies, ion implantation became an interesting doping technique in research laboratories. In the 1970s this technique became widely adopted by the semiconductor industry and has been a dominant doping technique to date. Following a doping step using ion implantation, high-temperature annealing is needed in order to repair the damage to the Si crystal structure caused by the bombardment with the high-energy ions. Modifications have been made to this method since then to address the new challenges arising with the downscaling of semiconducting devices. This leads to new techniques introduced into ion implantation as well as the emergence of a new implantation technique, plasma immersion ion implantation.

2.3.1 Ion implantation

The process of ion implantation is schematically shown in Figure 2-5. The dopant ions are extracted from the ion source and accelerated by an electric field. This ion beam then passes through a mass analyzer to select the desired ions and filter out contaminations. Thereafter, the ion beam is guided through a set of lenses to focus it onto the substrate. Finally, the ions are accelerated or decelerated to the desired energy and bombard the substrate. The ions penetrate through the surface, lose their energy due to collision with substrate atoms and then come to a stop. This collision mechanism results in significant crystal damage along the way, which has to be repaired by high-temperature annealing. This annealing step also drives the dopants into crystal lattice positions, resulting in electrical activation of the dopants.

Ion implantation is the dominant doping technique for the semiconductor industry since the 1970s. Compared to the diffusion techniques it offers a number of benefits.⁵⁰ It allows independent control over the dopant concentration and the depth, or the doping profile. This is achieved by tuning the area dose and the ion energy. The dopant ion beam is scanned over the sample to achieve homogeneous doping on large or multiple wafers. Furthermore, it is capable of introducing an amount of dopants exceeding the solid solubility limit. Compared to diffusion, the thermal treatment needed for ion implantation can be lower. This reduces the lateral diffusion of the dopant and leads to a more well-defined location of the doped region.

Figure 2-5 A typical arrangement of an ion implanter.⁵¹ © 1998 Elsevier Science S. A.

As transistors are scaled down to smaller dimensions, the depth of the doped junction needs to be reduced accordingly. According to the 2013 edition of the International Technology Roadmap for Semiconductors (ITRS), for 14 nm node the depth for source/drain doping is 8.8 nm, and for 10 nm node this is 7.3 nm.⁵² For normal ion implantation it is difficult to reach such shallow doping simply by reducing the implantation energy. This is due to the transient enhanced diffusion (TED) associated with the implantation process: the damage to the crystal structure can cause the dopants to diffuse much faster than desired during the annealing step. As a result, the dopant distribution becomes deeper than as implanted. This makes it challenging for ion implantation to form ultra-shallow doping. The TED is more prominent for boron.

There are two reasons for this: (i) the boron atoms are lighter, hence at a given implantation energy they are accelerated to a higher speed, which causes more damage to the crystal structure, and (ii) boron has a higher diffusivity in silicon. When shallow boron doping is required, BF_2^+ can be used instead of B^+ as the former ion is heavier. Still, it remains challenging to achieve ultra-shallow boron doping. For n-type doping, because the dopants are heavier and have lower diffusivity, the TED effect is less. This makes n-type shallow doping less challenging to achieve.

For single-crystal materials, the atoms are located at the crystal lattice positions. Along certain orientations these atoms form channels. When ions enter the material along these directions they can penetrate much deeper along these channels. This results in a deeper implanted dopant profile than expected. This is known as the channeling effect. In practice, ion implantation is normally done at $7^\circ - 10^\circ$ off the perpendicular direction to avoid direct exposure of the channels to the incident beam. However, ions can still be randomly scattered into the channels and penetrate deeper into the material. This is more likely to happen for ions with a lower mass and a lower energy. To suppress the channeling effect, a pre-amorphized implantation step can be used prior to the dopant implantation. This is achieved by a preceding implantation step with a high dose of Si or Ge ions. This bombardment generates enough damage in the material to make it amorphous. The crystal orientation then becomes randomly distributed in the amorphized material, which avoids the exposure of channels at any orientation.

Achieving shallow doping using ion implantation is less straightforward. Schmitz *et al.*⁵³⁻⁵⁵ have reported the use of silicon oxide as a screening layer and implanted into such oxide layer. A subsequent thermal annealing process diffused the dopant into silicon. Junctions of sub-20 nm were reported in these studies.

2.3.2 Plasma immersion ion implantation

The traditional ion implantation method can form well-controlled doping profiles in materials. However, the high costs of implantation instruments limits its application. Plasma immersion ion implantation (PIII) has been proposed as a cost-effective alternative to ion implantation.⁵⁶⁻⁵⁷ The principle of PIII is schematically shown in Figure 2-6. The substrate is put in a chamber filled with a high-density plasma of the dopants ions. The plasma can be generated by a plasma induction device or by a negative bias applied on the substrate. The substrate bias accelerates the ions towards the sample leading to penetration into the substrate material. In recent years the use of PIII has been extended to the production of silicon-on-insulator (SOI) wafers, the implantation of insulating materials, and biomedical applications.⁵⁸

Figure 2-6 Schematic representation of plasma immersion ion implantation (PIII). The substrate is put in a chamber filled with a dopant precursor gas. The gas is ionized either by the negative bias on the substrate or another plasma induction device, and the ions are accelerated towards the substrate. The ion sheath is the region in which the ions are accelerated by the substrate bias.

PIII is capable of doping steep trenches at the surface. The conformal implantation of trenches with aspect ratios of up to 12 has been demonstrated.⁵⁹ The doping of 3D finFET silicon structures has been reported by Lee *et al.* (Figure 2-7).⁶⁰ They showed a substantially lower level of crystal damage by PIII compared to normal ion implantation. PIII is also capable of introducing high doses of dopants at low implantation energy. Such low-energy, high-dose doping is challenging for standard ion implantation due to its low ion extraction rate at low implantation energy. This

makes PIII an interesting strategy to make ultra-shallow high-dose doping. On the other hand, PIII lacks the mass analyzer to filter out undesired contaminations. Therefore, an ultrahigh purity dopant gas is needed for PIII to achieve high-quality doping. Furthermore, an annealing step is still necessary to activate the dopant ions and to repair the crystal damage resulting from implantation.

Figure 2-7 Scanning spreading resistance microscopy (SSRM) image of a silicon finFET doped using the PIII. A conformal doping along the surface of the fins (orange layer at the yellow structures) is shown in this figure.⁶⁰ © 2013 AIP Publishing LLC

2.4 In-situ dopant incorporation

With the diffusion and implantation methods, dopants are introduced into the substrate as foreign atoms in a separate process step. Contrary to these ex-situ doping techniques, in-situ doping incorporates the dopant atoms into the substrate while it is being grown. This technique can easily be incorporated into fabrication processes involving chemical deposition or epitaxy. In-situ doping methods operate at temperatures that are lower than the temperatures necessary to drive diffusion or to repair damages caused by implantation. This makes the in-situ doping suitable for samples that are not compatible with high-temperature processes.

2.4.1 Chemical vapor deposition

The growth of silicon films by chemical vapor deposition (CVD) has been studied from the early 1980s.⁶¹⁻⁶² Precursor gases that are commonly used include silane and mono-, di-, tri- or tetra-chlorosilanes mixed with hydrogen. The dopant precursors can be added into the depositing gas to result in the deposition of doped silicon in one step. The most common dopant precursor gases for boron doping are diborane (B_2H_6) and trimethylboron ($B(CH_3)_3$).⁶³⁻⁶⁴ For phosphorus doping, phosphine (PH_3) is commonly used.⁶³ Low-pressure CVD (LPCVD) and plasma-enhanced CVD (PECVD) are two commonly used processes to form doped silicon films. The substrate is heated up to temperatures above 600 °C. Deposition rates of LPCVD are typically low at a few nm per minute. To achieve higher deposition rates and lower deposition temperatures, PECVD can be used. With PECVD, deposition can be achieved at 300 °C. The deposition can be 40 times higher than for LPCVD. The deposited layer resulting from CVD usually consists of amorphous or polycrystalline silicon. The doping concentration of CVD can be controlled by tuning the partial pressure of the dopant precursor gases. The concentration can be in the range of $10^{17} - 10^{21} \text{ cm}^{-3}$ for phosphorus and $10^{17}-10^{22} \text{ cm}^{-3}$ for boron.⁶⁵

The in-situ doping approach during CVD processes has proven to be widely useful. For instance, this technique is used to form amorphous Si (a-Si) films for LCD displays and thin-film solar cells. The a-Si has a larger optical absorption coefficient than crystalline Si (c-Si), which makes it a more ideal substrate for solar cells. Lower temperatures that are used in this process also reduce the fabrication cost.⁶⁶ The low-temperature required during this process also makes it possible to make devices on plastic substrates. This constitutes a solid base for the future application of this process for flexible electronics.

2.4.2 Vapor-liquid-solid deposition

In recent years the metal-catalyzed vapor-liquid-solid (VLS) deposition gains increasing interest for the fabrication of silicon nanowires or nanodots, owing to its capability to achieve nanowires with well-controlled diameter and length.⁶⁷ Figure 2-8 schematically shows this approach and the resulting nanowires. This technique was first demonstrated by Wagner and Ellis in 1964.⁶⁸ In this strategy, gold particles are first deposited on a silicon surface.⁶⁹ Subsequently, the substrate is heated up to above 363 °C in an atmosphere of silicon precursor gas, above which temperature gold and silicon can form a liquid mixture. When more silicon atoms enter the liquid alloy from the vapor phase precursor, it starts to precipitate from the liquid alloy. This bottom-up growth results in single-crystal silicon nanowires. The diameter of the wires is controlled by the size of the gold nanoparticles. Radial growth of the wire can also occur, but this is mostly unintended or undesired. Dopants can be added to the precursor gas to create doped wires. The commonly used precursors are P, PH_3 , or trimethylantimony (TMSb) for n-type and B_2H_6 , trimethylboron (TMB), or AsH_3 for p type.⁷⁰ The dopant is incorporated into the liquid alloy seeds on top of the wire while growing. It has been reported that dopant incorporation is found to be more efficient in radial growth than in axial growth.⁷¹ For phosphorus doping, the wire resistivity was found to be proportional to the PH_3/SiH_4 ratio in precursor.⁷²⁻⁷⁴

Figure 2-8 (a) The mechanism of vapor-liquid-solid (VLS) growth and (b) SEM images of the resulting silicon nanowires.⁷² © 2010 American Chemical Society.

Various silicon devices based on VLS nanowires have been reported. Lieber *et al.* have demonstrated pH and DNA sensors with Si nanowires made from VLS methods.⁷⁵⁻⁷⁶ La Magna *et al.* have fabricated silicon solar cells using such VLS wires.⁷⁷ Fabrication of field-effect transistors based on the Si nanowires has also been reported.⁷⁸⁻⁸⁰ The nanowires have also been used as bio-sensors⁷⁶ for the detection of DNA and various gas phase sensing methods for the detection of H₂,⁸¹⁻⁸² NO₂,⁸³ humidity,⁸⁴⁻⁸⁵ and NH₃.⁸⁶ Sensing devices for detection of organic compounds have also been reported.⁸⁷⁻⁹⁰ Due to the small size of the nanowires, quantitative measurement of the doping can be a challenge although progress has been made in recent years.⁷⁰ The level of doping in the nanowires is one important factor for the device performance hence optimization of the device also includes control of the doping level.^{80, 84-85}

2.5 Summary

The doping of silicon plays an important role in tuning the electrical properties of the material. Three major categories of doping strategies have been discussed above: diffusion, ion implantation, and in-situ incorporation. These doping strategies have evolved over the past decades to keep up with the demands arisen from pushing the technology for electronic device fabrication to smaller dimensions and from low cost requirements for solar cells.

Aforementioned doping approaches have been developed to primarily address a number of challenges that relate to specific requirements such as the depth, concentration, spatial resolution of the doping, or specific limitations imposed by the fabrication conditions that can be used. Spin-on doping has been developed to lower fabrication costs. Monolayer doping provides a defect-free doping process, while adding another dimension to controlling the doping level in silicon. Laser doping makes it possible to form ultra-shallow doping with a steep dopant distribution, and it allows patterned doping. Ion implantation provides independent control of doping

concentration and dopant distribution. Plasma implantation achieves shallow doping, while reducing the damage to the crystal structure. The in-situ doping offers a low-temperature approach to dope silicon structures. Evolvement in semiconductor industry is going to push the doping technique forward to address the new challenges. The change towards the 3D finFET device architecture lowers the requirements for shallow doping, but the challenge to achieve well-defined levels and distributions of doping without crystal damage remains. For solar cells the drive for lower costs and higher efficiencies requires more cost effective and mass scale doping technique.

2.6 References

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Chapter 3

Controlling the dopant dose in silicon by mixed monolayer doping¹

Molecular monolayer doping (MLD) presents an alternative to achieve doping of silicon in a nondestructive way and holds potential for realizing ultra-shallow junctions and doping of nonplanar surfaces. Here, we report the mixing of dopant-containing alkenes with alkenes that lack this functionality at various ratios to control the dopant concentration in the resulting monolayer and concomitantly the doping dose in the silicon substrate. The mixed monolayers were grafted onto hydrogen-terminated silicon using well-established hydrosilylation chemistry. Contact angle measurements, X-ray photoelectron spectroscopy (XPS) on the boron-containing monolayers, and Auger electron spectroscopy on the phosphorus-containing monolayers showed clear trends as a function of the dopant-containing alkene concentration. Dynamic secondary-ion mass spectroscopy (D-SIMS) and Van der Pauw resistance measurements on the in-diffused samples showed an effective tuning of the doping concentration in silicon.

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3.1 Introduction

Downscaling of electronic devices is driven by performance improvement and cost reduction.¹⁻² For decades, the semiconductor industry has been shrinking electronic components to keep up with Moore's Law. Doping of silicon is one of the key processes to tune its electrical properties by intentionally incorporating foreign atoms into the crystal lattice.³ Conventional doping relies on ion implantation, which involves bombarding the material with high-energy, dopant-containing ions.³ The advantage of this technique is its independent control of doping concentration and junction depth or doping profile.⁴ However, ion implantation suffers from various drawbacks including damage to the crystal lattice during ion bombardment and subsequent transient-enhanced diffusion of the dopants caused by these defects.⁵ This limits the application of this technique in making ultrashallow junctions,⁶ which are used to suppress short channel effects merged with the downscaling of transistors. Alternative approaches to doping include solid-phase diffusion. However, this technique faces limits at controlling the doping concentration, especially near the surface. These drawbacks constitute a great challenge for further downscaling silicon devices.

The recently developed molecular monolayer doping (MLD) technique offers a promising alternative.⁷ This technique utilizes hydrosilylation⁸⁻¹² to covalently attach dopant-containing molecules to hydrogen-terminated silicon. The dopants are subsequently driven in by a high-temperature annealing process. Compared to ion implantation, it is a milder technique to introduce dopants into a material and thus avoids crystal damage. Furthermore, this technique has the potential to dope 3-D structures on nonplanar silicon surfaces, which are more vulnerable to crystal damage.¹³ Using MLD, dopants can be introduced into the material from the sidewalls, as well as from the top on such surfaces. Furthermore, sub-5 nm junctions have been demonstrated to date,¹⁴ making MLD ideally suited for producing ultrashallow

junctions. Localized doping on silicon has been shown by combining MLD with nanopatterning techniques such as nanoimprint lithography, achieving doped dot or line patterns on silicon.¹⁵⁻¹⁶ While the control of junction depth and localized doping have been established with MLD, the precise control of the amount of dopant or doping dose remains challenging.

Currently achieved doping concentrations with MLD are on the order of 10^{20} cm^{-3} . On the other hand, in the semiconductor industry the doping of silicon ranges from as low as parts per billion level up to a few percent, which is in the range of $10^{15} - 10^{21} \text{ cm}^{-3}$. We believe that extending the doping concentration of MLD to a broader range will greatly expand its potential, especially in electronics and solar energy collection. Here, we report a technique in which a monolayer, consisting of a dopant-containing compound and the dopant-free 1-undecene, is grafted onto the silicon surface. The 1-undecene reacts with H-Si sites, hence reducing the ones available for the dopant-containing molecule. This reduces the amount of dopant atoms available for incorporation in the silicon crystal lattice during the annealing process. Although initial attempts were pioneered by Javey *et al.*,⁷ the use of only two mixing ratios (1:5 and 1:20) with boron doping prevented a clear establishment of the validity of this method to reproducibly control the doping dose. Here we present a detailed study on the relation between the mixing ratio in solution, the monolayer composition resulting on the surface, and the doping dose inside the silicon upon thermal annealing for both boron and phosphorus doping using X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), dynamic secondary-ion mass spectroscopy (D-SIMS), and Van der Pauw measurements.

3.2 Materials and methods

3.2.1 Monolayer formation

Allylboronic acid pinacol ester (97%, ABAPE), diethyl vinylphosphonate (97%, DVP), 1-undecene (97%) and mesitylene (puriss, >99.0%) were ordered from Sigma-Aldrich and used as received. ABAPE or DVP were mixed with 1-undecene at various fractions from 100% (pure dopant molecule) to 0.1%. This precursor mixture was then diluted with mesitylene at a ratio of 1:19 v/v. The mixed chemicals were transported into a reaction flask and degassed using the freeze-pump-thaw method for at least three cycles. Single-side polished intrinsic silicon<100> wafers were diced into 1×1 cm pieces and cleaned in acetone sonication for 10 min to remove particles generated during dicing and then in Piranha (98% of H₂SO₄ and 30% H₂O₂ mixed at 3:1 v/v) for 30 min to remove any possible organic contaminant on the surface. Thereafter, the pieces were dipped in 1% aqueous HF to remove the native silicon oxide layer and to yield a hydrogen-terminated surface. After rinsing in Milli-Q water (resistivity > 18 MΩ·cm) and drying in a N₂ stream, the cleaned silicon pieces were transported into the reaction flask in a glovebox filled with nitrogen. Hydrosilylation, which grafts the chemical compounds onto the H⁻Si surface, was performed by heating the reaction flask equipped with a condenser up to 180 °C in an oil bath overnight under continuous nitrogen inflow. The reaction was stopped by removing the heating. The pieces were taken out, rinsed with an excessive amount of toluene (puriss), acetone (puriss), methanol (absolute), and MilliQ water, followed by sonication in acetone for 10 min to remove any physisorbed material. Contact angles were measured immediately after the hydrosilylation. Then the pieces were sealed in a nitrogen glovebox and stored under nitrogen prior to further measurements or high-temperature annealing.

3.2.2 XPS and AES

XPS measurements were performed on a Physical Electronics Quantera scanning XPS setup. Monochromatic Al-K α X-rays at 1486.7 eV were used. The chamber was evacuated to below 3×10^{-9} Torr. Measurements were performed with argon neutralization, and the working pressure was maintained at around 2×10^{-8} Torr throughout the measurement. A takeoff angle of 20 degree and acceptance angle of 20 sr were used for collecting signals from the monolayers. Collected spectra were calibrated setting the C 1s peak at 284.8 eV.

AES measurements were performed at room temperature with a scanning Auger electron spectroscope (JEOL Ltd. JAMP-9500F field emission scanning Auger microprobe) system. AES spectra were acquired with a primary beam of 10 keV. The takeoff angle of the instrument was 0°. We used the differential energy spectrum to subtract background from the direct Auger spectrum for calculating the peak-to-peak intensity. The first differential $d(N(E))/d(E)$ Auger spectra were obtained by numerical derivation of the direct $N(E)$ integrated Auger data displaying an absolute scale with counts/second units by a universal Savitzky–Golay (SG) Quadratic differential filter using seven points and used to calculate the peak-to-peak intensity of Auger electrons and derive the elemental compositions. The differential spectrum is simply the differential of the direct spectrum with respect to energy. All AES spectra were evaluated by CasaXPS software (version 2.3.16 Prerel 1.4). The spectra were calibrated with the carbon peak at 263.0 eV.

3.2.3 Capping layer deposition and annealing

Fifty nm of SiO₂ was sputtered onto the monolayer-modified silicon surface using a custom-built sputtering system. The chamber was backfilled with 1 sccm of oxygen to achieve stoichiometric SiO₂ layers. The power applied on the target was 400 W, resulting in a deposition rate of 3.4 nm/min. High-temperature annealing was

performed in a furnace set at 1000 °C for 5 min. After annealing, the samples were taken out and cooled down to room temperature.

3.2.4 SIMS measurements

In-diffused samples were first dipped in HF to remove the capping layer and then cleaned with Piranha to remove any organic residuals from the surface. SIMS depth profiles were recorded using a Cameca IMS 6f system with 3 keV O_2^+ primary ions in positive mode. The error for all data was within 10%. Secondary ions of ^{11}B and ^{31}P were detected. The measured ^{11}B concentration was converted to total boron coverage using the known isotopic ratio. The measurement chamber was backfilled with O_2 . Quantification and depth calibration were based on reference samples with known profiles.

3.2.5 Sheet resistance measurements

The four-probe Van der Pauw method¹⁷ was used to determine the sheet resistance of samples on a probe station. The current was swept between two neighboring connections while the voltage was measured between the other two. The slope extracted from the measured I - V curve gave the resistance. Swapping the current source and voltage measurement electrodes would measure another resistance. The average of these two gave the resistance R_A . The resistance R_B was measured at rotated polarity using the same method. Sheet resistance R_S was then determined from the equation

$$e^{-\pi R_A/R_S} + e^{-\pi R_B/R_S} = 1$$

The two resistances used to calculate R_A and R_B were used separately to determine the standard deviation of the sheet resistance data.

3.3 Results and discussion

Preparation of the samples is schematically shown in Figure 3-1. In MLD, we used allylboronic acid pinacol ester (ABAPE) and diethyl vinylphosphonate (DVP) with olefin terminal groups as the dopant source. Piranha cleaning and HF etching provides the hydrogen-terminated silicon surface. Molecules were grafted onto the surface by hydrosilylation using mixtures of dopant-containing alkene and 1-undecene at various mixing ratios from 100% (pure dopant compound) to 0.1%. A capping layer of 50 nm SiO_2 was deposited on top to prevent the dopant atoms from being released to the ambient during the subsequent annealing step. The surface junction was achieved after high-temperature annealing at 1000 °C for 5 min, followed by removal of the capping layer in 1% aqueous HF.

Figure 3-1. Preparation process of the mixed monolayer doping samples: (a) wet etching of native SiO_2 with dilute aqueous HF yields the H-terminated silicon surface, (b) hydrosilylation grafts dopant as well as diluting molecules onto the H-terminated Si surface, (c) SiO_2 capping layer is sputtered onto the modified surface and (d) a high-temperature rapid annealing and removal of capping layer result in a surface junction with dopants.

Following the hydrosilylation reaction, the substrates were first characterized by water contact angle (CA) measurements. The difference in wettability of the dopant-containing molecules and 1-undecene and their ratio will cause different CAs to be measured. The results are shown in Figure 3-2. ABAPE (boron) and DVP (phosphorus) contain a more hydrophilic head group compared to 1-undecene. The advancing/receding CAs for the monolayers formed by neat ABAPE and DVP start at low CA and increase when diluted with an increasing amount of undecene. This increase of the CA is observed up to the value of approximately 105/85, where it becomes constant with an increasing amount of undecene. This value corresponds to the reported value for alkene monolayers on silicon.¹⁸ The plateau is reached for monolayers formed from mixed solutions containing 30% ABAPE and 10% DVP as shown in Figure 3-2a and b, respectively. At lower fractions of dopant adsorbate, the CA is not sensitive anymore to changes in the composition. This trend can be explained by Cassie's law, which predicts the CA on a composite surface, θ_c , based on the CAs on each of the two components and fractions of the two components:

$$\cos \theta_c = f_1 \cos \theta_1 + f_2 \cos \theta_2.$$

where θ_1 and θ_2 are the CAs observed for the two components separately. With this equation and the measured advancing/receding CAs of neat ABAPE, DVP, and 1-undecene monolayers of 77.6/54, 54.5/0, and 105/88, we calculated the predicted CAs for both ABAPE and DVP mixed surface. The calculated data are shown as dashed lines in Figure 3-2. The measured CAs fit well with the calculated ones, which indicates that the fraction of ABAPE and DVP in the mixed monolayers with 1-undecene is in a good agreement with their amounts present in the solutions. The slight overestimation of the CA of the DVP mixed monolayers (Figure 3-2b) may indicate a small preference for the binding of DVP relative to 1-undecene in this case.

Figure 3-2 Contact angle measurements of silicon substrates functionalized with mixed monolayers of allylboronic acid pinacol ester (ABAPE, a) or diethyl vinylphosphonate (DVP, b) and 1-undecene as a function of the fraction of dopant adsorbate in solution. Advancing (■) and receding (▲) contact angles are shown separately. Predicted CAs based on Cassie's law are shown as dashed lines.

To get quantitative results on the composition of the mixed monolayers, samples with ABAPE monolayers were investigated by X-ray photoelectron spectroscopy (XPS). The measurements were performed at a 20° takeoff angle to achieve a higher relative boron signal intensity. Figure 3-3a shows a spectrum acquired on a full ABAPE monolayer. The boron signal at 191.6 eV partially overlaps with the Si 2s plasmon signal. The higher energy edge of the Si 2s plasmon was used as tilted background (red line in Figure 3-3a) in the quantification. Figure 3-3b shows the C 1s region in which the two peaks at 284.8 and 286.8 eV correspond to C–C and C–O bonding in the molecules, respectively. The ratio of the two peak areas was calculated to be 3.3, close to the theoretical 3.5 deduced from the atomic ratio of ABAPE ($C_9H_{17}O_2B$). Relative boron and carbon fractions as well as the boron to carbon ratio were calculated for the monolayers prepared at different fractions of dopant adsorbate in solution (see Table 3-1). The measured relative boron fraction decreases dramatically from 1.09% for the monolayer prepared with the neat compound to about 0.01% for the monolayer prepared at 6% of ABAPE. The latter approaches the detection limit of the instrument, and lower amounts of boron could not be unambiguously detected. The measured carbon fraction, on the other hand, increased as more 1-undecene was

added into the monolayers. We note that from the pure compound (100% ABAPE) a B/C ratio of 0.03 is measured, which is lower than the theoretical 0.11 deduced from the atomic ratio of ABAPE. This could be attributed to unintended carbon contamination from the ambient. Given that all samples were prepared and measured under the same conditions, implying similar amounts of contamination, the variations over the series can nevertheless be determined reliably.

Figure 3-3 XPS spectrum at 20° takeoff angle of the B 1s (a) and C 1s (b) regions, for a full monolayer of ABAPE. Due to partial overlap with the Si 2s plasmon peak, a tilted baseline (red) was used for quantification. Two carbon peaks at 284.8 (green) and 286.8 eV (blue) are attributed to C–C and C–O bonding, respectively.

Table 3-1 Relative boron and carbon concentrations and boron to carbon ratio from XPS measurements on surfaces modified with mixed monolayers with ABAPE and 1-undecene.

Sample	B [%]	C [%]	B/C
100% ABAPE	1.09±0.17	34.05	0.0320±0.0050
80% ABAPE	0.69±0.32	40.75	0.0169±0.0078
60% ABAPE	0.68±0.13	47.71	0.0142±0.0027
30% ABAPE	0.14±0.12	45.73	0.0031±0.0026
10% ABAPE	0.06±0.12	51.53	0.0012±0.0023
6% ABAPE	0.01±0.01	51.07	0.0002±0.0002

Because of the overlap of the phosphorus P 2p signal with the Si 2p plasmon peak, we were unable to establish the amount of DVP on silicon by means of XPS. Alternatively, Auger electron spectroscopy (AES) was performed on those samples. A full AES spectrum of the 100% DVP sample is shown in Figure 3-4a. Signals of phosphorus, carbon, oxygen and silicon can be detected in the full spectrum scan. Figure 3-4b shows the quantification of the amount of phosphorus measured on monolayers prepared at different fractions of DVP. Two locations on each sample were measured. All samples were measured under the same conditions, with the same instrumental settings to make sure that the sample-to-sample trend could be determined reliably. The measured phosphorus concentration decreases from about 1.7% to about 0.5% as the DVP fraction varies from 100% to 10%. The phosphorus signal leveled off at DVP fractions below 6%. Overall, both the XPS (boron) and the AES (phosphorus) data confirmed that mixing the dopant adsorbate with 1-undecene provides mixed monolayers on the surfaces. We also tried to measure ABAPE samples using AES; however, the instrument's detection limit for boron prevented us from drawing any firm conclusion from the data. Even though both data do not give well quantified results, the relative trends indicate a roughly linear relationship between the fraction of dopant adsorbate and its presence in the mixed monolayer in both dopant cases, in agreement with the CA data presented above.

Figure 3-4 (a) Full differentiated AES spectrum on a pure DVP monolayer sample. P, C, O, and Si can be identified from this spectrum. (Inset) Zoomed in region of P. (b) Relative amount of P plotted as a function of the DVP fraction in the mixture used to make the monolayers. Two points were measured on each sample (■ and ◇).

In order to diffuse the doping atoms into the underlying silicon substrate, a SiO_2 capping layer of 50 nm was sputtered on top to prevent the monolayer to be disintegrated and removed from the substrate during the rapid thermal annealing step. The diffusivity of boron and phosphorus is considerably higher in silicon than in silicon oxide¹⁹⁻²⁰. The samples were annealed at 1000 °C for 5 min during which the molecules forming the monolayer decompose and the formed elements diffuse into the silicon.

To study the diffusion process, the capping layer was removed and dynamic secondary ion mass spectroscopy (D-SIMS) was used to measure the depth profiles of the diffused elements (Figure 3-5a and b). The dopant profiles follow the diffusion profile by Fick's law. For boron-doped samples, the dopants diffuse to a depth of about 125 nm for the pure compound. The diffusion depth gradually decreases to 50 nm for the 0.1% boron-containing adsorbate. The surface concentration reaches $1.6 \times 10^{19} \text{ cm}^{-3}$ for the pure compound and this concentration decreases to $4.2 \times 10^{18} \text{ cm}^{-3}$ for the 0.1% diluted adsorbate. For phosphorus-doped samples, the measured diffusion depth also varied from about 150 nm for the pure compound to 50 nm for

the 0.1% phosphorus-containing adsorbate. The surface concentration varied from $2.4 \times 10^{19} \text{ cm}^{-3}$ to $2.2 \times 10^{18} \text{ cm}^{-3}$. These data effectively show that mixing the dopant molecules with 1-undecene can tune the doping concentration. Lower concentrations can be achieved by further diluting the adsorbate in the hydrosilylation process. The areal doses of dopant per cm^{-2} were calculated by integrating the concentration over depth as shown in Figure 3-5c and d. For both the boron- and the phosphorus-doped cases the total dose was reduced by a factor between 2 and 3 as the mixing ratio decreased by 1 order of magnitude. This result deviates from the fractions in the monolayer prior to diffusion of the dopant atom into silicon and the contact angle measurements done before on the monolayers. We observed that at lower concentrations within the monolayer the dopants are more efficiently diffused. Multiple reasons can contribute to this behavior as the diffusion of the atoms from the monolayer into the silicon is a complex process and depends on the decomposition kinetics of the molecules, solubility and diffusivity of the specific elements in Si and SiO_2 and the related interfacial effects. Although the diffusivity of the dopants in Si is considerably higher than their diffusivity in SiO_2 it still remains unclear how much of the dopants is lost in the capping layer. Even though the diffusion process is nonlinear, our data show that the doping dose can be tuned in a controlled manner over an order of magnitude by changing the ratio between dopant adsorbate and 1-undecene for both P and B doping (Figure 3-5c and d).

Figure 3-5 Dynamic SIMS dopant profiles of (a) boron- and (b) phosphorus-doped surface junctions after capping layer deposition and high-temperature annealing. Black, red, blue, magenta, and green lines show the doping profile of 100%, 10%, 3%, 1%, and 0.1% mixing ratios, respectively. (c and d) Total dose of dopant per cm^{-2} ; dashed line indicates the decreasing trend with the fraction of adsorbate. All concentration and total dose measurements have an error below 10%.

Since the doping utilizes organic precursors, incorporation of carbon is potentially problematic in this process. The boron- and phosphorus-containing molecules have nine and six carbon atoms in their structures, while the undecene molecule has 11. The total amount of carbon could therefore be expected to be an order of magnitude higher than the dopant. We attempted to measure the carbon profile using SIMS. Due to the presence of atmospheric carbon residues that cannot be removed completely, the detection limit of carbon is restricted by a background level of about $1 \times 10^{18} \text{ cm}^{-3}$.

Consequently, we were unable to measure reliably the carbon content in the samples. Previous studies suggest that carbon contamination in MLD is limited to a depth of a few nanometers close to the surface.²¹ Moreover, based on previous measurements of leakage currents, it is well accepted that the incorporation of carbon into the silicon lattice is not of a major concern.¹⁴

To see how the amount of doping in the substrate affects the electrical properties, the sheet resistance of the doped junctions was measured using the four-point Van der Pauw method.¹⁷ An estimate of the sheet resistance (R_S) can be calculated from the measured SIMS profile using the following relation:

$$\frac{1}{R_S} = \int qN(x)\mu(x) dx . \quad (3-1)$$

where q is the electron/hole charge, $N(x)$ is the concentration profile as a function of depth x , and $\mu(x)$ is the carrier mobility which can be determined using Klaassen's model:²²

$$\mu(x) = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (N(x)/N_{ref1})^{x_1}} . \quad (3-2)$$

The measured and calculated R_S values are shown in Figure 3-6. Both sets of data follow the same trend: as the amount of dopant atoms decreases, the resistance of the silicon increases. So, qualitatively, we can conclude that controlling the monolayer doping dose provides a way to control the electrical properties of the substrate.

The measured R_S is in good agreement with the predicted one for phosphorus-doped samples. For the boron-doped ones, the measured R_S trend is steeper than the theoretical one but still in good agreement. As a control experiment a sample modified with pure 1-undecene and annealed under the same conditions was prepared and characterized as well. The resistance measured for this carbon-doped silicon substrate is shown in Figure 3-6 (dashed line). R_S of an intrinsic piece of Si without any modification was also measured and indicated as the solid line. The

resistance of the carbon-doped sample, although lower than the intrinsic one, is still in the same order of magnitude. This indicates that the presence of carbon has a minor effect on the silicon resistance.

Figure 3-6 Sheet resistance measurements (▲) on (a) boron- and (b) phosphorus-doped samples as well as the estimated values (■) based on the doping profile measured by SIMS. Dash and solid lines indicate the RS measured on “carbon doped” and intrinsic Si without any doping. Standard deviations of all data points were found to be below 5% apart from the 1% boron absorbate one, which has an error of 16%.

3.4 Conclusions

We demonstrated tunable silicon doping using MLD for both p- and n-type dopants. The doping-containing precursor molecules are mixed with undecene and grafted onto the silicon surfaces by hydrosilylation to control the amount of the dopants at interface. A surface junction was formed by deposition of a capping layer and high-temperature annealing to drive in the dopant atoms. Measurements on both the modified surface and the in-diffused junctions showed that tuning of the doping level by mixing the monolayers is feasible. Water contact angle goniometry on the modified surface indicated that the monolayer composition is proportional to the fractions of doping-containing molecules in the solution. The surface concentrations achieved are

$4.2 \times 10^{18} \text{ cm}^{-3}$ for boron-doped and $2.2 \times 10^{18} \text{ cm}^{-3}$ for phosphorus-doped silicon. Both the surface concentration and the doping dose can be varied over 1 order of magnitude. The high concentration measured at lower dopant atom fractions suggests a suppression of the dopant atom migration into the silicon at higher concentration. Further dilution of the boron or phosphorus adsorbate could in principle achieve a lower level of doping. We also demonstrated that the resistance of the samples correlates with the amount of dopants introduced via the monolayer. This shows that using mixed monolayers constitutes an important control parameter in the MLD technique and will dramatically enhance its potential use in the formation of nanoscale functional devices.

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Boosting the boron dopant level in monolayer doping by carboranes¹

Monolayer doping (MLD) presents an alternative method to achieve silicon doping without causing crystal damage, and it has the capability of ultra-shallow doping and the doping of non-planar surfaces. MLD utilizes dopant-containing alkene molecules that form a monolayer on the silicon surface using the well-established hydrosilylation process. Here, we demonstrate that MLD can be extended to high doping levels by designing alkenes with a high content of dopant atoms. Concretely, carborane derivatives, which have ten B atoms per molecule, were functionalized with an alkene group. MLD using a monolayer of such a derivative yielded up to ten times higher doping levels, as measured by X-ray photoelectron spectroscopy and dynamic secondary mass spectroscopy, compared to an alkene with a single B atom. Sheet resistance measurements showed comparably increased conductivities of the Si substrates. Thermal budget analyses indicate that the doping level can be further optimized by changing the annealing conditions.

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4.1 Introduction

Semiconductor technology is continuously pushed towards smaller dimensions in order to achieve better device performance and lower fabrication costs.¹⁻² Doping of silicon is one of the crucial steps in semiconductor device fabrication.³ Conventional doping is predominantly based on ion implantation.³⁻⁴ Alternative doping techniques have been introduced including in-situ chemical vapor deposition, solid source dotation, and proximity doping.⁵ Very recently silicon nanoparticles doped with boron have been shown to effectively dope silicon wafers up to 10^{21} cm^{-3} .⁶ Monolayer doping (MLD) is a promising alternative that was pioneered by Javey and coworkers.⁷ It avoids the crystal damage that is common for ion implantation and offers the capability for ultra-shallow doping and for doping 3-D structures.⁸⁻⁹

In semiconductor technology, silicon is doped in the range of 10^{15} to 10^{21} cm^{-3} to achieve desired electrical properties. Initially reported doping levels of silicon using MLD have been on the order of 10^{20} cm^{-3} . We have reported an MLD process based on mixed monolayers to achieve lower doping levels in a controlled manner (see Chapter 3).¹⁰ In this concept, the doping precursor is mixed with an alkene that does not contain the dopant, and this mixture is grafted onto the silicon surface by hydrosilylation. Varying the mixing ratio has resulted in an effective tuning of the doping level in silicon. Yet, the nature of this mixing process limits its application to lower doping levels only. Yerushalmi and coworkers have recently proposed monolayer contact doping.¹¹ By this method, the doping precursor is first grafted onto a donor substrate by hydrosilylation, and this substrate is then brought into contact with the target substrate. A subsequent high-temperature annealing step is used to drive the dopant atoms into both the donor and target substrates. By repeating the hydrosilylation-contact-annealing cycle on the same target substrate, higher levels of phosphorus doping have been achieved.

Here, we demonstrate a different approach to achieve higher doping levels. We designed and used alkene molecules that carry a carborane cluster. Using these molecules with their naturally high content of boron in MLD, higher doping levels in silicon can be achieved readily in a single grafting and annealing process. This makes the technique attractive when a higher doping level is required while minimizing the thermal budget.

4.2 Materials and methods

4.2.1 Compounds preparation

CB-H₂ (1,2-C₂B₁₀H₁₂) was supplied by Katchem Ltd (Prague) and used as received. CB-(Me, allyl) (1-CH₃-2-CH₂CH=CH₂-1,2-C₂B₁₀H₁₀) and CB-(allyl)₂ (1,2-(CH₂-CH=CH₂)₂-1,2-C₂B₁₀H₁₀) were prepared according to the literature.¹²⁻¹³

4.2.2 Monolayer formation

The samples were prepared using the same method as previously published.¹⁰ The adsorbates were dissolved in mesitylene and the solutions were degassed using the freeze-pump-thaw method. A lightly n-doped silicon<100> wafer (resistivity > 10 kΩ cm) was diced into 1×1 cm pieces, cleaned in acetone by sonication for 10 min, followed by a Piranha solution for 30 min. A dip in 1% HF for 1 min removed the native oxide and yielded a hydrogen-terminated Si surface. The silicon substrate and the degassed solution were put into a reaction flask in a nitrogen glove box. The flask was then heated to 180 °C in an oil bath overnight at a constant nitrogen flux. After the reaction the samples were taken out and rinsed with ethanol, acetone, and MilliQ water. Samples were then sonicated in acetone for 10 min to remove any physisorbed material.

4.2.3 Capping layer deposition and annealing

100 nm of SiO₂ was sputtered onto monolayer-modified samples using a custom-built sputtering system. The chamber was backfilled with 1 sccm of oxygen to achieve stoichiometric SiO₂ layers. The annealing was performed using a Solaris 150 rapid thermal annealing system. The temperature ramp-up and ramp-down rates were 75 °C/s and 125 °C/s, respectively. The times given for the annealing conditions correspond to the total times including ramp-up, holding, and ramp-down phases, and the temperature was monitored at all stages.

4.2.4 SIMS measurements

In-diffused samples were first etched in HF to remove the capping layer and then cleaned with Piranha. Depth profiles were recorded using a Cameca IMS 6f system with 3 keV O₂⁺ primary ions in positive mode. Secondary ions of ¹¹B and ³¹P were detected. The measured ¹¹B concentration was converted to total boron coverage using the known isotopic ratio. The measurement chamber was back filled with O₂. Quantification and depth calibration were based on reference samples with known profiles.

4.3 Results and discussion

We followed the MLD process as previously described in Chapter 3 (Figure 4-1A).¹⁰ Three types of previously reported carborane derivatives were tested: ortho-carborane (CB-H₂), the monoallyl, monomethyl derivative CB-(Me, allyl),¹³ and the bis-allyl derivative CB-(allyl)₂.¹² (Figure 4-1B). All carborane derivatives contain ten B atoms per molecule, intended to promote high boron doping levels. The allyl groups of CB-(Me, allyl) and CB-(allyl)₂ allow reaction with hydrogen-terminated silicon and therefore the covalent grafting of the adsorbates onto the surface. CB-H₂ lacks such a reactive group and is therefore used as a control. Allylboronic acid pinacol ester

(ABAPE) has been used previously¹⁰ and serves here as a comparative control representing an adsorbate that has only a single B atom.

The MLD process is schematically shown in Figure 4-1A. Silicon substrates were cleaned and etched with 1% HF to remove the native oxide. The carborane derivatives were grafted onto the H-terminated silicon surface by the hydrosilylation reaction. X-ray photoelectron spectroscopy (XPS) was performed to study the extent of functionalization. Boron, carbon, oxygen and silicon were quantified to determine the atomic concentrations of these elements. The results are summarized in Table 4-1. Samples functionalized with CB-(Me, allyl) and CB-(allyl)₂ showed significantly higher amounts of boron than the ones with compound CB-H₂ and ABAPE. Carbon values shown in Table 4-1 are higher than arising from the adsorbates alone, which is attributed to adventitious carbon as observed before (see Chapter 3).¹⁰ Nevertheless, boron-to-carbon ratios were significantly higher for the former two cases. Figure 4-2 shows the XPS spectra of silicon substrates modified with monolayers of the three carborane derivatives. A B1s peak at about 189.6 eV is visible for the CB-(Me, allyl) and CB-(allyl)₂. No boron signal is observed for the CB-H₂. When comparing the boron contents of the monolayers of CB-(Me, allyl) and CB-(allyl)₂ with that of ABAPE, the former two show 8-10 times more boron than for ABAPE. This agrees favorably with the difference in the amount of boron atoms in the respective adsorbate molecules. Because CB-(Me, allyl) and CB-(allyl)₂ have similar structures and give similar boron contents at the surface, we used only CB-(Me, allyl) and ABAPE in subsequent analyses.

Figure 4-1. A) The monolayer doping process: a. wet etching of native SiO₂ with dilute aqueous HF yields the H-terminated silicon surface; b. grafting of dopant molecules using hydrosilylation; c. SiO₂ capping layer is sputtered onto the silicon surface with monolayers; d. a spike annealing and removing of capping layer result in a surface junction. B) Structures of the carborane derivatives and the allylboronic acid pinacol ester (ABAPE).

Table 4-1. XPS atomic percentages on silicon after monolayer formation.

Compound	B [%]	C [%]	B/C ratio	O [%]	Si [%]
CB-H ₂	0.19	26.86	0.007	29.61	43.34
CB-(Me, allyl)	9.33	29.31	0.32	19.65	41.72
CB-(allyl) ₂	10.25	43.88	0.23	15.66	30.21
ABAPE ^{a)}	1.09	34.05	0.032		

^{a)} Values of this compound reported in Ref ¹⁰.

Figure 4-2. XPS B1s spectra of silicon substrates modified with CB-H₂, CB-(Me, allyl) and CB-(allyl)₂.

A SiO₂ capping layer was deposited on the monolayers of CB-(Me, allyl) and ABAPE, and these samples were annealed at three different temperatures. Boron profiles for the CB-(Me, allyl) annealed under these conditions and ABAPE samples annealed at 1000 °C for 6 s were measured by dynamic secondary ion mass spectrometry (D-SIMS) (Figure 4-3a). The junction depth as well as the doping concentration increase as the annealing temperature increases. The carborane sample annealed at 1000 °C showed a much higher doping concentration and deeper junction compared to the ABAPE sample annealed under the same conditions (Figure 4-3a). The total amount of boron (Figure 4-3b) showed a 7.3 times increase for the carborane sample ($2.2 \times 10^{13} \text{ cm}^{-2}$) compared to the ABAPE sample ($0.30 \times 10^{13} \text{ cm}^{-2}$). Considering a 10% error in the D-SIMS measurements, these numbers agree well with the observed difference in amounts of B present in the monolayers preceding annealing.

We also annealed a sample at 1000 °C for 15 s (Figure 4-3a,b). As expected, the total amount of boron increases compared to the annealing at 1000 °C for 6 s (Figure 4-3b). However, these results also indicate that the annealing time has a smaller impact on the dopant concentration than the annealing temperature. Varying the annealing

temperature by 50 °C results in a significant change in both the highest doping concentration and the total dopant dose. On the other hand, increasing the annealing time by 2.5x changes the total doping dose only slightly, and almost no change in the highest doping concentration was observed. Furthermore, we observed a plateau in the doping profiles near the surface for annealing conditions 1, 2 and 3. This kink-and-tail behavior is attributed to the solid solubility of boron in silicon.¹⁴ As the solubility of B is related to the temperature, the highest level of doping is achieved at the highest annealing temperature. A high annealing temperature is thus needed when a high doping concentration is desired. However, the increased diffusivity of dopants at higher temperatures makes it more challenging to achieve shallow doping.

Figure 4-3. a) D-SIMS profiles of boron for the samples made by MLD using CB-(Me, allyl) (solid line) and ABAPE (dashed line), annealed at: 1) 1050 °C, 6 s (red), 2) 1000 °C, 15 s (green), 3) 1000 °C, 6 s (blue), and 4) 950 °C, 6 s (purple). b) The total boron dose of samples made from CB-(Me, allyl) annealed for 6 s as a function of annealing temperature (■). Sample made from ABAPE annealed for 6 s (●) and from CB-(Me, allyl) annealed for 15 s (■) are also shown. All concentrations and total dose measurements have errors below 10%.

The sheet resistance (R_S) of the samples was measured subsequently using the four-point Van der Pauw method. The measured sheet resistances for the carborane and ABAPE samples are shown in Figure 4-4. The R_S values of the ABAPE samples were 17, 20, 13 and 3.1 times higher than the carborane samples annealed at the same conditions. The significantly lower R_S values of the carborane samples clearly indicate

increased dopant concentrations in these samples compared to ABAPE. Since the conductivity of a sample is inversely related to the sheet resistance, the roughly one order of magnitude higher conductivities obtained by the carborane samples agrees well with the 10 times higher boron content in the adsorbate and its subsequent monolayers. These results also indicate that despite the high thermal stability of carboranes, the extent of the incorporation of the boron atoms within the crystal lattice is similar as for previously observed adsorbates under the same annealing conditions. Furthermore, atomic force microscopy measurements of the surface morphology of the silicon wafer before and after the doping cycle revealed no considerable modifications (Figure 4-5).

Figure 4-4. Four-point Van der Pauw measurements of the sheet resistance (R_s) on the samples prepared using CB-(Me, allyl) (square, ■ and □) and ABAPE (circle, ● and ○) as a function of the annealing temperature. The solid squares and circles (■ and ●) indicate the samples annealed for 6 s and the hollow square and circle (□ and ○) indicate the samples that were annealed for 15 s. Errors for the carborane samples were found to be below $\pm 1\%$ except for the sample annealed at condition 4, which had an error of 22%. For the ABAPE samples, the errors were found to be below $\pm 4\%$ except for the sample annealed at condition 3, which had an error of 13%.

Figure 4-5. AFM images of a) undoped and b) doped silicon surfaces. The rms of height in the black squares for a) and b) are 0.202 and 0.177 nm, respectively. c) and d) show the height profile from the yellow lines in a) and b) respectively.

We further studied the correlation between the annealing process and the resulting doping level. Due to the short annealing time and comparable timescales of temperature ramping, it is difficult to make a direct comparison between the different annealing conditions. To solve this issue, we employed a thermal budget¹⁵ evaluation, which takes into account the temperature dependence of the diffusivity. According to Fick's law the diffusivity of dopant atoms is defined as:

$$D = D_0 \exp \left(-\frac{E_a}{k_B T} \right), \quad (4-1)$$

where E_a is the activation energy for diffusion, k_B is Boltzmann's constant and T is the temperature. We calculated the thermal budget for each diffusion condition, which is

defined as the multiplication of D and time (t).¹⁶ Given the fact that the temperature also varies with time during the annealing process, the thermal budget can be calculated as:

$$\text{Thermal Budget} = D_0 \int \exp\left(-\frac{E_a}{k_B T(t)}\right) dt. \quad (4-2)$$

Using the temperature ramping curve followed during the annealing process, we performed numerical calculations of the thermal budget for each annealing condition. The thermal budget arises from a temperature ramp-up, a hold phase, and a ramp-down. The separate contributions of these phases to the thermal budget are shown in Figure 4-6. The ramp-up and ramp-down phases contribute to about 10% each to the total thermal budget. These become more important when shorter annealing times are used, and therefore the thermal budget calculation as presented here is most important when evaluating conditions for ultrathin doping layers.

Figure 4-6b shows the total dopant dose derived from D-SIMS and the inverse of the sheet resistance ($1/R_s$) of the samples as a function of the thermal budget. The nearly linear dependence of the sheet resistance (R_s) and the SIMS dopant dose on the thermal budget indicates that the thermal process determines the amount of boron that has diffused into the silicon. This also implies that with the CB-(Me, allyl) used in this study, the amount of boron at the silicon surface before the annealing step can be seen as an infinite source. The highest possible doping level is hence dominated by the thermal annealing step. As discussed above, the surface concentration is limited by the annealing temperature. These factors indicate that by changing the annealing temperature and time, the doping concentration and dose can be controlled independently to some extent.

Figure 4-6. a) Thermal budget of the four annealing conditions: 1) 1050 °C, 6 s, 2) 1000 °C, 15 s, 3) 1000 °C, 6 s, 4) 950 °C, 15 s. Note that the thermal budgets of ramp-up, hold and ramp-down phase are shown separately. b) Inverse of the sheet resistance ($1/R_s$) and total dopant doses derived from SIMS are also plotted to show the correlation of these with the thermal budget.

4.4 Conclusions

A novel strategy for achieving high p-doping levels in Si by monolayer doping has been presented, using carborane molecules as a rich source of boron atoms. The XPS measurements indicate about ten times more boron atoms presented on the carborane-modified monolayers compared to ABAPE samples, in line with the difference in B atoms present in these molecules. D-SIMS and sheet resistance measurements also indicated a ten times increase in the doping dose under the same annealing conditions when comparing carborane and ABAPE samples. A thermal budget evaluation indicated good correlations between the SIMS dose and the conductivity on the one hand and the thermal budget on the other hand, indicating a good control over the dopant dose by the thermal annealing conditions, also for spike anneal conditions.

4.5 References

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Fabrication of bulk planar junctionless transistors using monolayer doping

The bulk planar junctionless transistor (BP-JLT) has been proposed as an alternative device design with a better performance and an easier fabrication process. The BP-JLT device is homogeneously doped throughout the source-channel-drain region and relies on a p-n junction at the interface between the device and the substrate to electrically isolate the device. Monolayer doping (MLD) is an alternative doping technique that has been demonstrated to form ultra-shallow doping without causing crystal damage. Here, we report the fabrication of BP-JLT devices using MLD to create the doped layer. MLD provides the ultra-shallow doping that forms the device body. Characterization by contact angle measurements, X-ray photoelectron spectroscopy (XPS), and secondary-ion mass spectrometry (SIMS) on the samples showed the successful formation of a layer doped of 25 nm using MLD. I-V measurements showed functional BP-JLTs of the fabricated device.

5.1 Introduction

Based on Moore's Law, the semiconductor industry is continuously pushing technology towards smaller scales for better performance and lower fabrication costs. This downscaling trend for devices is posing increasing challenges for manufacturing.¹ New manufacturing techniques and device architectures have been proposed to keep up with the pace defined by Moore's Law. These include the implementation of silicon on insulator (SOI) wafers,² high-k gate dielectric materials,³⁻⁴ strained silicon technology⁴ and the transition from traditional MOSFETs to junctionless transistors (JLTs).⁵

Reduction of the transistor channel length following the downscaling trend requires abrupt source/drain doping for traditional transistors. Such doping poses great challenges for manufacturing. The JLT, on the other hand, is a type of device architecture in which the entire source-channel-drain region is homogeneously doped. It lacks an internal p-n junction between the source/drain and the channel region. The JLT architecture thus eliminates the need for source/drain doping and hence eases the fabrication effort. Various device geometries have been reported based on the JLT. The gate-all-around (GAA),⁶ fin field-effect transistor (finFET),⁷ ultra-thin body silicon on insulator (UTB-SOI),^{4,8} and bulk planar JLT (BP-JLT)⁹ have been demonstrated. For BP-JLTs, the junctionless transistor is fabricated on planar silicon. It relies on a p-n junction between the device body and the substrate to electrically isolate the device. Such planar design is compatible with the planar process flow in industry. Fabrication of the BP-JLT requires ultrashallow doping ($X_j \sim 10$ nm), which poses a challenge on device fabrication using traditional doping techniques.

Monolayer doping (MLD) was pioneered by Javey *et al.* in 2008.¹⁰ MLD has various advantages over traditional ion implantation techniques: (i) it avoids crystal structure damage; (ii) it is capable of doping 3-D structures and of (iii) forming ultra-shallow

junctions. The localized doping of MLD can be realized by combining MLD with lithography and dry etching techniques.¹¹ Tuning of the doping dose in MLD has also been reported using mixed monolayers (see Chapter 3)¹² or using carborane derivatives (see Chapter 4).¹³

In this chapter, a novel approach of fabricating BP-JLT devices using MLD is presented. MLD is utilized to form an ultra-shallow boron doping on the surface that becomes the BP-JLT device. Such shallow boron doping is challenging to achieve using traditional doping techniques due to the high diffusivity of boron in silicon. Using MLD we demonstrate that BP-JLTs with ultra-shallow device doping can be realized. Electrical measurements show that functional JLTs have been achieved.

5.2 Materials and methods

5.2.1 Wafer cleaning

Si (100) wafers, both n-type (resistivity 1 – 10 Ω cm) and intrinsic (resistivity >10,000 Ω cm), were subjected to standard cleaning by immersion in a beaker with 99% HNO_3 for 5 min and then in another beaker with 99% HNO_3 for 5 min to remove organic residuals. After rinsing with deionized water, the wafers were immersed in 67% HNO_3 and heated up to 95 $^\circ\text{C}$ to remove metal traces. The cleaning was finished after rinsing the wafer in deionized water and spin drying.

5.2.2 Photolithography

The photolithography process was started with a dehydration bake of the wafer at 120 $^\circ\text{C}$ for 5 min. Then an adhesion promotor (HMDS) and the photoresist (Olin OiR 906-12) were spin coated onto the wafer at 4000 rpm for 30 s for both layers. The wafer was then baked at 95 $^\circ\text{C}$ for 60 s. The exposure was performed using an EVG EV620 mask aligner with a Hg-lamp at 12 mW/cm² for 4.2 s. The exposed photoresist was developed in Olin OPD 4262 for 60 s. The development was stopped by rinsing

the wafers in deionized water. A hard bake was not performed on the wafers for easy removal of the resist with acetone. Except for the last lithography step after which the metal electrodes were deposited, the wafer was cleaned with UV-ozone for 5 min (PR100, UVP Inc.) prior to other process steps.

5.2.3 Monolayer doping

The monolayer doping procedure described in Chapter 3 was adopted in this chapter. A special beaker is used to process the 4-inch wafers.

5.2.4 Metal deposition

The metal electrodes were deposited using sputtering. The chamber was backfilled with Ar at 6.6×10^{-3} mbar. Prior to the sputtering of each material, a pre-sputter with the shutter covering the source was performed for 1 min to clean the source material.

5.2.5 Electrical measurements

Dicing tape was applied to the finished wafers. The wafers were then cut into small pieces in a dicing machine. Prior to electrical measurements, a piece was taken from the diced wafer and cleaned in acetone by sonication for 10 min to remove the particles generated during dicing. The piece was then stuck to the measurement chip with conductive tape and the devices were connected to the chip by Al wire bonding. The entire set-up was then put in a four-probe station to make electrical contacts to the chip. A Keithley 2400 was used as the source and measurement instrument. The voltage/current was applied by the instrument and the current/voltage reading were taken directly from the instrument.

5.3 Results and discussion

The fabrication process of the BP-JLT devices is schematically shown in Figure 5-1. The wafers with alignment marks pre-inscribed by photolithography and dry etching were

first cleaned and then 100 nm of thermal oxide layer was grown on the wafer. A lithography step and selective etching of the SiO_2 layer exposed the silicon underneath. After removing the photoresist, MLD was performed using a previously reported¹² procedure with allylboronic acid pinacol ester (ABAPE) as the dopant molecule. MLD was achieved by monolayer formation, application of a capping silicon oxide layer and rapid thermal annealing. This process step promises the formation of a shallow doping of boron at the accessible areas on the wafer. The thermal oxide and capping layer were then etched in buffered HF (BHF) and the wafer was cleaned again to remove carbon residuals from previous steps. Then an isolation layer of 100 nm SiO_2 was deposited using plasma enhanced chemical vapor deposition (PECVD). This layer was deposited to provide better electrical isolation and damage resistance at the metal contact pads where wire bonding was performed. Another photolithography and selective etching in BHF exposed the device areas again. The wafer was then cleaned and 20 nm of alumina was deposited by atomic layer deposition (ALD) at 300 °C. Contact holes for source and drain electrodes were selectively etched after a lithography step and a quick etch in BHF. Finally, the metal electrodes of 2 nm Cr and 100 nm Au were fabricated using photolithography and metal lift-off.

Figure 5-1 Schematic representation of the fabrication process of BP-JLT devices made using MLD. (a) The silicon wafer is cleaned and alignment marks are inscribed by photolithography and dry etching. Then 100 nm of thermal oxide layer is grown. (b) The device area is defined by lithography and BHF etching of SiO₂. (c) Grafting of the dopant molecule is achieved by hydrosilylation. (d) A thermal diffusion and removal of the SiO₂ in BHF results in the surface junction. (e) 100 nm of SiO₂ is deposited as an isolation layer and lithography is used to expose the device area. (f) 20 nm of alumina is deposited by ALD as the gate oxide. (g) Contact holes are opened on the gate oxide layer by lithography and BHF etching; h) the metal electrode of Cr and Au is formed using sputtering and metal lift-off.

Figure 5-2 shows an image of a complete wafer with BP-JLT devices. The stripes across the center are flat areas where characterization such as contact angle and XPS can be performed. Each block on the wafer consists of BP-JLTs with varying channel lengths and widths.

Figure 5-2 Photograph of the completed BP-JLTs. The two stripes across the center are flat areas where various characterizations such as contact angle, XPS and SIMS can be performed.

To confirm the successful attachment of ABAPE onto the silicon surface, contact angle (CA) and X-ray photoelectron spectroscopy (XPS) measurements were performed on the flat testing area of the wafers. The results of the CA measured before and after the hydrosilylation are shown in Table 5-1. The data were taken on five points on the wafer, one in the center and four near the edge of the wafer. The upper/lower and left/right match the orientation in Figure 5-2, with the flat side of the wafer at lower part of the image. CA measured before the hydrosilylation on hydrogen-terminated silicon showed an average static CA of $61.2 \pm 3.7^\circ$. Given the relatively large error from the measurement, this value is in agreement with the reported CA from literature for hydrogen-terminated silicon.¹⁴ After hydrosilylation, the CA increases slightly to $63.8 \pm 1.7^\circ$.

Table 5-1 Contact angle data on wafers before and after hydrosilylation with ABAPE.

Position on the wafer	Contact angle [°] before hydrosilylation	Contact angle [°] after hydrosilylation
center	59.5 ± 0.1	62.7 ± 0.2
upper	60.1 ± 0.5	62.7 ± 0.7
right	63.1 ± 0.1	63.3 ± 0.2
lower	56.8 ± 0.9	63.5 ± 0.7
left	66.5 ± 0.8	66.7 ± 0.2
Average	61.2 ± 3.7	63.8 ± 1.7

The CA measurements alone provide limited information about the monolayer coverage on the silicon surface. To further investigate the coverage, an XPS elemental scan of boron at around 191.3 eV is shown in Figure 5-3a. The boron signal is partially overlapping with the Si 2s plasmon signal, but clearly indicates the presence of boron. This confirms the successful grafting of the ABAPE monolayers onto the silicon surface. The Si spectrum in Figure 5-3b shows slight oxidation of the silicon surface as indicated by the shoulder at the higher energy side of the peak. According to literature,¹⁵⁻¹⁷ densely packed alkene molecules passivate the silicon surface and protect it from oxidation when exposed to ambient. On the other hand, Si oxidation upon MLD is observed in our work and also by O'Connell *et al.*¹⁸ Such oxidation is observed despite care being taken to remove traces of oxygen, including the freeze-pump-thaw process to de-gas the compound before hydrosilylation. The poorer protection against oxidation for ABAPE is therefore attributed to the rather short chain length of the molecule providing less good monolayer packing compared to long-chain alkenes. At the same time, in agreement with the findings by O'Connell *et al.*, we observed that this amount of oxidation has no appreciable effect on the diffusion process.

Figure 5-3 XPS measurements on a sample after the hydrosilylation step shows (a) the boron region and (b) the silicon region. (a) The green fitting curve is for the Si 2p plasmon, the dark blue curve represents the boron fitting, and the red is the sum of these two fits. (b) The silicon region shows a shoulder at the high-energy side, indicating slight oxidation of silicon.

Quantification of all four elements (B, C, O, and Si) measured by XPS is summarized in Table 5-2. The measurements from all five points taken on the wafer are in good agreement with each other. This indicates a good homogeneous monolayer across the whole wafer. The measured amount of boron at about 1.8 % is also in agreement with previously measured values, as reported in Chapter 3.¹²

Table 5-2 The XPS atomic percentages of all elements measured from the test stripes after hydrosilylation.

	B [%]	C [%]	O [%]	Si [%]
center	1.4	15.0	14.7	68.8
upper	2.0	14.3	13.2	70.5
right	1.5	13.6	14.1	70.7
lower	1.5	12.9	13.7	71.9
left	1.6	12.2	13.4	72.8
Average	1.8	13.5	13.2	71.5

MLD is capable of forming ultra-shallow junctions. To investigate the dopant distribution and to study the dependence of the distribution on the annealing temperature and time, secondary ion mass spectrometry (SIMS) measurements of the dopant profile were performed on a separate batch of flat silicon pieces that went through the monolayer doping process and were annealed at various temperatures and times. The measured profiles are shown in Figure 5-4. When comparing the profiles of samples processed at various annealing temperatures (900 °C, 1000 °C and 1050 °C) and different annealing times at the same temperature (15 s and 6 s at 1000 °C), it is clear that the annealing temperature has a higher impact on the surface dopant concentration. This is attributed to the limited solubility of B in solid Si, which increases with temperature, and is in agreement with observations reported in Chapter 4.¹³ In case a higher doping concentration is desired, a higher annealing temperature is preferred. However, increasing the annealing temperature also increases the diffusivity of the dopant. This causes the dopants to diffuse faster into the bulk resulting in a deeper junction. In this study we chose to anneal at 1000 °C at a short anneal time of only 6 s for the relatively high surface concentration and the shallow junction that can be achieved this way. This resulted in a surface concentration of $8.7 \times 10^{18} \text{ cm}^{-3}$ and a junction depth of about 25 nm.

Figure 5-4 Dopant profile measured by secondary ion mass spectrometry (SIMS). The in-diffusion was achieved at various drive-in temperatures and times, resulting in dopant profiles with different surface concentrations and junction depths.

After subsequent steps that deposit the gate dielectric and fabricate the electrodes, the finished devices were then diced into smaller pieces and connected to a measurement platform with aluminum wire bonding. Both n-type (resistivity 1 – 10 Ω cm) and intrinsic (resistivity > 10,000 Ω cm) wafers were used as substrates during fabrication. I - V measurements were done on these samples and the results on one of the BP-JLT devices are shown in Figure 5-5. The measured transistor has a channel length of 80 μm and channel width of 50 μm . The drain current (I_d) versus drain voltage (V_{ds}) shown in Figure 5-5a and b for n-type doped and intrinsic wafers, respectively, show a typical transistor behavior. The BP-JLT on an intrinsic wafer (Figure 5-5b) showed a higher conductance of the device. This is in agreement with a previous study on BP-JLTs,⁹ in which the devices on wafers with a lower background doping level showed a higher conductance. The I_d - V_{gs} curves at -0.5 V drain bias for devices on n-type doped and intrinsic wafers are shown in Figure 5-5c. The curves show that the device works in accumulation mode, which behavior for junctionless transistors has been predicted by Colinge.¹⁹ The device made on an intrinsic substrate (blue line) showed a higher threshold voltage at -2.18 V compared to the one on n-

type wafer (black line) at -0.76 V. The sub-threshold swing was very similar for both devices (0.33 and 0.34 V/dec for n-type and intrinsic wafers, respectively). We note that the off-state currents measured for both devices are on the order of 10^{-9} A, which is higher than predicted by other studies of BP-JLTs.²⁰ This is probably caused by contaminations introduced in the substrate during fabrication. It was found that metallic contaminations significantly increase the off-state current.²¹ Overall, the I - V curves shown here clearly show functional devices.

Figure 5-5 I_d - V_{ds} curves measured from the BP-JLTs fabricated on (a) n-type and (b) intrinsic wafers. (c) I_d - V_{gs} curves for BP-JLTs on n-type (black line) and intrinsic (blue line) wafers at -0.5 V drain bias. For (a) to (c), the channel length and width of the devices were 80 and 50 μ m, respectively. (d) The I_{on} and I_{off} for devices on n-type wafers with varying channel widths.

Preliminary measurements on the on/off currents in devices with different channel widths were performed, and the results are shown in Figure 5-5d. The drain bias was fixed at -0.5 V for these measurements. As expected, a wider channel shows a higher

on/off current, indicating a lower resistance of the channel. Further optimization of the devices depends on the desired application, which affects the desired electrical properties. The RTA technique combined with the thermal budget study in Chapter 4 provides a flexible route to control the dopant depth and concentration in the device by tuning the RTA temperature and time. The back-side doping level and backside bias also offer two extra control parameters.

5.4 Conclusions

We demonstrated the fabrication of bulk planar junctionless devices using monolayer doping. MLD was utilized to form an ultra-shallow doped layer on the silicon surface. SIMS measurements showed a junction depth of 25 nm whereas I - V measurements confirmed the successful fabrication of functional junctionless transistors. The behavior of the BP-JLT devices is in agreement with predictions from previous studies on BP-JLTs. The feasibility of MLD in ultra-shallow doping makes it easier to achieve the desired doping depth for BP-JLTs. The further optimization of the devices will depend on the desired application, and the desired electrical properties will have to dictate the device parameters. The BP-JLT architecture, compared to JLTs made on SOI wafers, adds an extra control parameter. This provides more flexibility in device design and fabrication.

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Monolayer contact doping from a silicon oxide source substrate

In this chapter a modified monolayer contact doping process is reported. Monolayer contact doping (MLCD) is a modification of the monolayer doping (MLD) technique. It involves monolayer formation of a dopant-containing adsorbate on a separate source substrate that is subsequently brought into contact with the target substrate, upon which the dopant is driven into the target substrate by thermal annealing. The conceptual modification of the MLCD process described in this chapter is that the previously used Si source substrate is replaced by a SiO₂ substrate, which allows the use of more easily accessible and processible silane monolayers, and at the same time provides a better capping effect which prevents the dopants to diffuse back into the source substrate. Additionally, a boron-rich carborane silane was used here to construct the monolayer that delivers the dopant, to boost the doping level in the target substrate. X-ray photoelectron spectroscopy (XPS) showed a successful grafting of the dopant adsorbate onto the SiO₂ surface. With secondary ion mass spectrometry (SIMS) we were able to conclude a similar doping level as MLD being achieved. Finally, doping of silicon nanowires using the MLCD is also demonstrated.

6.1 Introduction

The doping of silicon plays a crucial role in tuning the properties of electronic devices. The ever evolving technology in semiconductor industry drives devices to smaller dimensions in order to achieve higher performance and to reduce the costs of their production.¹⁻² In this downscaling trend, realizing shallower doping while preventing crystal damage becomes crucial.³ Monolayer doping (MLD) is a promising doping method as an alternative to ion implantation to form doped structures in silicon.⁴⁻⁶ It utilizes a reaction known as hydrosilylation⁷ to covalently bind dopant-containing alkene molecules onto the silicon surface of the target wafer. The dopant is then driven into the silicon through high-temperature annealing. Covalent anchoring of alkenes on silicon through hydrosilylation requires the preparation of a hydrogen-terminated silicon surface, which is achieved by removing the native oxide layer by wet fluoride etching. Moreover, a capping layer of SiO₂ is deposited on the monolayer prior to the thermal annealing step which is required to prevent the dopant from escaping the target surface during the heating process. This capping layer needs to be removed after the drive-in process again by fluoride etching. These fabrication steps can be incompatible with the substrate, especially when aiming for devices that are fabricated on silicon-on-insulator (SOI) wafers. Removal of the capping layer can cause the backside oxide layer to be removed as well.

Yerushalmi *et al.* proposed a monolayer contact doping (MLCD) approach which solves the material incompatibility issue.⁸ MLCD features a dopant monolayer to be formed on a separate silicon substrate which functions as the source substrate. This source substrate is brought into contact with the target substrate that needs to be doped, and in a thermal annealing step, the dopant is driven into the target substrate. The source substrate is then discarded, leaving the doped layer on the target substrate. With MLCD, the target substrate does not have to undergo any wet chemistry and post-doping processing. Higher levels of doping can, in principle, be

achieved by repeating the MLCD process using multiple source substrates on a single target substrate. Drawbacks of MLCD are the use of monolayers on H-terminated silicon, which are less accessible than, for example, the widely employed monolayers of silanes on silicon oxide, and the use of silicon as the source substrate which causes that the dopants will diffuse into this substrate during the annealing step with equal probability as into the target.

In this chapter we propose an improved MLCD process, based on the use of SiO_2 as a source substrate instead of silicon. The dopant monolayer formation can now be based on the widely used silane chemistry instead of hydrosilylation. The SiO_2 source substrate used here acts at the same time as a capping layer thus preventing the loss of dopant atoms by diffusion into the source substrate. Furthermore, we use a boron-rich carborane derivative (also employed in Chapter 4) to boost the doping level in the target substrate. Contact angle, X-ray photoelectron spectroscopy, secondary ion mass spectroscopy, and resistance measurements have been performed to study the monolayer on the source substrate and to explore the process of doping by this modified MLCD process. Finally, the method is applied to silicon nanowires to create doped nanowires.

6.2 Materials and methods

6.2.1 Monolayer formation on the source substrate

Silicon wafers were cleaned by immersion in 99% HNO_3 and subsequently in 69% HNO_3 at 95 °C to remove organic and metal contaminations, respectively. After removing the native oxide in 1% HF, the wafers were loaded into a thermal furnace, and a 100 nm oxide layer was grown at 1100 °C for 45 min. After cooling down, the wafers were diced and stored in a wafer box. Prior to each surface modification, one or several pieces were taken from the stock and cleaned in acetone by sonication for 10 min to remove particles generated during dicing and then cleaned in Piranha

solution (98% H_2SO_4 and 30% H_2O_2 mixed at a 3:1 ratio) for 30 min. The pieces were then transported into a nitrogen glovebox and temporarily stored there. A silane-functionalized carborane compound, 1-triethoxysilyl-2-methyl-carborane, to be used as the dopant adsorbate, was synthesized using previously reported methods.⁹⁻¹⁰ Glassware used for the silane monolayer formation was baked in an oven at 120 °C for at least 3 h to remove any moisture. The compound was dissolved at 1% v/v in toluene, obtained from a solvent purification system MB-SPS-800. The silane solution was then put in a reaction flask and transported into the nitrogen glovebox. In the nitrogen glovebox, the SiO_2 pieces were loaded into the flask with the silane to allow the monolayer to be formed. The glassware was sealed by a glass cap with a valve. The whole setup was then taken out of the glovebox with the valve closed. A balloon filled with dry nitrogen was attached to the setup and the valve was opened to keep a positive pressure inside the setup. This setup was then left in the fume hood overnight at room temperature. After the reaction, the source wafer pieces were taken out and rinsed by ethanol (puriss.), acetone (pure) and Milli-Q water (resistivity >18 M Ω cm). Subsequently, they were sonicated in acetone for 10 min to remove any physisorbed material and stored in a sample box.

6.2.2 Rapid thermal annealing

The rapid thermal annealing (RTA) was performed in a Solaris 150 rapid thermal annealing system. Prior to annealing, the target silicon substrate was cleaned by Piranha solution for 30 min and dipped in 1% HF for 20 s to remove the native oxide. The source substrate was brought into contact with the target substrate and loaded into the RTA system. The temperature was ramped up at 75 °C/s to reach 1000 °C, held for 6 s at 1000 °C, and then ramped down at 125 °C/s to reach 400 °C. Subsequently, the substrates were taken out and left to cool down to ambient temperature.

6.2.3 XPS and SIMS measurements

The X-ray photoelectron spectroscopy (XPS) measurements were performed as described in Chapters 3 – 5.

The time-of-flight secondary ion mass spectrometry (TOF-SIMS) measurements were performed at an Ion-ToF TOF-SIMS IV instrument in dual-beam positive mode. The analysis beam was a 25 keV Bi^+ ion beam with diameter of 3 μm . The sputtering beam was a 2 keV O_2^+ beam. Depth scaling calibration was based on reference samples with transitions at known depth. Optical profilometry was used on a few craters after the measurement to cross check with the depth profiling. Concentration scale calibration was based on a reference ^{11}B implant with a known profile. Prior to the measurements on the source substrates with a silane monolayer, performed to determine the initial amount of dopant, 10 nm of Si was sputtered onto the substrate to cap the monolayer.

6.2.4 Electrical measurements

Sheet resistances were measured using the method described in Chapter 3. Electrical measurements on silicon nanowires were performed on samples fabricated on SOI wafers. The backside oxide was 145 nm thick and the device layer was 66 nm thick. The nanowires had the same geometry as the ones previously reported.¹¹ Electrical measurements were performed on a probe station by mounting the sample on an isolated sample holder and directly contacting it with the probes utilizing a contact pad fabricated on the sample. The four-point probe method was used to determine the resistance of the nanowires.

6.3 Results and discussion

The proposed monolayer contact doping process is schematically shown in Figure 6-1. The silane carborane derivative used here was synthesized using previously reported

methods.⁹⁻¹⁰ The monolayer grafting onto the SiO_2 source substrate was accomplished by using a 1% v/v solution of the silane carborane in toluene at room temperature overnight. The dopant was transferred into the target substrate by bringing the source substrate into contact with a target substrate and annealing them at 1000 °C using rapid thermal annealing (RTA).

Figure 6-1 The monolayer contact doping process using a silicon oxide source substrate. A silicon wafer with a 100 nm layer of thermal SiO_2 is used as the source substrate, and (a) is functionalized with a monolayer of a silane carborane. (b) The source substrate is brought into contact with the target silicon substrate and both of them are loaded into a thermal furnace for rapid thermal annealing (RTA). (c) The dopants are driven into the target substrate forming a doped surface layer.

The formation of the silane monolayer on the source substrate was initially evidenced by contact angle (CA) measurements. After cleaning, the starting oxide-coated substrate was highly wetting ($\text{CA} < 20^\circ$). After monolayer formation, the CA had increased to 81.8° . The stability of the monolayer was explored by re-measuring the CA (81.5°) of the monolayer after three-week storage in air, which indicates the monolayer is stable for at least 3 weeks under normal conditions at room temperature. Upon RTA, the monolayer is decomposed and the dopant atoms are driven into the target substrate. This was witnessed by a dramatic decrease of the contact angle of the source substrate down to 7.1° .

X-ray photoelectron spectroscopy (XPS) was performed on the source substrate right after the monolayer formation as well as after a three-week storage in air. The boron

signals at 189.7 eV are shown for both substrates in Figure 6-2. Quantitative measurements of the elements B, C, O, and Si are summarized in Table 6-1. The ratio of silicon to oxygen was found to be close to 1 : 2, which is expected for a SiO_2 surface. The amount of boron on the samples (7.26%) is of the same order of magnitude as obtained for a monolayer of an alkene-functionalized carborane on H-terminated silicon (9.33%) that was used in MLD (see Chapter 4). This indicates a similar amount of boron is present on the surface of the MLCD source substrate. The amount of boron on the surface after three-weeks storage was found to be at the same level (6.27%) as the freshly prepared surface. The B to C ratios were higher for the silane monolayers than for the alkene monolayer, indicating less adsorption of adventitious carbon.

Figure 6-2 XPS measurements on SiO_2 -covered Si wafer pieces with carborane silane monolayers showing the boron signal at 189.7 eV for samples (a) right after the monolayer formation and (b) after three-week storage in air.

Table 6-1 Elemental composition of carborane silane monolayers on oxide-covered Si substrates measured by XPS.

	B [at. %]	C [at. %]	O [at. %]	Si [at. %]
Freshly prepared	7.26	16.28	52.61	23.86
3-week storage in ambient	6.27	11.58	56.53	25.63
CB-(Me, allyl)*	9.33	29.31	19.65	41.72

* A monolayer of an alkene-modified carborane attached to H-terminated silicon, as measured previously (see Chapter 4).¹²

After the monolayer formation, the source substrate was brought into contact with a target substrate upon which the substrate stack was annealed at 1000 °C for 6 s in an RTA process to drive the dopant into the target substrate. A single source substrate was used to dope three intrinsic silicon target substrates (samples 1, 2, and 3) consecutively in order to monitor the depletion of boron from the source. The sheet resistance (R_s) of these targets was subsequently measured (Figure 6-3).

Figure 6-3 Sheet resistance (R_s) measurements of intrinsic silicon samples that were consecutively doped by a single SiO_2 source substrate functionalized with a monolayer of a carborane silane (samples 1 to 3) and of an intrinsic wafer that received no doping (4). The gray line indicates the R_s measured on an intrinsic silicon surface that was doped using MLD with a carborane alkene (see Chapter 4).

Comparing the R_s of the target doped by MLCD (sample 1) to the ones achieved from MLD using carborane alkene derivatives on H-terminated silicon (gray line in Figure 6-3, reported in Chapter 4), they are of the same order of magnitude, and both are two orders of magnitude lower than the resistance of the intrinsic silicon substrate before doping (sample 4, Figure 6-3). This shows that using a silane derivative of the dopant molecule and the SiO_2 of the source wafer as a backside capping layer effectively leads to (at least) the same level of doping as realized by MLD. The slightly lower R_s achieved by MLCD is attributed to the SiO_2 layer that is grown using thermal oxidation, which provides a higher quality oxide compared to sputtered SiO_2 that is generally used as a capping layer in MLD, and consequently lower losses of the dopant atoms are observed. This is in agreement with the observation by Javey *et al.*⁴ that the Si:O stoichiometry of the silicon oxide capping layer has an effect on the diffusion efficiency.

Apparently, the source substrate is capable of performing multiple doping steps of different targets. This is witnessed by the sheet resistance of samples 2 and 3 in Figure 6-3. The gradual increase of R_s from samples 1 to 3 indicates decreasing amounts of dopants being incorporated into the targets. However, the capability of performing multiple doping steps with the same source substrate indicates that the dopant on the source substrate is not fully depleted during the first RTA step. This offers the possibility to re-use the source substrate or to use multiple annealing steps in order to tune the level of doping.

Secondary ion mass spectrometry (SIMS) was used to investigate the doping depth and boron profile of a target substrate that underwent MLCD (Figure 6-4). These findings were compared to a profile obtained for a MLD-doped sample using a carborane alkene under the same RTA conditions (see Chapter 4). The MLCD approach resulted in a higher surface concentration compared to the MLD sample. The dopant extends to roughly the same depth in both cases, although the MLCD

sample shows a steeper profile. The total area dose of the dopant for MLCD was $4.4 \times 10^{13} \text{ cm}^{-2}$, while the one for MLD is $2.2 \times 10^{13} \text{ cm}^{-2}$. This agrees well with the results from the R_s measurements, and confirms that the modified MLCD process is capable of reaching a similar level of doping as MLD. Given that MLCD requires minimum substrate preparation and avoids material incompatibility issues, this makes MLCD a promising alternative to MLD for the doping of silicon structures, in particular on SOI wafers where the use of fluoride etching must be avoided.

Figure 6-4 Boron dopant profiles measured by time-of-flight secondary ion mass spectrometry (TOF-SIMS) on a MLCD sample (black solid line), and on a MLD-doped sample using a carborane alkene (gray dashed line, see Chapter 4), annealed under the same RTA conditions.

In the foregoing discussion it was indicated that the dopant was not fully depleted after the first annealing step. To quantitatively study the relation between the amount of dopant in the monolayer on the source substrate and of the dopant that diffused into the target during RTA, a carborane silane monolayer-covered source substrate was measured with SIMS to determine the amount of dopant per area. The measured areal dose was $2.3 \times 10^{15} \text{ cm}^{-2}$. The surface density of SiO_2 can be easily determined using the density of SiO_2 ¹³ and the molecular weight of SiO_2 ¹³ using the following expression:

$$\left(\frac{\rho N_A}{M_w} \right)^{2/3}, \quad (6-1)$$

where ρ is the density of SiO_2 , N_A is Avogadro's constant, and M_W the molecular weight of SiO_2 . Using the above expression, the surface density of SiO_2 was calculated to be $7.9 \times 10^{14} \text{ cm}^{-2}$. Given that each carborane molecule has ten boron atoms, the packing density of the monolayer was then calculated to be 29%. The lower packing density is attributed to the larger footprint of the adsorbate molecules due to its large carborane headgroup. Comparing this areal dose to the one measured on the silicon target after annealing (sample 1), we note that the in-diffusion efficiency of the doping process is only about 2%. This low diffusion efficiency is attributed to the limited solid solubility of boron in silicon and the low thermal budget, arising from the short annealing time used here during the RTA step, as discussed in Chapter 4.

As a proof of concept, the improved MLCD process was applied to the doping of silicon nanowires on a SOI wafer. The silicon nanowires were prepared on a SOI wafer with a similar architecture as recently reported by Duffy *et al.* (Figure 6-5).¹¹ The wires were 10 μm long and 40 nm wide. Four contacts extended from each wire to allow four-point probe measurements. Preliminary data for the electrical resistance of the wires was obtained before and after MLCD, giving values of 66 G Ω and 7 G Ω , respectively. The measured lower resistivity clearly indicates the incorporation of the dopant into the nanowires. This shows the capability of doping silicon nanowires without putting them through the chemical processes that involve monolayer formation of the wires themselves, as well as capping layer application and removal.

Figure 6-5 Schematic representation of the nanowire structure used here. The current is driven through A and D while the voltage is measured between B and C.

6.4 Conclusions

An improved MLCD process was developed in this study. A Si wafer with a thermal SiO_2 layer was used as the source substrate. A silane-functionalized carborane derivative was used as the dopant molecule. The silane reaction on the silicon oxide was used to graft the molecules onto the source surface. This methodology provides two main advantages to the MLCD process: (i) silane chemistry is more developed and employs less harsh reaction conditions than the monolayer formation on H-terminated silicon, and (ii) the use of silicon oxide provides a better capping function than silicon.

Upon annealing, R_s and SIMS measurements revealed similar dopant incorporation levels as obtained by MLD. We also found that the source substrate was capable of performing doping on multiple target substrates by repeating the annealing on other target substrates in series using the same source substrate. By quantifying the dopant areal doses on the source and target wafers, the dopant diffusion efficiency was found to be only 2%. This offers potential for re-using the source substrate.

Finally, the improved MLCD process was applied to the doping of silicon nanowires prepared on a SOI wafer. The doping of such nanoelectronic structures is challenging by MLD because of material compatibility issues with the wet chemical steps in this

process. The MLCD doping provided a straightforward doping of the silicon nanowires as witnessed by a strongly lowered resistance of the wires after doping. All in all, the modifications of the MLCD process developed here will promote the application in future nanoelectronic device fabrication.

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Summary and outlook

The evolution of the semiconductor industry calls for new techniques to address the challenges arising from the downscaling trend known as Moore's law, which has brought electronic devices into the nano-regime. Monolayer doping (MLD) is an interesting alternative for the currently mostly employed ion implantation to introduce a dopant into silicon. The MLD technique is capable of forming ultra-shallow doping without causing crystal damage to the substrate. It is also capable of doping non-planar surfaces.

In this thesis, we have addressed a variety of conceptual novelties to MLD. We demonstrated the tuning down of the doping level using the mixed-monolayer doping concept and the tuning up using carborane clusters. Being able to control the doping level extends the versatility of MLD. Furthermore, the fabrication of junctionless transistors, as well as the modified monolayer contact doping (MLCD) and the doping of silicon nanowires using this technique, have demonstrated the versatility of the MLD and MLCD in device fabrication.

In Chapter 3, we have reported the tuning down of the doping level using mixed monolayers. The dopant adsorbate, allylboronic acid pinacol ester (ABAPE) or diethyl vinylphosphonate (DVP), was mixed with a dummy alkene that lacks the dopant. The mixing ratio was tuned between 100% to 0.1% of the dopant adsorbate. Contact angle measurements, X-ray photoelectron spectroscopy (XPS) and Auger electron spectroscopy (AES) confirmed the grafting of the dopant adsorbate and the tunability of the surface concentration by the mixing ratio in solution. Secondary ion mass spectrometry (SIMS) and electrical measurements showed a tuning of the doping dose in the silicon substrate by one order of magnitude.

In Chapter 4, carborane clusters have been used as the dopant to enhance the doping level in MLD. The carborane has ten boron atoms in each molecule compared to only one boron atom in ABAPE. This higher amount of boron can effectively boost the doping level by ten times. This was qualitatively and quantitatively confirmed by XPS, SIMS and electrical measurements. The SIMS data showed the dependence of the doping concentration on the annealing temperature. A thermal budget analysis revealed that the resulting doping dose depended on the annealing conditions.

In Chapter 5, MLD has been utilized to fabricate bulk planar junctionless transistors (BP-JLTs) which require an ultra-shallow doping to be formed on a silicon surface. With MLD, such an ultra-shallow junction can be created. MLD in combination with the BP-JLT device design offers a JLT architecture that is compatible with planar processing to fabricate transistors. SIMS measurements indicated the successful shallow doped layer of the active device areas. Electrical measurements showed that functional transistor devices had been made. The backside doping level and backside bias also offer two extra parameters to tune the device performance.

In Chapter 6, monolayer contact doping (MLCD) has been modified by replacing the commonly used silicon source substrate by SiO_2 . This modification changed the monolayer grafting processing to a more accessible silane reaction, while at the same time the SiO_2 acts as a more efficient backside capping layer during the annealing process. SIMS and electrical measurements showed that a similar, or even slightly higher, doping level can be reached compared to MLD. When comparing the dopant concentrations on the source (before annealing) and target substrates (after annealing), SIMS measurements showed that less than 2% of the dopant adsorbate was incorporated into the silicon substrate during the annealing step. Using this method, the doping of silicon nanowires was demonstrated in preliminary test experiments.

To conclude, we have demonstrated the tuning capability of MLD both down and up, by mixed monolayer doping or by using carborane clusters as the dopant, respectively. Furthermore, the capability of forming ultra-shallow doped layers by MLD has been employed in the fabrication of BP-JLTs. MLD has been shown to dope substrates that are incompatible with the wet chemistry involved in MLD. All these capabilities demonstrated in this thesis extend the versatility of MLD, and promote it as an interesting candidate to be adopted in mass scale for the doping of silicon in semiconductor industry.

In the future the optimization of the junctionless transistors fabricated using MLD can be achieved based on the desired application. The design of BP-JLTs offers additional parameters to tune the device performance. This junctionless design can also be utilized for silicon-based sensing applications with the gate electrode removed and the channel area exposed for attaching analytes. The thermal budget study in Chapter 4 and the concentration dependence on the annealing temperature reveals a certain flexibility in tuning the concentration and dose by varying the annealing temperature and time. This tuning capability can be further explored to reach a level of independent control of doping concentration and depth in MLD, which is difficult to achieve by other diffusion-based doping techniques.

Samenvatting en vooruitblik

De ontwikkeling van de halfgeleiderindustrie vraagt om nieuwe technieken om de uitdagingen aan te kunnen die voortkomen uit de miniaturisatietrend, beter bekend als de wet van Moore, die elektronische schakelingen naar het nanogebied gebracht heeft. Monolaag-dotering (MLD) is een aantrekkelijk alternatief voor ionenimplantatie, wat nu de meest gebruikte techniek is om dotering in silicium aan te brengen. De MLD-techniek kan een ultradunne dotering vormen zonder schade aan te brengen aan het kristalrooster van het substraat. MLD kan ook niet-vlakke oppervlakken doteren.

In dit proefschrift hebben we verschillende conceptuele innovaties voor MLD besproken. We hebben aangetoond dat het doteringsniveau naar beneden bijgesteld kan worden via gemengde monolaag-dotering en naar boven door het gebruik van carboraanclusters. Daarnaast is de mogelijkheid om ultradunne gedoteerde lagen te vormen via MLD gebruikt in de fabricage van vlakke transistors zonder junctie. Monolaag-contactdotering (MLCD) is gebruikt om substraten te doteren die niet compatibel zijn met de vloeistoffen betrokken bij MLD. Alle mogelijkheden, zoals aangetoond in dit proefschrift, breiden de veelzijdigheid van MLD uit en brengen MLD voor het voetlicht als een aantrekkelijke optie in de grootschalige dotering van silicium in de halfgeleiderindustrie. Meer details zijn te vinden in de Engelse versie van de samenvatting.

In de toekomst kan de optimalisatie van junctieloze transistors, gemaakt via MLD, gebaseerd worden op de gewenste toepassing. Het ontwerp van vlakke junctieloze transistors biedt extra parameters om de prestaties van elektronische schakelingen te regelen. Dit junctieloze ontwerp kan ook gebruikt worden voor silicium-gebaseerde sensortoepassingen waarbij de gate-elektrode verwijderd is en het kanaal beschikbaar is voor het binden van analyten. De studie van het thermisch budget in Hoofdstuk 4

en de concentratie-afhankelijkheid van de doteringstemperatuur tonen een zekere flexibiliteit in het fijnregelen van de concentratie en dosis door het variëren van de doteringstemperatuur en de tijd. Deze regelmogelijkheden kunnen verder onderzocht worden om een onafhankelijke controle over de doteringsconcentratie en -diepte in MLD te behalen, wat moeilijk te bereiken is met andere diffusiegebaseerde doteringstechnieken.

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About the author

Liang Ye was born on 12 July, 1985 in Nanjing, an eastern city of China. He received his Bachelor degree in Materials Science in Nanjing University in 2008. Then he joined the research group of Prof. Haixiong Ge in the same University where he focused on nanoimprint lithography and other micro-/nano-fabrication techniques. His master thesis was entitled: "The Fabrication of Sub-Micrometer Free-Standing Metal Grating with Nanoimprint Lithography".

In 2011, after being stuck in one city for more than 25 years, he decided to make a giant leap in his life and eventually landed in the research group of Prof. Jurriaan Huskens as a PhD candidate at the University of Twente in the Netherlands. He studied the doping of silicon using molecular monolayers. He focused on the tuning of the doping dose and application of this technique in the fabrication of transistors.