VERTICAL HYBRID INORGANIC-ORGANIC NANOELECTRONIC DEVICES

Janine Wilbers

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Janine G. E. Wilbers

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VERTICAL HYBRID INORGANIC-ORGANIC NANOELECTRONIC DEVICES

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This thesis is dedicated to my mother.

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Introduction

This thesis comprises different concepts for (vertical) hybrid inorganic-organic nanoelectronics devices. The work was financially supported from the NWO-nano ("Stichting voor de Technische Wetenschappen, STW") program, grant no. 11470 "Organic Semiconductor Vertical Quantum Dots".

Hybrid inorganic-organic nanoelectronics devices can be seen as structures that are at least in one dimension in the sub-micrometer regime and which are built up of inorganic materials and organic materials. In most cases the stiff inorganic matter is forming the electrode material while the organic matter is used as the active component. What is the reason for the implementation of organic materials into electronic devices? In 1974 Aviram and Ratner predicted that a single molecule can function as a molecular switch [1]. The utilization of molecules as components in electronics would allow for an enormous downscaling of electronic circuits which might extent Moore's Law, which predicts that the number of elements on one integrated circuit is doubled every two years [2, 3]. The possibilities for organic materials in nanoelectronics devices are expected to be huge due the feasibility of chemical modification. Research on "organic electronics" comprises single-molecules [4], self-assembled monolayers [5], organic single-crystals [6, 7], organic semiconductors [8] and pure carbon-based materials [9].

However, contacting molecules for investigating their properties is not straightforward. In this thesis, several device structures for contacting and electrical characterization of organic materials are discussed. Chapter 2 gives a brief introduction about organic electronics especially of organic field-effect transistors and the charge transport mechanisms in organic materials. In Chapter 3, the experimental methods utilized for the fabrication of our vertical hybrid nanodevices discussed in Chapters 4 – 6 are explained. The fabrication and electrical characterization of large-area, symmetric metal- molecular monolayer-

metal junctions with ultrasmooth template-stripped bottom electrodes and top contacts applied by wedging transfer are covered in Chapter 4. The soft-landing technique wedging transfer was also used for top-contacting thin films of organic semiconductors. These top-contacts were subsequently used as an etch mask to fabricated vertical metal- organic semiconductor- metal pillar structures. We fabricated these pillar structures as two-terminal devices with source and drain electrodes (Chapter 5) as well as three-terminal devices with the addition of a gate electrode (Chapter 6). The trapping of DNA over vertical nanogaps towards a chip to electrically detect hypermethylated DNA for early cancer diagnostics is discussed in Chapter 7.

So far, three-dimensional (3D) devices with relatively thick organic semiconductor films of 10 to 100 nm (Chapter 5 and 6) and two-dimensional (2D) devices with organic thin films (5 nm) (Chapter 5) and self-assembled monolayers (Chapter 4) have been realized and electrically investigated. In Chapter 8, we introduce the fabrication of nanochannels with openings below 10 nm. These nanochannels will in the future be filled with molecules to enable one-dimensional (1D) molecular transport.

This introduction chapter finishes with an outlook for the realization of zero-dimensional (0D) hybrid nanoelectronics devices namely few-electron/ few-hole organic semiconductor vertical quantum dots. For this goal the vertical organic field-effect transistor architectures described in Chapter 6 is proposed to be confined in the vertical dimension by very thin organic films and also in the lateral dimension by first reducing the pillar diameter and secondly by applying a side-gate.

In summary, this thesis focuses on investigating the electrical properties of organic materials in 3D and 2D configurations, providing efficient ways for electrical contacting and device fabrication. It further suggests methods to proceed to building to 1D and 0D devices, which promises interesting physics to investigate in the quantum mechanical regime.

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Chapter 2

Theoretical background

In this Chapter, a short overview of organic electronics is given. The working principle of organic field-effect transistors is described and the relevant properties of organic semiconductors are covered. At the end of this Chapter, the charge transport mechanisms in organic monolayers and organic semiconductors are discussed.

2.1 Organic Electronics

Organic semiconductors (OS) are currently attracting a lot of attention due to a wide range of applications in photonics and electronics industry like flat-panel displays, flexible organic transistors, and organic photovoltaics [1, 2]. Organic molecules cannot compete with the electrical performance of crystalline silicon with respect to excellent computational power, high transistor densities or high switching speed operations and they are not expected to replace silicon technology [3, 4]. Lots of effort was already done to chemically modify organic semiconductors in order to render them more conductive and increase their stability in ambient conditions [5]. However, since most OS can be processed from solution at room temperature, they are compatible with numerous (flexible) substrates and they can be chemically modified with respect to the application, there is a huge variety of niche products for which organic semiconductors are extremely interesting like low-cost radio-frequency identification tags, sensors or optoelectronic equipment [6-8]. Possible low-cost, large-area examples are sensors [9, 10], organic transistors [6], organic solar cells [11, 12], and organic light-emitting diodes (OLEDs) [1]. Some of these applications became already commercial available like e.g. the OLEDs.

In the following section the working principle of organic field-effect transistors and different geometries are discussed. The consecutive sections cover the definition of organic semiconductors and their charge transport characteristics.

2.2 Organic field-effect transistors

An organic field-effect transistor (OFETs) consists of three components: a thin organic film, an insulating layer and three (metallic) electrodes, see Figure 2.1. The three electrodes are the source (S) through which the charge carriers are injected into the active organic layer, the drain (D) through which the charge carriers exit the organic semiconductor, and the gate (G) which electrostatically tunes the carrier concentration (and character) of the conductive layer in the organic semiconductor. The gate electrode is separated from the organic semiconductor by the insulating layer (gate dielectric), the carrier concentration (and hence the conductivity) of the organic semiconductor is modified by attracting or repelling charge carriers from the conductive channel due an electric field.

Figure 2.1. Schematic architectures of planar OFETs. (a) The OS is applied on top of pre-patterned source and drain electrodes on the gate dielectric; (b) the OS is applied on the gate dielectric and source and drain contacts are formed on top of the OS; (c) top-gated device with pre-patterned source and drain electrodes; (d) top-gated device with source and drain electrodes formed on top of the OS.

An OFET is essentially a parallel-plate capacitor and the carrier layer is accumulated inside the OS in close vicinity to the gate electrode. The OFET operation takes place in this accumulation regime, which either accumulates holes or electrons. For p -type organic semiconductors, the conductivity of the active channel is increased when a negative gate voltage is applied relative to the source. Since electrons are the charge carriers in n -type organic semiconductors, the enhancement of the conductivity is achieved with the application of a positive gate bias relative to the source [6]. The basic principle of charge carrier flow in OFETs upon application of a gate bias is illustrated in Figure 2.2.

Figure 2.2. Charge carrier flow in (a) *n*- and (b) *p*-type planar organic field-effect transistors [6].

The charge density at the dielectric is equal on both sides but with opposite sign. In the low drain voltage regime, the channel conductance is proportional to the drain and gate voltage according to Ohm's law which is called the linear regime. When the drain voltage is increased, a point is reached at which it is equal to the gate voltage. A pinch off of the channel occurs and the current of the channel becomes independent of the applied drain voltage and the saturated regime is reached. The two regimes are given by the following equations:

$$I_{Dlin} = \frac{W}{L} \mu C_i (V_G - V_T) V_D - \frac{1}{2} V_D^2 \quad (2.1)$$

$$I_{Dsat} = \frac{W}{2L} \mu C_i (V_G - V_T)^2 \quad (2.2)$$

with W being the channel width and L the channel length, μ is the mobility, C_i is the capacitance of the insulator per unit area and V_G , V_D and V_T are the gate voltage, drain voltage and threshold voltage which includes several potential drops through the gate-dielectric-OS stack [3, 13]. The quadratic term for the linear current can be neglected for the limit $V_d \ll V_g$, and the current in the linear regime is expressed by

$$I_{Dlin} = \frac{W}{L} \mu C_i (V_G - V_T) V_D. \quad (2.3)$$

The OFET performance is highly influenced by the device structure and the material properties. For application in for example OLEDs, sufficiently large current densities are a requirement [14]. In order to reach high current densities, either the channel lengths have to be reduced which is not straightforward in the case of planar devices or the mobility should be increased. Planar channel lengths in the sub-100 nm range can only be achieved with expensive sophisticated nanolithography techniques, which are not suitable for low-cost, large-area applications. The OFET performance is highly influenced by the device structure and the material properties. Furthermore, scaling-down planar OFET architectures results in increasing influence of the contact resistances which reduces the enhancement of the device performance. The contact resistance can be decreased in devices with a staggered architectures in which the gate electrode is applied on top of the organic semiconductor. Thereby, the charge transfer can take place over an area expanding the source/drain electrodes [15-17].

Vertical transistors have an organic semiconductor sandwiched between the source and drain electrodes and the current flow is thus perpendicular to the substrate. The gate electrode is either completely surrounding the metal-OS-metal vertical stack or applied only from one side which is depending on the device structure. An example of a vertical OFET with a surrounding side-gate like we were working on in Chapter 6 is schematically illustrated in Figure 2.3. Vertical organic field-effect transistors (VOFETs) are very attractive with respect to scaling down transistor since the channel length can be easily scaled down to the nanometer regime as it is given by the thickness of the organic layer [18].

Figure 2.3. Schematic example of a vertical OFET with an organic semiconductor sandwiched between source and drain electrodes and a side-gate.

VOFETs are presently just at the beginning of their development, and reports on vertical device structures are still few in comparison with planar devices. However, the number of vertical organic transistors is increasing over the last ~20 years, an overview of the number of publications on vertical organic transistor structures given in Figure 2.4 [18]. In order to really estimate the potential of VOFETs, the complete working principles have to be understood, therefore a lot of research is required in this field. Difficulties are mainly given by the huge variety of device structures leading to output data which is challenging for comparison. Depending on the device architecture it is expected that the conduction does not take place in a two-dimensional conductive channel along the gate dielectric but is more given by a complex three-dimensional structure through the bulk of the OS [19]. However, this is highly dependent on the structure. For devices with a surrounding gate electrode, we are expecting to have a working principle comparable to that of an planar transistor with a conductive channel at the circumference of the vertical transistor. The possibility of fabricating vertical

devices that operate at low voltages in combination with device performances comparable to their planar counterparts now already shows their great potential [20, 21]. Low-voltage operation is favored since OS are supposed to be utilized in large-area, low-cost electronics which require low power consumption [22].

Figure 2.4. Overview of the number of publications on vertical organic field-effect transistors with different device structures between 1994 and 2015 [18].

When looking at the design of VOFETs, the majority is fabricated with a step-edge on which the organic semiconductor is vapor-deposited or applied from solution with bottom as well as top gate electrodes. Some examples of such a step-edge devices reported in literature are shown in Figure 2.5.

Figure 2.5. Examples for step-etch vertical organic field-effect transistors. (a) VOFET with graphene-OS-metal heterojunctions [21]; (b) VOFET on a flexible substrate [23]; (c) all-organic VOFET [24].

In the case of step-edge VOFETs, the organic semiconductor is covering a pre-defined edge. The gate contact is generally formed along the full length of the organic film, so that the charge carriers can flow between the source and drain contacts in a conductive channel comparable to the mechanism known from planar OFETs [18]. Another very promising example of a low-voltage VOFET is based on interdigitated vertical sub- μm channels with highly doped silicon as the gate material covered with a SiO_2/Al_2O_3 stack as gate dielectric [20]. On these trenches metal electrodes were deposited as source and drain electrodes followed by the organic semiconductor (see Figure 2.6).

Figure 2.6. Example of a VOFET based on (a) grating of interdigitated trenches [20].

The VOFET design described in this thesis is different to these architectures as the vertical metal-OS-metal stack is completely surrounded by the dielectric and gate electrode. The dimensions are in the sub- μm regime in the vertical as well as the lateral regime. Furthermore, each VOFET is contacted separately.

2.2.1 Soft-landing techniques for top-contacting of organic thin films

In contrast to vertical architectures with pre-defined electrodes on which organic materials are deposited, the fabrication of devices with contacts on top of organic thin films and/or patterned organic layers is not straightforward. The reason is their vulnerability to direct metal evaporation and most chemicals used in standard lithography procedures like acetone, isopropanol, dimethyl sulfoxide (DMSO), methyl isobutyl ketone (MIBK) and tetramethylammonium hydroxide (TMAH) [19, 25]. Direct metal deposition onto self-assembled monolayers (SAMs) or organic thin films results in metal penetration which often leads to electrical shorts and unclear interfaces with metal atom impurities due to metal filaments. A variety of techniques already exists which avoids damage of the organic materials during top-contacting. Most so-called soft-landing techniques are used for molecular junctions in which a self-assembled monolayer is sandwiched between source and drain contacts. Examples are transfer printing [26, 27], conductive polymers as contacts [28], liquid metals [29], lift-off float-on (LOFO) [30], polymer-assisted lift-off [31] and wedging transfer [32, 33]. Moreover, graphene was proven to be suitable as a non-destructive top contact for organic thin films [34]. Very interestingly, gently top-contacted, vertical transistor structures were presented with a central gate design [35, 36] (see Figure 2.7). Hereby, on the one hand indirect, cooled metal evaporation was utilized to non-destructively form contacts on the organic layer [35, 37], and on the other hand gold nanoparticles were first applied before metal evaporation [36]. In the case of the gold nanoparticles a special gate effect meaning that a transition from symmetric to rectifying current-voltage characteristics was observed at low gate voltages (few tenths of volts). This was attributed to charging of the gold particles affecting the spatial profile of the voltage over the junction [36].

Figure 2.7. Schematics of central-gate vertical transistors based on self-assembled monolayers with (a) Pd top contacts deposited by indirect, cooled evaporation and (b) with Au nanoparticles between the monolayer and the top contact [35, 36].

As already mentioned above, organic semiconductors and self-assembled monolayers of organic molecules are very sensitive to solvents used during standard lithography. This is more a problem for VOFETs than for planar OFETs since the OS and/or the top-contacts still have to be patterned. Special fluorinated photoresists allow direct patterning of organic materials in the micrometer range, because the resist as well as the chemicals used for development and lift-off procedures are compatible with the used organic materials (pentacene and C_{60}) [19].

The various different fabrication methods and device structures influence the electrical performance of (vertical) OFETs. In order to get a clear understanding of the physical mechanisms taking place in organic semiconductors, the electrical characteristics have to be compared. Important parameters are the charge transport mechanism, the current density and the mobility of the charge carriers. In the last section of this chapter, the main charge transport mechanisms are discussed.

2.3 Organic semiconductors

A material which is insulating at low temperature close to zero Kelvin, but which shows considerable conductivity at higher temperature is generally defined as a semiconductor. In Figure 2.8, the energy level diagrams of a metal, insulator and semiconductors are illustrated.

Figure 2.8. Energy diagram for metals, insulators and extrinsic *n*- and *p*-type semiconducting materials [3].

In metals the conduction band is partially-filled, in insulators the conduction band is empty while the valence band is filled. For insulators and (intrinsic) semiconductors the valence and conduction bands are separated by a band gap. However, at elevated temperatures electrons can be thermally activated. The conductivity of inorganic semiconductors can be controlled by doping of the material with dopant atoms, which means that an impurity band is created either close to the conduction (*n*-type) or close to the valence (*p*-type) band [3].

Organic semiconductors can be classified into two classes: small molecules and polymers. Small molecules are mainly evaporated by vapor deposition in vacuum, however several small molecules like for example 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) can be processed from solution [38, 39]. Polymers are generally deposited from solution due to their good solubility in organic solvents. The electrical performance of small molecules is in most cases higher than that of polymers due to a better ordering. For both categories, a large variety of electron- and hole-transport materials exists.

The metal-organic semiconductor interface is of crucial importance for the device performance of OFETs. In order to have ohmic contacts, which means that the current is not contact-limited, the work function of the metal has to be aligned with the HOMO or LUMO level of the organic material. If the Fermi levels (E_F) of the two materials are different, they form a thermal equilibrium, thus a shared Fermi level, by charge carrier exchange. At the interface, a contact potential arises, and charges that were moved into the organic semiconductor are either stored as a space charge, a surface sheet charge or as a combination of the two phenomena [40].

Organic semiconductors consist of hydrocarbons and have a carbon atom backbone [41]. Chemical doping of organic semiconductors is not straightforward. Whether an OS behaves *n*- or *p*-type depends on the applied gate voltage and the workfunctions of the contacts relative to the highest occupied molecular orbital (HOMO)/ lowest unoccupied molecular orbital (LUMO) levels of the OS.

π -conjugated molecules with high HOMO levels and electron-donation properties are utilized as *p*-type semiconductors. Conjugation denotes alternating single and double bonds in the carbon backbone which stabilize the molecules [3]. Most organic semiconductors have LUMO levels between -2 and -4 eV and HOMO levels between -5 and -6 eV, leading to energy bandgaps of $E_G > 2$ eV [40]. When electrode metals like gold or palladium with work functions around 5 eV are utilized, the mismatch between the HOMO level of the organic compound and the metal is small and the charge transport is not injection limited. In present organic electronic devices hole-transporting organic semiconductors are favored over electron-transporting materials since they exhibit higher charge carrier mobilities and better environmental stability in most cases [42]. The reason therefore is the position of the LUMO level (-3.0 eV to -4.0 eV) of *n*-type OS and their instability in air and water environment [42, 43]. This instability arises from a redox reaction with wet oxygen under ambient conditions [44]. The workfunction of frequently used metals like Au lies around -5.1 eV. This introduces a high injection barrier which can decrease the charge mobility [42]. It is very unlikely to observe *n*-type behavior due to the difficulty of injecting electrons into the LUMO level [45]. An overview of *n*-type small molecule and polymer organic semiconductors used for OFETs can be found in References [42, 46]. From this overview it can be seen that gold with a

work function of about 5.1 eV is mainly used for source and drain contacts. An advantage of gold is its chemical inertness and often its surface is modified with SAMs before coating of the OS to lower the charge injection barrier from the metal to the OS [47]. Some devices were formed with metals that have a lower work function (e.g. aluminum, calcium or magnesium), enabling better electron injection, but these materials are less stable in ambient conditions than noble metals like gold and therefore less suitable. *n*-type organic semiconductors which are recently used in many devices are fullerene-based compounds like C₆₀ molecules, aromatic diimides like naphthalene and perylene tetracarboxylic diimides and organic semiconductors modified with cyano and/or carbonyl groups like molecules based on 7,7,8,8-tetracyanoquinodimethane (TCNQ) [21, 42, 48, 49]. Cyano and carbonyl groups are electron-withdrawing groups known to lower the LUMO level of the organic molecule to which they are attached. For application in electronic devices, it is important to increase the air-stability of *n*-type organic materials to reach the same stability as their *p*-type counterparts. Several very promising air-stable, solution-processable *n*-type organic semiconductors already exist [5, 50, 51].

Often used *p*-type organic semiconductors are acenes like pentacene [52], and heterocyclic oligomers like oligothiophenes [53]. Thermally evaporated pentacene exhibits one of the largest hole mobilities with 1.5 cm²/Vs deposited on octadecyltrichlorosilane (OTS) treated SiO₂ dielectric substrates with Au source and drain contacts [54]. Higher mobilities can be achieved with organic single-crystals showing values up to 35 cm²/Vs for pentacene [55] and 40 cm²/Vs for rubrene [56]. However, pentacene is insoluble in most standard solvents and therefore not very applicable for the implementation in flexible and/or low-cost organic electronics. Pentacene has been chemically modified to TIPS-pentacene to become soluble in solvents offering the possibility for spin-coating and exhibits mobilities of 1.2 cm²/Vs [38, 39]. Another widely studied *p*-type material is poly(3-hexylthiophene) (P3HT) due to its combined solution-processability and relatively high mobility > 0.1 cm²/Vs [57-59]. The high mobility arises from semicrystalline domain areas of self-organized polymer chains. The intermolecular $\pi - \pi$ stacking of polythiophene is responsible for the charge transport, the alkyl chains arrange in orthogonal

lamellae and are nonconductive. P3HT molecules can align in three manners: edge-on, face-on and vertical as depicted in Figure 2.9.

Figure 2.9. (a) Different orientations of P3HT molecules: edge-on, face-on and vertical. The lattice constants are a) the distance between the backbones of 1.7 nm, b) the stacking distance of 0.4 nm, and c) the distance between the side chains 0.4 nm [60]. (b) Edge-on and face-on orientations showing the lamellar directions $\langle 100 \rangle$ (charge transport is prevented due to the insulating alkyl chains) and $\langle 010 \rangle$ (charge transport takes place because of the interchain $\pi - \pi$ interaction of the polythiophene [20]).

The P3HT molecule orientation is very important for achieving high-mobility charge carrier transport. In the $\langle 100 \rangle$ direction (face-on) charge transport is constrained due to the insulating alkyl chains. The high mobilities were only observed with edge-on chain orientation [3]. Vertical orientations can be achieved via vertical confinement of P3HT, also here high mobilities were observed since charge transport takes place because of the $\pi - \pi$ overlap [60, 61]. The HOMO level of P3HT is about -5.2 eV [62, 63]. In Figure 2.10 the band diagram of P3HT sandwiched between two Au contacts is given, the only slight mismatch between energies gives rise to hole injection from Au into P3HT and electrons are going from the HOMO into the Au electrode without an injection barrier.

Figure 2.10. Band diagram of P3HT with Au source and drain electrodes.

Table 2.1 gives a brief overview of electrode materials used for OFETs with P3HT as the active organic semiconductor, illustrating that Au is one of the most frequently used electrode materials in combination with P3HT.

Table 2.1. Summary of some recent p-type OFETs based on P3HT.

Electrode material	OFET design	P3HT thickness [nm]	reference
Au/Pd – Au/Pd	vertical	370	[20]
Graphene - Au	vertical	100 – 200	[64]
Al – Au	vertical	300	[65]
Au – Au	planar	20 – 30	[66]
Au – Au	planar	2, 8, 15	[67]
Pt – Pt	planar	not mentioned	[68]

2.4 Charge transport mechanisms

The two most relevant charge transport mechanisms in organic materials are nonresonant tunneling and thermally assisted hopping, which are coherent and incoherent electron transfer, respectively. Tunneling transport only occurs in tunnel junctions.

2.4.1 Nonresonant tunneling

Nonresonant tunneling is generally accepted as the transport mechanism in molecular tunnel junctions of SAMs of alkanethiols [69]. This type of SAMs is investigated in Chapter 4. Alkanethiols are suitable test molecules for understanding the principles of molecular tunnel junctions, since their length can easily be varied by changing the number of carbon atoms in the alkane chain. Alkanethiols have a large energy gap between the HOMO and LUMO level of between 7 and 10 eV [70-72]. This large energy gap gives alkanethiols the characteristics of an insulator. Sandwiched between two metal electrodes, a molecular tunnel junction is formed (see Figure 2.11).

Figure 2.11. Schematic image of a molecular junction of alkanethiols sandwiched between two metal electrodes (dark yellow: -SH head group, green: h atoms, grey: carbon atoms).

Tunneling is temperature independent and shows an exponential decrease of the current density with increasing molecular chain length given by

$$J = J_0 e^{-\beta d}, \quad (2.3)$$

with β (n_c^{-1}) as the decay coefficient, d (n_c) the thickness of the SAM and J_0 as a constant (J at $d=0$), which is dependent on the system and includes the contact resistance [28, 69, 73]. The number of carbons (n_c) corresponds to the length of the organic layer. The thickness depends on the length of the molecule and on the angle with the substrate which varies with different substrate materials [74].

2.4.2 Thermally assisted hopping

The semiconducting characteristics of π -conjugated polymers like P3HT, which are discussed in Chapters 5 and 6, are a consequence of covalent interactions between the monomer of the backbone [66]. In the ideal case, the polymer chains would offer a conjugated path for the charge carriers but due to disorder, which is always present in organic films, and polarization of the neighboring medium, the π -conjugation is discontinuous and thus spatially and energetically distributed electronic sites are formed. In order to explain transport mechanisms in organic semiconductors, the transition rate between these localized states needs to be known. Thermally assisted hopping transport is strongly dependent on temperature since charge carriers need thermal energy in order to tunnel from one localized electronic state to another.

There are two main generally accepted models which describe the hopping transport mechanism. The first model was developed by Miller and Abrahams (M-A) [75]:

$$v_{ij} = v_0 e^{-\frac{2r_{ij}}{a}} \begin{cases} \exp\left(-\frac{\varepsilon_j - \varepsilon_i}{k_B T}\right) & \varepsilon_j > \varepsilon_i \\ 1 & \varepsilon_j \leq \varepsilon_i \end{cases} \quad (2.4)$$

with ν_0 being the attempt hopping frequency, r_{ij} the distance between sites i and j , a the average localization radius and e_i and e_j the respective localized energy levels of the sites [72, 76]. The Miller-Abrahams model holds for devices in which charge transport arises in the presence of energetic disorder. This is the case for most organic semiconductors, the higher the extent of disorder the more localized states are present. For strong disorder, the charge carriers have to hop between the localized states [72].

The second hopping transport model is the Marcus expression:

$$k_{ij} = \frac{J_{ij}^2}{\hbar} \left[\frac{\pi}{E_a k_B T} \right]^{1/2} \exp \left[-\frac{(\epsilon_j - \epsilon_i + E_a)^2}{4E_a k_B T} \right], \quad (2.5)$$

where $\hbar$ represents the Planck constant divided by 2π , $J_{ij} \propto \exp(-2\alpha R_{ij})$ is the transfer integral (R_{ij} is the hopping distance between the sites i and j , and α is the inverse localized range), which means an overlap of the wave function between the two sites, E_a is the polaron activation energy [77]. The Marcus expression takes strong charge-phonon coupling inside the disordered organic semiconductors into account, which means that reorganization energies as well as electronic coupling between molecules strongly influence the electron transfer rate [48].

2.4.3 Space-charge limited current

In the case that an external potential is absent, charge transport through the organic material only takes place by diffusion and is usually defined by a diffusion equation [72]:

$$\langle x^2 \rangle = nDt, \quad (2.6)$$

with $\langle x^2 \rangle$ defining the mean-square displacement of the charges, D being the diffusion coefficient, t the time and n an integer number equal to 2, 4, 6 for 1D, 2D and 3D systems, respectively. The Einstein-Smoluchowski equation explains the relation between the charge mobility and the diffusion coefficient [72]:

$$\mu = \frac{eD}{k_B T}, \quad (2.7)$$

with k_B denoting the Boltzmann constant and e the electron charge. Diffusion describes the local displacement of charge carriers around their average location. An applied external electric field generates a drift of the charge carriers:

$$\mu = \frac{v}{F}, \quad (2.8)$$

where v denotes the charge velocity and F the applied electric field. A drift is different from diffusion because it generates a displacement of the average location.

For organic semiconductors that are sandwiched between source and drain electrodes without an applied gate (like in diode devices) the mobility can be extracted from the current density-voltage (J - V) characteristics in the space-charge limited current (SCLC) regime given by the well-known Mott-Gurney equation [78]:

$$J_{SCLC} = \frac{9}{8} \varepsilon_0 \varepsilon_r \mu \frac{V^2}{L^3}, \quad (2.9)$$

where ε_0 is the vacuum permittivity, ε_r the dielectric constant of the organic thin film, V the applied voltage and L the channel length. J scales quadratically with the applied voltage. The SCLC behavior accounts for trap-free devices that are bulk resistance limited and not limited by the contact resistance. In the presence of traps the behavior is much more complex. The current is first characterized by a linear regime due to injection-limited transport at low bias voltage, and subsequently increases and when the trap-free regime is reached, the current also scales quadratically with the bias voltage [72]. For devices with traps, a trapping factor θ is incorporated into the formula which considers the bulk traps [79]:

$$J_{SCLC} = \frac{9}{8} \theta \varepsilon_0 \varepsilon_r \mu \frac{V^2}{L^3}, \quad (2.10)$$

In the SCLC regime, the maximum density of injected charge carriers (electrons or holes) is reached and a space-charge builds up in the organic material inhibiting further injection of electrons or holes from the metal electrode.

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Chapter 3

Experimental methods

All devices described in this thesis were fabricated in the cleanroom facilities of the MESA+ Institute for Nanotechnology at the University of Twente, Enschede.

The first part of this chapter focusses on the device fabrication of molecular junctions as well as vertical pillar structures with and without side-gates (Chapter 4 - 6). The fabrication of nanogaps and silicon nanocrystals are not described in this chapter but are treated in detail in Chapter 7 and 8, respectively.

In the second part, the used characterization techniques are explained followed by the last part that presents the measurement setups that were employed to investigate the devices.

3.1 Device structures

In Chapter 4, the fabrication and electrical characterization of cross-bar metal-molecular monolayer- metal junctions are described. Self-assembled monolayers were formed on ultrasmooth template-stripped bottom electrodes. Metal top contacts were gently applied with a water-based technique called wedging transfer.

The main part of the thesis focuses on the fabrication and characterization of vertical organic/inorganic pillar structures without and with a side gate (fabrication details are discussed in Chapters 5 and 6, respectively).

3.1.1 Large-area metal- molecular monolayer- metal cross-bar junctions

Bottom electrodes were formed by template-stripping of Au contacts [1]. The Au contacts were patterned by photolithography on a silicon <100> wafer with native SiO₂. Before metal evaporation the substrates were cleaned for 30 min with UV/ozone to ensure clean surfaces. 100 nm Au was evaporated without an adhesion layer. After lift-off in a resist stripper (Baker PRS 2000) an anti-sticking layer was deposited from the gas phase. Subsequently, a piranha-cleaned glass slide was glued onto the electrodes by means of an optical adhesive (OA). The anti-sticking layer ensures low adhesion of the OA to the SiO₂. The glass-slide including the metal electrodes can be stripped off the wafer by placing a razor under a corner of the glass-slide which is thereby separated from the substrate. As a result ultrasmooth Au electrodes embedded in the OA are achieved on which the self-assembled monolayers (SAMs) of alkanethiols were formed. The procedure for template-stripping is illustrated in Figure 3.1.

Figure 3.1. Schematic of the process steps for template-stripping of metal electrodes. (a) Au electrodes were patterned on a UV/ozone cleaned Si <100> substrate with native SiO₂; (b) a piranha-cleaned glass slides was glued to the metal structures by means of an optical adhesive (OA), the OA was cured under UV light for 2 hours; (c) the glass/OA/electrode devices were separated from the Si/SiO₂ substrate with a razor; (d) the devices were flipped and ultrasmooth metal electrodes were exposed.

Soft top-contacting of the SAMs was done by wedging transfer of Au electrodes in a cross-bar structure (see Figure 3.2). Therefore, the top electrodes were patterned in the same way like the bottom electrodes by photolithography and lift-off. In the next step, the electrodes were dip-coated in a hydrophobic polymer (cellulose acetate butyrate (CAB) in ethyl acetate, 30 mg/ml).

Figure 3.2. Scheme for the fabrication of metal-molecular monolayer-metal junctions with the wedging transfer method. (a) top electrodes were embedded in CAB and lifted off in water; (b) after aligning the top electrodes with respect to the bottom electrodes covered with SAMs, molecular junctions were formed by lowering the water level; (c) finished device.

When this device was dipped into water, the water penetrates in between the hydrophobic CAB and the hydrophilic SiO₂ substrate and thereby lifts off the transfer polymer including the Au electrodes due to the low adhesion of Au to SiO₂. The template-stripped bottom electrodes with the SAM were subsequently also placed in the beaker with water and the top electrodes were aligned with respect to the bottom electrodes with a micro-manipulator. The beaker was connected to a syringe pump with which the water was slowly pumped out. This allows a very soft transfer of the top electrodes onto the SAM.

3.1.2 Vertical pillar structures without gate

p-type Si <100> wafers were cleaned in UV/ozone steam (ultraclean line) followed by thermal dry oxidation of 200 - 350 nm SiO₂. The wafers were diced into smaller pieces of 11×11 mm² before further processing. Bottom electrodes of Ti/Au were defined by photolithography with a lift-off procedure. The organic semiconductor was spin-coated from solution onto the bottom electrodes. In the next step, electron-beam lithography (EBL) patterned Au or Pd circular top contacts were applied by wedging transfer onto the organic thin film and subsequently used as a mask for dry etching to structure the organic layer [2, 3]. Since the dots have diameters of $\leq 2 \mu\text{m}$, it is not possible to directly electrically contact them by wire bonding and furthermore this would damage the organic layer. Therefore the pillars were embedded in hydrogen silsesquioxane (HSQ), which is applied by spin-coating and turns into SiO₂ at elevated temperatures (120°C was used for curing of HSQ). In addition to the dielectric properties (dielectric constant <3) [4, 5], HSQ has another advantage. HSQ is applied by spin-coating and in that way planarizes which means that the film is thinner on top of the pillars than on the substrate [6]. The HSQ could thus be etched back until the top of the dots is opened up, while the bottom electrodes and the organic layer are still protected by HSQ. In the last step, a 100 nm thick Au layer with 2 nm Ti for adhesion was evaporated and large contact pads (150×150 μm^2) were defined by photolithography and reactive ion beam etching (RIE). RIE was utilized instead of metal lift-off because the HSQ was etched by the photoresist developer (Olin OPD 4262, contains tetramethylammonium hydroxide (TMAH)) with an etch rate of $\sim 170 \text{ nm/min}$ obtained by ellipsometry.

Table 3.1. Basic process flow for the fabrication of vertical pillar structures without gate electrodes.

(a) Bottom electrodes fabricated by photolithography on SiO ₂ substrates	(b) Spin-coating of the organic semiconductor (OS), wedging transfer of EBL patterned top contacts followed by dry etching of the OS	(c) Spin-coating of HSQ to embed the pillar structures and back-etching until the top contacts are open, deposition of large contact pads patterned by photolithography
<div style="display: flex; justify-content: center; align-items: center; gap: 10px;"> <div style="display: flex; align-items: center;"> Si SiO₂ Au P3HT HSQ </div> </div>		

3.1.3 Vertical pillar structures with gate

For devices including a side gate, the first steps are the same as described in Section 3.1.2. The Au was hereby replaced by Pd due to compatibility problems of Au with the atomic layer deposition (ALD) equipment used in the following step. ALD was utilized for the formation of the gate oxide because it forms very conformal layers around the pillar structures. Furthermore, ALD-Al₂O₃ is characterized by good insulating properties [7]. For the gate electrodes Al was evaporated and subsequently patterned by photolithography. The photoresist developer contains TMAH and this was utilized to simultaneously develop the photoresist and directly transfer the pattern into the Al. The photoresist was afterwards removed in acetone and isopropanol. The oxide as well as the gate metal were also deposited on top of the pillar, which introduces an undesired insulating layer. Therefore, the structures were embedded in HSQ and like for the devices without a gate, etched back till the pillars were opened up, while the gate was protected by HSQ. Then RIBE, connected to a secondary ion mass spectrometer (SIMS), was utilized to

mechanically etch the Al and Al_2O_3 on top of Pd. The HSQ was thereby also partly etched. HSQ was therefore spin-coated again and etched back till the Pd of the top contact was opened up again. In the last step, Pd was deposited with a Ti adhesion layer and patterned by photolithography and RIBE.

Table 3.2. Basic process flow for the fabrication of vertical pillar structures with gate electrodes.

(a) Bottom electrodes fabricated by photolithography on SiO_2 substrates	(b) Spin-coating of the, wedging transfer of EBL patterned top contacts followed by dry etching of the OS	(c) Conformal growth of Al_2O_3 by ALD as gate oxide

(d) Deposition of Al gate electrodes patterned by photolithography	(e) The structures are embedded in HSQ and etched back by RIBE to remove the Al and the oxide on top of the pillar	(f) The structures are embedded a second time in HSQ and etched back until the top contacts are open, deposition of large contact pads patterned by photolithography
Si SiO_2 Pd P3HT HSQ Al_2O_3 Al		

3.2 Preparation of self-assembled monolayers and organic semiconductor thin films

In this thesis, self-assembled monolayers (SAMs) of alkanethiols and thin films of the organic semiconductor poly(3-hexylthiophene) (P3HT) have been investigated in different device structures.

The formation of SAMs on template-stripped Au electrodes [1] was done from solution. The electrodes were immersed overnight for approximately 18 hours in 5 mM ethanolic solutions of dedecanethiols (C12), tetradecanethiols (C14) and hexadecanethiols (C16) for SAM formation followed by gently rinsing with ethanol and drying with N₂. The quality of the SAMs was characterized by contact angle measurements. A high-quality SAM of alkanethiols with a chain length of > 10 carbon atoms is known to have contact angles between 110° and 114° [3].

For the formation of thin films of P3HT, the material was dissolved at concentrations ranging from 2 mg/ml to 20 mg/ml in high-boiling-point solvents like dichlorobenzene or bromobenzene at 80 °C under stirring for 3 hours and then cooled down to room temperature under stirring. Subsequently, the solutions were filtered with a 0.2 µm-syringe filter and then kept in dark. The solution was spin-coated at ambient conditions for 45 sec at a spinning speed between 500 and 6000 RPM, and subsequently annealed on a hotplate at 100°C for 1 hour to completely evaporate the remaining solvent. The thickness was controlled by the concentration and the spin-speed, and measured by atomic force microscopy (AFM).

Table 3.3. AFM analysis of the P3HT thickness and root mean square (RMS) roughness for different spin-coating speeds. Thickness and root mean square (RMS) roughness of P3HT (9.8 mg/ml in bromobenzene) for different spin-coating speeds analysed by AFM.

Spin-speed [RPM]	Thickness [nm]	Roughness [nm]	AFM image
500	67	1.43
1000	44	0.8
2000	34	0.35
3000	19.5	0.165
4000	10.15	0.142

3.3 Photo- and electron-beam lithography

The metal electrodes for pillar structures with and without gate electrodes were patterned by photolithography and EBL. The lithography steps for molecular junctions by wedging transfer as well as for nanogaps and silicon nanocrystals are explained in detail in Chapter 4, 7 and 8, respectively. Photolithography was performed with a UV mask aligner EVG 620 with an intensity of 12 mW/cm². Positive and image reversal photoresists were utilized depending on the process. For lift-off procedures the image-reversal resist TI35 ES (MicroChemicals GmbH) was used, because it forms an undercut. Positive resist Olin 17 (Olin OIR-907-17, Arch Chemicals, Inc.) which forms straight side walls, was used for etching

procedures. Ti35 ES was used as follows: hexamethyldisilazane (HMDS) was spin-coated at 4000 RPM to increase the adhesion of the photoresist to the substrate, then Ti35 ES was spin-coated at 4000 RPM followed by a pre-exposure bake for 120 sec at 95°C, the resist was exposed for 20 sec to UV light with a standard photomask. During exposure nitrogen is generated in the photoresist. After > 30 min of waiting time to let the nitrogen diffuse out of the resist a reversal bake at 120°C for 120 sec was performed, subsequently a 60 sec flood exposure was done and in the last step the resist was developed in Olin OPD 4262 (containing tetramethylammonium hydroxide (TMAH) for 40 sec, rinsed with DI water and blown dry with nitrogen. The Olin 17 resist was spin-coated at 4000 RPM on HMDS-treated surfaces followed by a pre-exposure bake for 120 sec at 95°C, exposure was done for 4 sec with a standard photomask and the post bake was done at 120°C for 120 sec. Developing was done for 60 sec in Olin OPD 4262 followed by rinsing with DI water and blow dry with nitrogen. The devices were cleaned with UV/ozone before metal evaporation to remove resist residuals.

The top contacts (dots with diameters between 2 μm and 200 nm) that were applied by wedging transfer onto the organic thin films of P3HT were written by EBL. Poly(methyl methacrylate) (PMMA A4, in anisole, MicroChem) was spin-coated at 2000 RPM and baked for 3 minutes at 160°C for lift-off of ≤ 100 nm thick metal structures. For thicker metal structures up to 150 nm a bi-layer process was used. Here, a stack of copolymer (EL9) and PMMA A4 was used, both spin-coated at 2000 RPM and baked for 3 minutes at 160°C, respectively. The advantage of bi-layer structures is that the copolymer develops faster than the PMMA creating an undercut, which provides better lift-off results.

The Raith 150TWO (Raith GmbH) was used for EBL patterning. Structures were written with an acceleration voltage of 20 kV, an aperture of 60 μm , a working distance of 10 mm and a dose of $\sim 300 \mu\text{C}/\text{cm}^2$ for the VOFET top contacts. The electron beam current was 1.4 nA $\pm$ 0.1. The step size was ~ 30 nm and the writing field was $100 \times 100 \mu\text{m}^2$.

The structures were developed in a mixture of methyl isobutyl ketone : isopropanol MIBK:IPA (1:3) for 30 sec followed by rinsing with IPA and blown dry with nitrogen. In order to remove resist residues in the developed areas, the devices were cleaned by UV/ozone for 5 minutes prior to metal evaporation. This step is very important because only if the surfaces are clean, metal structures can be transferred from the Si substrate by wedging transfer.

3.4 E-beam evaporation of metals

Metal electrodes were deposited by e-beam evaporation (BAK 600, Balzers) with a 10 kV voltage source at a rate between 0.01 and 0.2 nm/s and a pressure below $1 \cdot 10^{-6}$ mbar. Here, the electron beam is focused on the material to be evaporated. The energy of the beam is transferred into the material, which consequently heats up, until at a certain temperature it starts to evaporate.

Figure 3.3. Photograph of the e-beam evaporation system BAK 600 (Balzers) in the cleanroom of the MESA+ Institute.

Au (for two-terminal devices) and Pd (for gated devices) were deposited as source and drain contacts, and Al (30 nm) was used as gate electrode. 2 nm Ti and 20 nm Au were used as bottom contacts, 70 nm Au for EBL patterned dots and 2 nm Ti and 100 nm Au for large top contact pads were used for vertical pillars without gate electrodes. For gated devices, the Au was replaced by Pd due to compatibility with the atomic layer deposition equipment. Ti served as an adhesion layer.

The top contacts were evaporated without an adhesion layer, because here a low adhesion is required for wedging transfer. The wedging transfer technique is a soft-landing method to gently contact organic thin films [1, 2], and is discussed in detail in Chapter 4. The basic principle of this method is that metal structures are formed on hydrophilic silicon with hydrophilic native SiO_2 substrates to which they have a low adhesion. In the following step the structures are embedded in a hydrophobic polymer. When the device was dipped into water the hydrophobic polymer including the metal structures was lifted off and was floating on the water interface. In this way, the metal structures can be transferred to a new substrate which is in our case the bottom electrodes covered with SAMs or a thin film of

organic semiconductor. For the VOFETs covered in Chapter 6, relatively thick top contacts (≥ 150 nm) are required. Without an adhesion layer, stress occurred in the metal with as a consequence bending of the structures as depicted in Figure 3.4. Au dots and lines used for wedging transfer had thicknesses between 70 nm and 100 nm, the built-up of stress during evaporation was not observed there.

Figure 3.4. Scanning electron microscopy (SEM) image of a Pd line e-beam evaporated on a Si/SiO₂ substrate without an adhesion layer.

In order to reduce stress during evaporation, we used water cooling with a special sample holder. In Figure 3.5, scanning electron microscopy (SEM) images of Pd dots with different diameters are shown that were evaporated with water cooling. It can be seen that for the largest diameters (2 μ m) the tension inside the metal is still stronger than the adhesion to the substrate and the edges are bent up. For smaller diameters the stress is less, especially for diameters in the sub- μ m regime.

Figure 3.5. SEM images of Pd dots on a Si substrate without an adhesion layer evaporated with water cooling. Images were taken at a cross section and the focus is at (a) 2 μm diameter dot, (b) 1 μm diameter dot, (c) 500 nm diameter dot and (d) a zoom-in of the 500 nm diameter dot.

3.5 Atomic layer deposition (ALD)

The Al_2O_3 gate dielectric was grown in a load-lock equipped atomic layer deposition (ALD) reactor (Picosun). The thermal ALD process was performed at 100°C with two precursor materials: trimethylaluminum $\text{Al}(\text{CH}_3)_3$ (TMA) and water. The precursors are alternating pulsed in the reactor starting with TMA. The reactor is purged after every cycle with N_2 . The chemical reactions are as follows [8]:

The asterisks hereby represent surface species. Both reactions are self-limiting and allow monolayer by monolayer growth of aluminium oxide. The

thickness is controlled by the number of steps, and is highly accurate. The Al_2O_3 thickness was checked with high-resolution SEM as well as ellipsometry. The breakdown voltage of a 20 nm thick layer was ~ 15 V, which was measured on a device with Pd bottom contacts and Al top contacts with a junction area of $5 \times 5 \mu\text{m}^2$. A value of ~ 15 V is comparable with breakdown voltages of ALD- Al_2O_3 reported in literature [7]. In most cases higher process temperatures ($\sim 300^\circ\text{C}$) are used during Al_2O_3 growth, since our Al_2O_3 was grown at 100°C in order to avoid damage of the organic semiconductor, a lower breakdown voltage was expected compared to layers grown at higher temperatures.

Figure 3.6. SEM image of a cross section of a Pd-P3HT-Pd structure covered with ALD- Al_2O_3 and Al deposited as a side gate (yellow: Au; red: P3HT; light blue: Al_2O_3 ; green: Al).

On the SEM image in Figure 3.6 it can be seen that the ALD- Al_2O_3 forms a very conformal layer around the Pd-P3HT-Pd pillar since it grows on the metal electrodes as well as on the organic semiconductor. The small overhang of the top contact creates a shadow effect during evaporation of the Al gate material. This is very beneficial because shorts between the top contact and the gate electrode are minimized when the gate electrode is slightly spatially separated from the pillar.

3.6 Dry and wet etching

In the fabrication process of vertical (gated) pillar structures, dry as well as wet etching was used.

The organic semiconductor thin film was etched with reactive ion etching (RIE) with oxygen plasma (20 sccm, 100 mTorr, 10°C , 10 Watt, 30 – 60 sec depending on the thickness of P3HT) in a parallel plate RIE system (TETSKE). The wedge-transferred metal dots served as an etch mask (see Figure 3.7).

Figure 3.7. SEM image of a cross section of a Pt-P3HT-Au structure after directional RIE.

The HSQ (DC XR 1541-006 from Dow Corning) was spin-coated at 1000 RPM and baked for 2 min at 120°C, resulting in thicknesses around 160 nm. It planarizes during spin-coating, which means that the film is thinner on top of the pillar structures than next to them [6]. The HSQ layer was etched back with RIE (CHF₃, He, O₂ plasma at -10°C and a pressure of 8×10^{-3} mbar in a RIE system with an inductively coupled plasma (ICP) (Adixen AMS100DE). These kind of systems have a higher plasma density compared to parallel plate systems. An RF current is sent through a coil which generates an oscillating magnetic field which on its turn produces an electric field. The path of the electrons inside the plasma is changed by the induced magnetic field whereby the enhancement of the plasma density is achieved [7].

The large top contact pads were patterned by photolithography and mechanically etched with noble gas Ar ions by RIBE (Oxford i300). The etching is highly directional and purely mechanical. The ion beam is accelerated in a strong vertical electric field and the vacuum inside the process chamber is so high ($\sim 2.5 \times 10^{-4}$ mbar) that collisions between atoms is very rare. This causes the directionality during etching because the ions reach the sample surface almost vertically. The system is connected to a SIMS detector, when the ion beam hits the sample surface, the crystal lattice is destroyed and the sample material is emitted. Some part of this material is ionized (secondary ions), it can be collected and accelerated to the detector [7]. Etching was stopped after the Pd/Au and Ti signal peaks disappeared.

For patterning of the Al gate electrodes wet etching was performed. Here, the etching properties of Al and Al₂O₃ in the developer Olin OPD 4262 were utilized. The positive photoresist was developed and subsequently, the samples were kept in the developer until the unprotected Al areas were etched away which could be seen by eye. The remaining photoresist pattern was stripped in acetone and IPA.

For removal of the Al and Al₂O₃ on top of the pillar, RIBE was utilized. The samples had sizes of 11×11 mm², and the areas that had to be etched were relatively small (2 μm to 200 nm in diameter). The SIMS signal is not strong enough to detect the Al. Therefore, a second sample with the same Al/Al₂O₃/Pd thicknesses as the vertical OFET samples but with an unpatterned layer was always introduced to the chamber during etching to enhance the signal.

3.7 Characterization techniques

For AFM a Veeco (Bruker) Dimension 3100 setup was used under ambient conditions. Images were recorded in tapping mode using a rectangular silicon cantilever (nanosensors PPP-NCHR) with a tip diameter of ~ 7 nm and a spring constant of 42 N/m. AFM was used to measure the roughness and thickness of the spin-coated organic semiconductors, to image the metal electrodes and to check if the HSQ was completely removed on top of the pillars. This could be observed by a change in the roughness, HSQ films were very smooth, while Au and Pd surfaces are characterized by grains. In order to examine if the side-gated pillar structures were conductive meaning that the Al₂O₃ layer was removed on top of the pillar, a conductive AFM probe was utilized. Images were taken in contact mode with a platinum silicide on n⁺-silicon probe (nanosensors, Pt-Si-CONT-20). Contact mode can be utilized without damage to the pillar structures due to the very soft tip which has a cantilever length of 450 ± 10 μm, a resonance frequency of 6 -21 kHz and a force constant of 0.02 – 0.77 N/m.

Cross sections of the devices were imaged with high-resolution (HR) SEM. FEI Sirion HR-SEM was used for pre-investigations and FEI Focused Ion Beam System (FIB) and Zeiss Merlin HR-SEM were utilized for high-resolution images.

Thicknesses of thermally grown SiO₂ and ALD-Al₂O₃ were measured with a Woollam M-2000UI ellipsometer.

3.8 Measurement setups

Electrical characterization of the devices was performed in a low-temperature probe-station (Janus ST-500) connected to a Keithley 2400 semiconductor characterization system in vacuum (<10⁻⁴ mbar) at room temperature controlled by LabVIEW. Temperature-dependent measurements were carried out in a liquid helium flow cryostat (Bruker Corporation) or with a He compressor (Oxford Instruments). For the helium flow cryostat, the sample chamber is first pumped to

vacuum and then filled with He gas. This procedure is repeated at least 5 times to ensure a good He atmosphere. The cryostat is then filled with flowing liquid He and the temperature is controlled via a heater. The lowest achievable temperature is 5 K. For the Oxford system, the He is compressed and then brought into the cryostat where it expands and thereby is cooling down the system. The lowest achievable temperature is 10 K. All measurements were done in two-terminal configuration. We observed an offset at zero voltage which was attributed to the measurement setup when performing measurements with equipment connected to Keithley multimeters. Therefore, for all consecutively measured devices we used a custom-built low-noise electronics (IVVI-DAC rack, Quantum Transport designed instrumentation, designed by Ing. Raymond Schouten from Delft University of Technology) [9]. The Delft electronics are isolated from the power net ground and are driven by batteries to eliminate interference sources and external noise. The applied voltages are controlled by digital-to-analog converters (DACs) which are connected to a PC by an optical fibre. The DAC transforms a digital signal from the PC into an analog signal (voltage). The sample is connected with one electrode to a voltage source module controlled by the DAC and with the other electrode to a current measure module. *I-V* measurements were performed with a transimpedance amplifier (also called current-to-voltage (I-V) converter), the basic principle of an I-V converter is shown in Figure 3.8.

Figure 3.8. Schematic of the measurement set-up.

An I-V converter converts the incoming current of the sample into a proportional voltage and is generally used to accurately measure in the low current regime. The converter is utilized to amplify the current signals. The module used for electrical measurements is designed to send very little energy through the sample. The input resistance is therefore not at the lowest possible value but fixed at a function of the V/A (R_f) setting according to

$$R_{in} = 2k\Omega + 10^{-3} * [V/A] \quad (3.3)$$

This function leads to the following values of the input resistance for R_f values between $1M\Omega$ and $1G\Omega$ (see Table 2).

Table 3.4. Calculated R_{in} values for different R_f for the Delft electronics.

R_f [Ω]	R_{in} [Ω]
1M	3k
10M	12k
100M	102k
1G	1M

A requirement for measurements is that the input resistance is much smaller than the resistance of the sample.

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Symmetric large-area metal-molecular monolayer-metal junctions by wedging transfer

In this Chapter, a method is described for fabricating and electrically characterizing large-area (100–400 μm^2) metal-molecular monolayer-metal junctions with a relatively high overall yield of $\approx 45\%$. The measurement geometry consists of ultrasmooth (template-stripped) patterned Au bottom electrodes, combined with ultra-smooth top Au electrodes deposited using wedging transfer. The fabrication method is applied to the electrical characterization of Au-alkanethiol self-assembled monolayer-Au junctions. An exponential decay of the current density is found for increasing the chain length of the alkanethiols, in agreement with earlier studies. The symmetric device geometry, and flexibility for contacting monolayers with various end groups are important advantages compared to existing techniques for electrically characterizing molecular monolayers.¹

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4.1 Introduction

Using molecular components is a promising development in modern electronics [1–3]. Studying and controlling charge transport through a single molecule or molecular monolayer are very difficult, however. Electrically contacting a molecular monolayer is easier than addressing a single molecule, and has resulted in reproducible data [4, 5]. A molecular layer embedded between two contacts typically forms a tunnel barrier between them, but also gives the possibility to add electronic functionality such as rectification or conduction switching. [6–8]. It is therefore useful to study these molecular layers in more detail first, before incorporating them in (single) molecular electronic devices [5, 9].

Although numerous techniques exist for electrically contacting molecular layers such as self-assembled monolayers (SAMs) [10], the biggest hurdle is being able to apply the top contact to create two-terminal devices in a manner that will reproducibly yield reliable junctions. Direct metal evaporation causes metal atoms to penetrate or damage the monolayer, resulting in a low yield [11]. Other methods trying to alleviate this problem, use an additional short-chain SAM [12], have a graphene [13], or reduced graphene oxide protective layer [14], have an intrinsic oxide layer [15] or introduce an extra conducting polymer layer between the monolayer and the metal top contact, which has a non-negligible resistance [4]. A low yield makes it unpractical to obtain statistically relevant numbers of measurements, while an additional layer makes it possible to generate monolayer based tunneling junctions with high yield. However, these protective layers also introduce ambiguities in the interpretation of the electron transport data. For example, when investigating rectification in molecular junctions [6, 16], extra care needs to be taken to prove that the rectification originates from the intrinsic molecular properties.

For fabricating metal-molecular monolayer-metal junctions without a protective layer between top contact and monolayer, but also without damaging the monolayer, several techniques exist. Most are limited by the need for strong adhesion of the top contact requiring the introduction of a chemisorbing functional group at the end of the molecular adsorbate, as is the case in micro/nanotransfer printing [17], break junctions [18], or flip-chip lamination [19]. Only a few

fabrication techniques work independently of the end group of the monolayer. Scanning tunneling microscopy (STM) [20], and conducting probe atomic force microscopy (CP-AFM) are such techniques [21]. With CP-AFM, for example, the influence of the metal work function on the tunneling current has been investigated, made possible by the independence of end group of the monolayer on the fabrication of the molecular junction [22]. A drawback, however, of these probe-based techniques is the time-consuming process of acquiring a statistically relevant number of measurements at many positions on several samples, the difficulty of exactly determining the contact area as well as that measurements with CP-AFM are influenced by the force applied, in ways that are difficult to quantify [23, 24]. More importantly, these methods are incompatible with device fabrication.

To our knowledge, only one technique allows the fabrication of large-area metal-molecule-metal junctions with a relatively high yield, without posing restrictions on the end group of the monolayer [25–27]. The latest iteration of this technique, permanent modified polymer-assisted lift-off (PeMoPALO) [27], introduced electrical contacting away from the molecular junction, removed the restriction on the junction area, and introduced the possibility to make permanent contacts via wire bonding. The system was used to study Si-alkyl-Au junctions (covalently attached monolayers of alkenes with a H-passivated Si surface). However, these alkyl layers are less thoroughly studied than SAMs of, for example, n -alkanethiols on Au, which are extensively studied [10, 28]. It is also difficult, synthetically, to vary the end group of these alkyl layers, and they are more difficult to analyze, in the sense that they incorporate not only a tunneling barrier but also a Schottky barrier [29]. A disadvantage inherent of the system is a reduced quality of the interface between the monolayer and top electrode, which affects the electrical measurements [30].

Here, we describe a soft lithography-based method to fabricate symmetric large-area metal-molecule-metal junctions with a relatively high yield for practically obtaining statistically relevant numbers of measurements, without an additional protection layer and without the need for a chemisorbing functional group in the monolayer. It consists of template stripping [31], to make patterned and ultra-smooth (< 0.5 nm RMS) metal bottom electrodes, which is important to reduce the

density of defects in the monolayer leading to shorts [10]. This is combined with a soft deposition method of ultra-smooth top electrodes embedded in cellulose acetate butyrate from water. This soft deposition method is adopted from the recently published “wedging transfer” method to deposit Au electrodes and graphene flakes [32]. The method is now – for the first time – applied to the fabrication of molecular Au-alkanethiol SAM-Au junctions, which is used here mainly as a reference system, and their electrical properties are compared to reported values of junctions fabricated by other methods with the main aim of showing the usability of this fabrication method. This is the first time that a floatation method is shown to work with metal/metal contacts, while previous reports only showed Si or oxidized Al as bottom contacts.

4.2 Results and Discussion

4.2.1 Fabrication of the Metal-Molecular Monolayer-Metal Junctions

Figure 1 schematically shows our method for fabricating metal-molecular monolayer-metal junctions. First (Figure 4.1 (a)), Au metal bottom and top electrodes were defined directly on a Si/SiO₂ wafer by photolithography and metal lift-off. No adhesion layer was used, because the electrodes had to be removed from the wafer later on by means of template stripping. After the application of an anti-sticking layer on the Si/SiO₂, the bottom electrodes were embedded in optical adhesive (OA) and template stripped (TS) from the wafer (Figure 1 (b)). TS consists of mechanically cleaving the Si/SiO₂–Au interface [31], exposing the ultra-smooth metal surface. Ultra-smooth surfaces are preferred, because they lower the density of defects in the monolayer [10], which results in fewer shorts, compared to electrodes used directly after electron-beam evaporation [33]. Atomic force microscopy (AFM) on the exposed Au electrodes embedded in OA, revealed an RMS roughness of 0.27 ± 0.04 nm (scan areas of $2 \mu\text{m} \times 2 \mu\text{m}$), which is in the expected range for TS metal surfaces [31, 34]. Embedding the metal electrodes in OA is necessary to prevent shorts at the edges of the electrodes where the monolayer is not densely packed [10, 35].

Figure 4.1. Scheme for the fabrication of metal-molecular monolayer-metal junctions with the wedging transfer method. (a) First, Au top and bottom electrodes were fabricated on a normal Si wafer with native SiO₂. Then, after the application of an anti-sticking layer on the Si/SiO₂, a cleaned glass slide was “glued” on the bottom electrodes by means of OA, and cured by UV illumination. (b) The glass slide was template stripped after curing, which caused the Au bottom electrodes to be transferred to the glass slide, with the ultra-smooth Au interface exposed, embedded in OA. (c) On the ultra-smooth bottom electrodes a SAM of n-alkanethiol was deposited from solution, after which (d) the top electrodes were embedded in cellulose acetate butyrate (CAB) and lifted off in water. (e) After aligning the top electrodes with respect to the bottom electrodes (probe needle), the molecular junctions were formed by lowering the water level (water drain). (f) With the device finished, the molecular junctions were electrically characterized with probes at the blue and black positions.

Figure 4.2 shows an AFM picture of an Au/OA interface after TS. It clearly shows that the Au electrode is not perfectly embedded in the OA. A trench exists next to the Au electrode, which has a width of a few 100 nm and a depth of 16 nm or more. Such a trench was reported before when TS electrodes were used [6]. This trench probably originates from shrinkage of the OA during polymerization (a linear shrinkage of 1.5% is reported by the manufacturer).

Figure 4.2. Tapping mode AFM height image of the Au/OA interface after TS showing the smoothness of the Au electrode and the trench next to it.

Next to a trench, on several occasions the Au electrodes were found protruding from the OA by 10–15 nm (Figure 4.3 (a, b)). This, together with the trench, is the most probable reason for the imperfect yield (see below). To solve the trench and protruding electrode problems, a procedure was tried in which the bottom electrodes were embedded in PMMA. This did decrease the trenches and protrusions considerably (see Figure 4.3 (c-f)) indicating that OA shrinkage was the problem. However, the PMMA itself gave other problems associated with swelling after overnight immersion in ethanol. This made it impossible to fabricate molecular junctions, and therefore bottom electrodes embedded directly in OA were used for further experiments.

Figure 4.3. Left side: Tapping mode AFM picture showing the height image of (a) the Au/OA interface after TS; (c) the PMMA/Au interface after TS when an anti-sticking layer was used, and (e) the PMMA/Au interface when no anti-sticking layer was used. Right side: Corresponding cross sections at the position shown in (a, c, e), showing the height difference between OA and Au (b) and accordingly between PMMA and Au with (d) and without (f) an anti-sticking layer.

On the bottom electrodes a SAM of *n*-alkanethiol was formed from solution (Figure 4.1 (c)). After this, the top electrodes were embedded in a hydrophobic

polymer layer of cellulose acetate butyrate by dip coating. This layer, including the metal top electrodes, was lifted off the wafer, by slowly dipping in Milli-Q water at an angle of 70° relative to the water surface (Figure 4.1 (d)). This resulted in a floating polymer layer, with the embedded electrodes facing downwards. By placing the bottom electrodes below the top electrodes at the bottom of the beaker, the top electrodes were gently applied on top of the SAM by lowering the water level with a syringe pump (Figure 4.1 (e)). This ensured gentle contact and prohibited shorts. Alignment was done by a probe needle, controlled with a micromanipulator that contacts the polymer layer. To ensure the removal of possible remaining water in the junction, the device was placed in a desiccator and pumped overnight. Thereafter, the molecular junctions could be electrically characterized with probes at the blue and black positions (Figure 4.1 (f)). Figure 3 shows the actual complete device.

The method for lifting-off Au electrodes without a detachment step was adopted from Dekker et al [32]. The technique is based on the hydrophobic effect, [36, 37] in this case easily explaining the lift-off by the fact that water wets hydrophilic surfaces and avoids hydrophobic ones [38–40]. We show here that it also works when depositing on top of a fragile SAM. The advantage over the PeMoPALO method is that the detachment step in HF (and the consecutive cleaning step) is obsolete. Furthermore, the lift-off and application of the top electrodes was done in water, ensuring a better quality interface [30].

Instead of applying the top electrodes embedded in cellulose acetate butyrate, while floating on the water-air interface, it was also tried to apply TS top electrodes, embedded in OA on a polydimethylsiloxane (PDMS) stamp, by hand. The procedure is shown and explained in Figure 4.4. The PDMS should provide conformal and soft contact. Although this approach worked, and gave the expected tunneling characteristics while electrically characterizing the resulting *n*-alkanethiol junctions, the overall yield after optimization was only 10%, compared to $\approx 45\%$ when applying the wedging transfer technique, while also having a spread in current densities of seven orders of magnitude. This rendered this approach unpractical and unreliable for electrically characterizing metal-molecular monolayer-metal junctions.

Figure 4.4. Scheme for the fabrication of metal-molecule-metal junctions with both electrodes TS. (a) First Au top and bottom electrodes were fabricated on a normal Si wafer with native SiO_2 . Then cleaned glass slides and flat PDMS stamps were “glued” on the bottom and top electrodes respectively by means of OA, and cured by UV. (b) The glass slide was template stripped after curing which causes the Au bottom electrodes to be transferred to the glass slide, with the ultrasmooth Au interface exposed, embedded in OA. (c) On the ultrasmooth bottom electrodes a SAM of *n*-alkanethiol was deposited from solution, after which (d) the PDMS stamp was template stripped, also exposing a ultrasmooth and clean interface. (d) Then the PDMS stamp is “flipped” and positioned perpendicular to the bottom electrodes and manually placed gently on top of the SAM. With the device finished, the molecular junctions were contacted at positions P1 and P2 and electrically characterized.

The design, shown in Figure 4.5, incorporates electrical contact points facing upwards and far away from the molecular junctions. This gives the possibility for integration in a sample holder. Also, remote contacting of the molecular junctions ensures that electrical measurements can be done without damaging the molecular junctions.

Figure 4.5. Photograph of the actual device, after wedging transfer, showing the molecular junctions (marked with a red box) and the electrical contacts far away from these junctions, facing upwards (probe 1 black box, probe 2 blue box).

Both in Figure 4.1 (c) and Figure 4.4 (c) the SAMs are only shown on the lower lines for simplicity. Practically, the whole device was immersed into the SAM solution for monolayer formation so that also SAMs form on the upper big line. However, since this line is 3600 times larger in area compared to the largest molecular junction, the contribution of the resistance is less than 0.3 % which is negligible and due to this large area it will most probably lead to electrical shorts.

4.2.2 Electrical Characterization of the Molecular Junctions

Molecular junctions with *n*-alkanethiol SAMs ($n_c = 12\text{--}16$) were electrically characterized by measuring the current density, J , as a function of the applied voltage, V . For every *n*-alkanethiol a minimum of 3 separate devices were fabricated and a minimum of 22 junctions ($\text{Au}/\text{SCn}_1\text{CH}_3/\text{Au}$) were measured. On each junction, 11 $J(V)$ traces (one trace = $0\text{ V} \rightarrow +1\text{ V} \rightarrow -1\text{ V} \rightarrow 0\text{ V}$) were recorded, from which the first one was discarded. For every *n*-alkanethiol 200–340 $J(V)$ data points were collected. All analysed junctions had an area size between 100 and 400 μm^2 , by changing the width of the top and/or bottom electrode by design.

Table 4.1 shows an overview of the total numbers of junctions measured, data points (N_j), working junction yield and other parameters, all specified per *n*-alkanethiol. A working junction is defined as a junction having a nonlinear $J\text{--}V$ slope with currents below 10^{-3} A at 1 V applied bias (which is more than one order of

magnitude higher than the highest current measured). Each junction must be measureable 11 times and these measurements should be “stable” in the sense that the current should not drift in consecutive measurements. A short is defined as a junction that has a linear ohmic J – V characteristic with a typical (contact) resistance of a few 100 Ω . An open circuit is defined as having a J – V characteristic that is independent of voltage and giving current values within the noise limit of the current meter (10^{-15} A). An unstable junction is defined as a junction not belonging to any of the other types of junctions (for example a nonsymmetric/offset junction around 0 V or a junction which displays continuously increasing current at consecutive measurements). The yield is then calculated by dividing the number of working junctions by the total number of junctions measured.

Table 4.1. Working device yields and other parameters for measurements of molecular junctions with SAMs of alkanethiols of different lengths ($n_c = 12$ –16) fabricated with the wedging transfer method. ^{a)} A short is defined in the text as a junction which has a linear, ohmic J – V curve (typical resistance of few 100 Ω); ^{b)} An open circuit is defined as a junction which exhibits current values in the noise level of the measurement setup (10^{-15} A); ^{c)} An unstable junction is defined as not belonging to the other three categories; d) The total number of values of J used for calculations.

n	Total number of junctions	Shorting junctions ^{a)}	Open circuits ^{b)}	Unstable junctions ^{c)}	N_J ^{d)}	Working device yield [%]
12	32	17	1	2	240	37.5
14	34	14	2	1	340	50.0
16	22	8	3	1	200	45.5

Figure 4.6 (a) shows a plot of a full trace (forward and backward) log-averaged [5, 23, 33, 41] $|J|$ as a function of V , for different lengths of n -alkanethiols ($n_c = 12$ –16). The physical explanation for taking the average of the $\log(|J|)$ values is that J depends exponentially on the thickness of the tunneling barrier, d , which is normally distributed [41]. Because of this, the mean, $\mu_{\log}$, and standard deviation, $\sigma_{\log}$, of the $\log(|J|)$ data were determined. Figure 4.6 (b, c, d) shows graphs of $\log$ -

averaged $|J|$ of the three n -alkanethiols separately, with ± 1 standard deviation. Table 4.2 shows an overview of $\mu_{\log} \pm \sigma_{\log}$ values, determined at 1, 0.5, and 0.2 V.

Figure 4.6. (a) Plot of log-averaged $|J|$ as a function of V , for different lengths of n -alkanethiols ($n_c = 12$ – 16). The plot contains a full trace (up and down), showing perfect overlap. (b, c, d) Plot of log-averaged $|J|$ (± 1 standard deviation) as a function of V , for different lengths of n -alkanethiols ($n_c = 12$ (red), 14 (blue), 16 (green)). The Y-axis of (c) and (d) is equal.

Table 4.2. Arithmetic average and standard deviation of $\log(|J|)$ ($\mu_{\log}$ and $\sigma_{\log}$), after excluding shorts and unstable junctions, determined at 1, 0.5 and 0.2 V for different lengths of n -alkanethiols ($n_c = 12$ – 16).

n_c	1 V $\mu_{\log} \pm \sigma_{\log}$	0.5 V $\mu_{\log} \pm \sigma_{\log}$	0.2 V $\mu_{\log} \pm \sigma_{\log}$
12	-0.79 ± 1.18	-1.23 ± 1.13	-1.75 ± 1.11
14	-1.28 ± 1.02	-1.78 ± 1.09	-2.31 ± 1.13
16	-2.04 ± 0.53	-2.49 ± 0.57	-2.99 ± 0.57

A large body of work suggests nonresonant tunneling through alkanethiol SAMs [28]. For different lengths of *n*-alkanethiols, *J* roughly obeys:

$$J = J_0 e^{-\beta d}, \quad (4.1)$$

where β (n_c^{-1}) is the decay coefficient, *d* (n_c) the thickness of the SAM and *J*₀ is a constant (*J* at *d* = 0) that depends on the system and includes the contact resistance.

Figure 4.7 shows the $\mu_{\log}$ values ($\pm\sigma_{\log}$) of the different *n*-alkanethiols, determined at 0.2, 0.5, and 1.0 V. The straight lines show Equation 1 with the parameters β and *J*₀ ($\text{A}\cdot\text{cm}^{-2}$) determined from a linear fit of $\ln(|J|)$. A β value of $0.72 \pm 0.09 \text{ n}_c^{-1}$ ($J_0 = 1000 \pm 4 \text{ A}\cdot\text{cm}^{-2}$) was determined at a bias of 1 V, a β value of $0.73 \pm 0.06 \text{ n}_c^{-1}$ ($J_0 = 401 \pm 2 \text{ A}\cdot\text{cm}^{-2}$) at 0.5 V, and a β value of $0.72 \pm 0.03 \text{ n}_c^{-1}$ ($J_0 = 102 \pm 2 \text{ A}\cdot\text{cm}^{-2}$) at 0.2 V, showing an insignificant dependence of the β value on applied bias. A direct comparison of these data is difficult, because practically no data exist on large-area metal-molecular monolayer-metal junctions or an “interlayer” is being used to protect the SAM from shorts. When looking broader, the derived β values fall within the range of reported values in the literature (from 0.51 to 1.16), also when compared to the majority of the values (from 0.73 to 1.11) [28]. It has to be noted that these data originate from many different electronic test beds, with and without an interlayer, using mono- and dithiols as the SAM and having one or two chemisorbed contacts.

When comparing the current density ($3.24 \times 10^{-3} \text{ A}\cdot\text{cm}^{-2}$ for *C*₁₆ alkanethiol at 0.5 V) to other “large-area” methods, for example EGaIn ($\approx 5 \times 10^{-5} \text{ A}\cdot\text{cm}^{-2}$) [41], or PEDOT:PSS ($\approx 8 \times 10^{-6} \text{ A}\cdot\text{cm}^{-2}$) [5], the current density is, as expected, higher. This is most likely coming from the fact that there is no protecting layer in between the SAM and metal. When comparing to the direct deposition method ($\approx 8 \times 10^{-1} \text{ A}\cdot\text{cm}^{-2}$) [11], our method clearly has a lower current density. This is also to be expected, because it is known that direct evaporation increases defects and metal filament formation. Comparing the current density ($5.9 \times 10^{-2} \text{ A}\cdot\text{cm}^{-2}$ for *C*₁₂ alkanethiol at 0.5 V) to a fabrication method with a thin layer of reduced graphene oxide as a “protective layer” ($\approx 2 \times 10^{-1} \text{ A}\cdot\text{cm}^{-2}$), [14] where the resistance contributed by the graphene layer should be negligible, these current densities are highly comparable.

Figure 4.7. Plot of log-averaged $|J|$ as a function of the number of carbon atoms, n_c , of the n -alkanethiol used in the junction (± 1 standard deviation) at different voltages (1, 0.5, and 0.2 V), including Equation 1 (straight lines) with the parameters β and J_0 determined from a linear fit of $\ln(|J|)$.

Comparing our yield ($\approx 45\%$) to yields of other floatation methods (for example PALO $\approx 70\%$ [26], MoPALO $\approx 80\%$ [27]), the relatively low yield has two probable origins. The method reported here is the first case in which a floatation method is used in combination with alkanemonothiols on Au. Other floatation techniques were only shown to work in combination with Si or oxidized Al. In our case, it may be possible to improve the yield by improving the monolayer quality even more (to obtain higher contact angles and less hysteresis), but having structured bottom electrodes instead of unstructured ones, as is for example the case for (Pe)MoPALO [27], is probably a larger problem. The structured bottom electrodes can give problems at the edges, where the SAM is less ordered, therefore more prone to metal filament formation and thus resulting in shorts. This is the most important reason why the electrodes were embedded. The structured bottom electrodes are important when considering measuring far away from the molecular junction and molecular junction integration in for example a crossbar architecture.

Even though the yield is somewhat lower, this method is an improvement from the perspective of device architecture and fabrication. Not only are thiols on Au now possible to study with floatation methods, but because this method only has a lift-off step in water, the interface between the molecular monolayer and metal top electrode is cleaner compared to the PALO/PeMoPALO method, which needs a HF detachment step and in the case of PeMoPALO has a floatation step from ethyl acetate [30].

With the design presented here (long “narrow” electrodes), we did not visually encounter any trapped water and all electrodes were well stretched without wrinkles. In case of another design (round dots embedded in the same way), however, some problems occurred with trapped water. We suggest this originates from the fact that the round dots are completely embedded in a hydrophobic area, while when using long “narrow” electrodes, the water can escape to the unmodified Au sides of the molecular junctions. To further investigate that our results are not affected by trapped water in the molecular junction, a control experiment was performed by making metal-metal contacts, without a SAM in between, with the wedging transfer technique. The resulting resistances were in the range of $\approx 100 \Omega$ for a $100 \mu\text{m}^2$ junction area or lower for larger areas of the junctions. These values were in the same range as metal-metal contacts made without the floatation method, the resistance of the two leads measured separately, and as the measured shorts in the presence of a SAM in the molecular junction. Compared to the dodecanethiol SAM (average of 23.2 M Ω) this is several orders of magnitude lower. The metal-metal I - V curves showed clear linear behaviour, indicating no problems with trapped water.

We also investigated the change of current density as a function of time and found that the small changes after several weeks, fall within the experimental error range. We tried to group the data of one thiol in different batches as a function of area and determined log-averaged current densities. These were, statistically speaking, not significantly different. Although these control experiments are convincing, we cannot completely exclude the presence of a few layers of water molecules. However, if present, such contamination has an apparently negligible effect on the charge transport.

4.3 Conclusion and Outlook

In this study, a floatation method is presented for fabricating and electrically characterizing symmetric, large-area molecular junctions, with a relatively high yield which allows statistically relevant numbers of measurements to be obtained in a practical manner (≈ 500 or more complete $J(V)$ curves on 50 or more molecular junctions per day). It is the first time that floatation methods are shown to work with metal/metal contacts, while previous reports only showed Si or oxidized Al as bottom contacts. The viability of this fabrication method was indicated by using n -alkanethiols as a reference system, showing an exponential length dependence of tunneling current for different lengths of n -alkanethiols, with a β value of $0.72 \pm 0.09 \text{ } n_c^{-1}$ ($J_0 = 1000 \pm 4 \text{ A}\cdot\text{cm}^{-2}$, determined at 1 V) which is in the range of the majority of reported values in the literature. The characteristics of the fabrication method now permits straightforward extension of this system to a variety of molecules and electrodes, and the study of the relationship between organic structure and tunneling current in monolayers, without the problem of introducing ambiguities in the interpretation of data. When using no additional, protecting layer on top of the monolayer, it appeared crucial to apply the top electrodes as gently as possible. Manual application of ultra-smooth top electrodes embedded in OA on a PDMS stamp worked, but the approach was probably not gentle enough, as indicated by a yield of $\approx 10\%$. Applying the top electrodes with the wedging transfer method is a softer procedure and resulted in a greatly enhanced yield. As both the bottom and top electrodes are ultra-smooth and structured by photolithography, this method can be extended to other metals, as long as the metal is poorly adhering to the native SiO_2 . This gives the opportunity to study the influence of the metal work function on the electronic performance of molecular monolayer devices. Equally important is the combination of the photolithographic electrode patterning with an alignment step while applying the top electrode opens the door to integration into more complex devices.

Experimental

General Information

Single side polished p-type Si(100) wafers were purchased from Okmetic. Cellulose acetate butyrate (average $M_n \approx 30$ kDa) and 1-dodecanethiol ($\geq 98\%$) were purchased from Sigma Aldrich. 1-Tetradecanethiol ($\geq 98\%$) and 1-hexadecanethiol ($\geq 95\%$) were purchased from Fluka. 1H,1H,2H,2H-Perfluorodecyltrichlorosilane (PFDTs, $\geq 97\%$) was purchased from ABCR GmbH. Negative photoresist (TI35 ES) was purchased from MicroChemicals and developer, Olin OPD 6242, was purchased from FujiFilm. HMDS was purchased from BASF. Optical adhesive (No. 61) was purchased from Norland. Solvents were of analytical grade, except for ethyl acetate (technical grade). All chemicals were used as received.

Electrode fabrication

The following procedure was used for fabricating Au electrodes without an adhesion layer. The negative photoresist TI35 ES was used as a metal lift-off mask to generate the electrode pattern. This resist was chosen for the negatively tapered sidewalls, which is preferred in single-layer lift-off. First, the electrode pattern was created in the negative resist. The process started with spin-coating an adhesion layer, HMDS (5 s 500 rpm, 30 s 4000 rpm), after which TI35 ES was spin-coated (5 s 500 rpm, 30 s 4000 rpm) followed by a pre-exposure bake step (2 min, 95°C). The photoresist was exposed (20 s, EVG EV620 Mask Aligner, Hg-lamp 12 mW·cm⁻²) through a patterned photomask, followed by a degassing step (30 min), a post-exposure bake (2 min, 120°C) and a flood exposure (60 s, no mask). The wafer was then developed in Olin OPD 4262 (60 s) and rinsed with Milli-Q water in a quickdump rinser. Prior to metal evaporation, the wafer was cleaned with UV-ozone (PR-100, UVP inc) for 30 min, guaranteeing a clean and poorly adhering native silicon oxide substrate. Immediately after this step, 100 nm Au was evaporated (BAK 600, Balzers), with a deposition rate between 2–4 Ås⁻¹ ($< 10^{-6}$ mbar). This evaporation needs to be controlled carefully: a too low evaporation rate resulted in damaged electrodes at the metal lift-off step while a too high evaporation rate resulted in incomplete template stripping. After the evaporation step, metal lift-off was performed by placing the wafer gently in a resist stripper (Baker PRS 2000) for 60 min. When the lift-off was tried in acetone, the wafer did

not completely clean. Normally, a sonication step is also used, but this destroys the Au electrodes when no adhesion layer is used. Afterwards the wafer was gently dipped in a beaker with deionized water, followed by spin-drying. The bottom electrodes were prepared for template stripping (TS). To lower the adhesion of OA to the Si/SiO₂ first an anti-sticking layer of PFDTs was deposited from the gas phase for 60 min by adding 0.05 mL PFDTs with the substrate in a dessicator, which was pumped down for 10 min [6]. Then drops of OA were applied on top of the bottom electrodes. After applying freshly cleaned glass slides (Thermo Scientific microscopic slides, 1 mm thick, cleaned with piranha for 30 min) on top of the drops, the OA was UV-cured for 2 h. This resulted in a sandwich of Si/SiO₂/Au/OA/glass where the interface between SiO₂ and Au was the weakest. The Au/OA/glass composite was template stripped from the wafer by applying a razor blade at a low angle, with respect to the wafer, at a corner of the glass slide. When applying a small force parallel to the wafer, the Au/OA/glass composite separated from the wafer, which exposed the ultra-flat Au electrodes embedded in the OA.

SAM preparation

All *n*-alkanethiol SAMs were prepared by the same method. After TS of the bottom electrodes, the substrate was immersed in an ethanolic solution of the thiol of choice (5 mM) as soon as possible. The solution was kept overnight (≈ 18 h) under an argon atmosphere. After SAM formation, the substrate was gently rinsed with ethanol and dried with N₂. The quality of the SAMs was checked by contact angle measurements. Table 4.3 shows the static and dynamic water contact angles and the contact angle hysteresis for all alkanethiol SAMs.

Table 4.3. Water contact angles and contact angle hysteresis for C₁₂, C₁₄, and C₁₆.

Alkanethiol (# of carbon atoms, n_c)	θ (°)	θ_a (°)	θ_r (°)	$[\theta_a - \theta_r](^\circ)$
C ₁₂	104.5 $\pm$ 0.6	104.6 $\pm$ 0.6	86.7 $\pm$ 0.4	17.9
C ₁₄	101.1 $\pm$ 1.6	104.0 $\pm$ 0.2	87.7 $\pm$ 0.2	16.3
C ₁₆	111.5 $\pm$ 1.2	112.8 $\pm$ 0.1	98.4 $\pm$ 0.2	14.4

Wedging transfer

The wedging transfer technique was adopted from ref. [32]. In short, the substrate with top electrodes on it was dipped for 5 s into a cellulose acetate butyrate solution (30 mg/mL in ethyl acetate), including 1-dodecanethiol (0.1 vol%) to enhance the sticking of the polymer to the Au. The polymer was dried under ambient conditions for 3 min. In order to allow good wedging transfer, the polymer was dissolved at the bottom and edges of the substrate with a cotton swab dipped in ethyl acetate. The wafer was then slowly dipped into Milli-Q water under an angle of $\approx 70^\circ$, separating the hydrophobic polymer from the hydrophilic wafer. This resulted in a floating polymer layer with the Au electrodes embedded, with the ultra-smooth interface facing downwards. The top electrodes embedded in the cellulose acetate butyrate were manipulated with a micromanipulator while the water level was slowly decreased by a syringe pump. Alignment was done by eye, but when done under a microscope the accuracy would be on the order of microns. With a better micromanipulator a sub-micrometer accuracy can be obtained [32]. After contact was made, the molecular junction device was placed in a desiccator and pumped down overnight to evaporate possible remaining water between the top and bottom contacts. The setup used is shown in Figure 4.8.

Figure 4.8. Set-up for wedging transfer; the cellulose acetate butyrate film with the Au contacts is floating on water in the glass beaker (middle) and is aligned with a micromanipulator (right), contact with the bottom electrodes with the monolayer is made by slowly lowering the water level by pumping out the water with a syringe pump (left).

Electrical measurements

The electrical measurements were done with a Karl Süss probe station connected to a Keithley 4200 semiconductor characterization system. The current-voltage curves were measured by varying the applied voltage in steps of 5 mV from 0 V $\rightarrow$ 1 V $\rightarrow$ -1 V $\rightarrow$ 0 V. Each full trace thus gave two current data points at each voltage value, one from the forward and one from the backward sweep. For all calculations and fitting (except for Figure 4.6) the forward and backward $J(V)$ trace were used together. The applied voltage was started at 0 V to avoid rapid voltage changes across the molecular junction which would otherwise result in turn-on phenomena. The $J-V$ curves were not reproducible when the applied voltage started directly at 1 V. When a non-short junction was measured, the measurement would be repeated another ten times.

AFM measurements

The surface topography of freshly template-stripped Au bottom electrodes was analysed by atomic force microscopy (AFM) under ambient conditions with a Veeco (Bruker) Dimension 3100. Images across various scan areas were recorded in tapping mode using a rectangular silicon cantilever (nanosensors PPP-NCHR) with a tip diameter of ≈ 7 nm and a spring constant of 42 N/m. The rms roughness of the electrodes was determined by averaging over 30 areas from three different electrodes, where each area was $2\ \mu\text{m} \times 2\ \mu\text{m}$.

Contact angle measurements

Contact angles (θ) were measured with MilliQ water ($18.2\ \text{M}\Omega\cdot\text{cm}$) on a Krüss G10 Contact Angle Measuring Instrument, equipped with a CCD camera. Advancing and receding contact angles (θ_a , θ_r) were determined automatically during growth and shrinkage of the droplet by a drop shape analysis software. Results of water contact angles and contact angle hystereses ($\theta_a - \theta_r$) for C_{12} , C_{14} and C_{16} are shown in Table 4.3. Average static contact angles were determined from averaging three different measurements.

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Charge transport in nanoscale vertical organic semiconductor pillar devices made by wedging transfer

In this Chapter, charge transport measurements in nanoscale vertical pillar structures incorporating a thin layer of the organic semiconductor poly-(3-hexylthiophene) (P3HT) are reported. Ultrathin P3HT layers are gently top-contacted using wedging transfer, resulting in well-behaving, robust nanoscale vertical junction lengths carrying very high current densities. Modeling of the current-voltage data for P3HT thicknesses of 40 and 100 nm points at good hole injection and thermally assisted hopping transport through the P3HT. At smaller thicknesses of 5 and 10 nm, the modeling overestimates the measured data, suggesting an edge-on orientation of the P3HT close to the electrodes.¹

¹ Part of this chapter will be submitted as J.G.E. Wilbers *et al.*, “Charge transport in nanoscale vertical organic semiconductor pillar devices made by wedging transfer”. The simulation of the temperature *J-V* data was done in collaboration with Peter A. Bobbert from the TU Eindhoven. Prof. dr. Reinder Coehoorn from the TU Eindhoven is thereby acknowledged for providing the computer code.

5.1 Introduction

For application in light-emitting diodes, field-effect transistors and solar cells, organic semiconductors are playing an increasingly important role due to easy processability and suitability for low-cost and flexible electronics [1, 2]. Properties such as charge carrier mobility, solution-processability, crystallinity and interface properties have to be investigated for implementation of organic semiconductors into electronic devices [3]. For many applications, it is crucial to have sufficiently large current densities [4]. This can be realized by choosing organic semiconductors with large mobilities [5, 6], by reducing the channel length down to the nanoscale [7], or, as demonstrated in this Chapter, both.

For the fabrication of nanometer-sized active channels for planar devices source and drain electrodes have to be patterned by electron-beam lithography (EBL) or other nanolithography techniques [8, 9]. However, many techniques include shadow mask evaporation, which allows only nanoscale sizes in one direction, as shadow masks normally have microscale dimensions.

A vertical configuration, where the organic thin film is sandwiched between two (metallic) contacts, is very attractive because the channel length is defined by the thickness of the organic layer and the device area is given by the overlap of the contacts [10, 11]. Vertical devices enable the investigation of physics of organic semiconductors at the nanoscale, and are already commonly used in molecular monolayer junctions [12, 13]. The vertical geometry has several advantages over planar structures. It offers the possibility to electrically investigate organic layer thicknesses ranging from monolayers to thick layers that have bulk properties. At small junction thickness, the electric field at low voltage can still be very high. The junctions can thus operate at low voltages, while maintaining sizeable current densities, which is beneficial for the implementation into low-power electronic devices like organic light-emitting diodes and organic field-effect transistors [4, 14]. Future applications might be, for example, active matrix displays [15].

Top contacting and nanopatterning of thin layers of organic semiconductors is not straightforward. Direct metal evaporation can result in penetration through the organic film, often leading to damage of the film and electrical shorts [16, 17]. Standard lithography methods that generally include

optical and EBL resists and developers, as well as lift-off procedures in solvents like acetone or dimethyl sulfoxide (DMSO), cannot be applied to pattern organic semiconductors, because most organic semiconductors dissolve in these chemicals [18, 19]. There are methods to avoid damage of the organic layer, for example, by indirect evaporation of metals onto cooled samples [20]. However, in that technique shadow masks are used for patterning the metal top contacts, which do not allow nanostructuring in the lateral dimensions. Other approaches for top contacting organic thin films and/or monolayers are so-called soft-landing techniques such as transfer printing [21, 22], the use of conductive polymers [23] or liquid metals [24] as top contact, lift-off float-on (LOFO) [25] and polymer-assisted lift-off (PALO) [26]. These methods, which are mainly utilized for the fabrication of molecular tunnel junctions, all have their own advantages and disadvantages. They either introduce an additional resistance or an oxide layer, or hazardous chemicals are used during processing. Soft lithography is another way of direct patterning of organic layers [27]. The photoresist used during this soft lithography is compatible with organic semiconductors. However, the metal contact is in this case directly evaporated onto the organic thin film, which can, as already mentioned, lead to electrical shorts especially for thin organic films.

5.2 Fabrication of vertical organic semiconductor pillar devices

In this Chapter, a method to realize vertical organic devices with ultrashort junction lengths down to 5 nm is demonstrated. Thin layers of regioregular poly-(3-hexylthiophene) (P3HT) were gently contacted by wedging transfer [28], and subsequently further structured by dry etching. By applying this water-based technique, EBL-patterned metal top electrodes (200 nm to 2 μ m in diameter) were gently transferred onto P3HT. This was the only step in which EBL was applied. All the other steps were either self-aligning or achieved with standard photolithography. In earlier work (Chapter 4), we showed that we were able to contact self-assembled monolayers (SAMs) of alkanethiols of different lengths by wedging transfer [29]. The SAMs were used as a proof-of-concept for the technique. We now optimized this technique for contacting and patterning P3HT. For our devices we used the *p*-type organic semiconductor P3HT, because it forms

a smooth thin film that can be easily varied in thickness by changing the concentration and/or the spin-coating speed. Regioregular P3HT (with highest occupied molecular orbital (HOMO) of ~ 5.2 eV and lowest unoccupied molecular orbital (LUMO) of ~ 3.0 eV [30, 31]) is widely used for organic-based electronic devices due to its relatively high mobility (> 0.1 cm²/Vs) as compared to other organic semiconductors [32-34]. The high mobility is due to crystallites that form via self-assembly by π - π inter-chain assembly [33]. However, the mobility does not only depend on regioregularity and molecular weight, but also on the solvent used to dissolve the P3HT. The higher the boiling point of the solvent, the slower the solvent evaporates during and after spin-coating, and thus the better the crystallinity of the thin film. A higher crystallinity gives better conductivities [34, 35]. For this reason and the high solubility of P3HT in this solvent [35] we used bromobenzene as solvent. Au was used as electrode material because of its work function around 5.1 eV, which is close to the HOMO level of P3HT [36, 37]. In order to achieve sufficient current injection from the electrode into the organic semiconductor with low contact resistance, the work function has to be aligned to either the HOMO or LUMO level of the organic film [38].

Figure 5.1 schematically shows the fabrication steps of the vertical metal-P3HT-metal pillars. P3HT was spin-coated onto clean Au bottom electrodes on Si/SiO₂ substrates (Figure 5.1 (a, b)). The thickness was varied by different spin-coating speeds and concentrations (2 mg/ml for 5 nm P3HT, 10 mg/ml for 10 nm and 40 nm P3HT and 20 mg/ml for 100 nm P3HT). For wedging transfer hydrophilic areas are required. For the previous SAM devices described in Chapter 4, the molecules were only on the metal bottom electrodes, while the rest of the substrate was hydrophilic. This is different for the P3HT devices. P3HT was spin-coated over the whole substrate, leading to a completely hydrophobic surface. Therefore, we first removed P3HT from the upper part of the SiO₂ substrate (not shown in the figure), and subsequently wedging transfer was performed. The metal top contacts (70 nm thick Au disks with a diameter between 200 nm and 2 μ m) were wedge-transferred onto the P3HT by placing the substrate under an angle of $\sim 45^\circ$ on a grid holder in a beaker with Milli-Q water and slowly pumping out the water (Figure 5.1 (c)). In this way, the cellulose polymer first makes contact with the hydrophilic SiO₂ and then softly lands on the P3HT. In the next step, directional

reactive ion beam etching was performed to form vertical pillars (Figure 5.1 (d)). The Au disks served as an etch mask for the P3HT.

Figure 5.1. Fabrication steps for vertical Au-P3HT-Au pillars: (a) patterning of bottom electrodes by photolithography on Si/SiO₂ substrates; (b) spin-coating of P3HT; (c) wedge transferring of top contacts onto the thin P3HT film [28, 29]; (d) directional dry etching of vertical pillars using oxygen plasma; the top contacts served as an etch mask for P3HT; (e) spin-coating of HSQ and planarization by reactive ion etching with CHF₃ to open up the top Au contacts; (f) evaporation of large top contacts patterned by photolithography.

Next, the pillars were embedded in an insulating layer of hydrogen silsesquioxane (HSQ), which is thinner on top of the pillars than on the substrate due to its planarization effect [39]. The top Au contacts of the pillars were exposed by reactive ion beam etching, while the organic layer was still protected (Figure 5.1 (e)). Subsequently, in order to contact the pillar structures, a 100 nm thick metal

layer was deposited and patterned by photolithography to form large contact pads (Figure 5.1 (f)).

In this way, we fabricated nanoscale Au-P3HT-Au vertical pillar structures and electrically characterized them. A detailed explanation of the fabrication process can be found in the experimental part.

5.3 Results and Discussion

Scanning electron microscopy (SEM) was used to image a cross-section of a metal-P3HT-metal device after directional dry etching and spin-coating of HSQ (see Figure 5.2). The top Au clearly served as an etch mask for the underlying P3HT thin film (see Figure 5.2 (a)). In Figure 5.2 (c), a final device with large top contacts is shown.

We analyzed devices with four different thicknesses of P3HT (5nm, 10 nm, 40 nm and 100 nm) and with different junction areas (pillar diameter between 200 nm and 2 μm). Two-terminal current-voltage (I - V) characterizations were performed in a probe station in vacuum for room temperature (RT) measurements and in a He compressor for low-temperature analysis. Both measurement setups were connected to custom-built low-noise electronics.

Figure 5.2. SEM images (false color) of a cross-section of (a) Pt-P3HT-Au test structures, (b) Au-P3HT-Au structures embedded in HSQ, and (c) final Au-P3HT-Au structures with large top contacts.

Table 5.1. Overview of working device Au-P3HT-Au junctions for different thicknesses and pillar diameter; n.c. stands for non-conductive, us for unstable and s for short circuit. *not taken into account in Figure 5.3 and Figure 5.4 due to values in the compliance of the measurement set-up.

P3HT thickness [nm]	Pillar diameter [μm]	Total number of junctions	working junctions	non-working junctions
5	2	10	2 (1*)	7 (s), 1 (us)
	1	11	6	3 (s), 1 (n.c.) 1 (us)
	0.5	16	8	6 (s), 2 (n.c.)
	0.4	1	1	
	0.3	15	4	10 (s), 1 (n.c.)
	0.2	1	1	
10	2	29	19	8 (s), 2 (n.c.)
	1	35	22	10 (s), 3 (n.c.)
	0.5	39	26	1, (s), 12 (n.c.)
	0.2	12		10 (n.c.), 2 unstable
40	2	8	7	1 (s)
	1	10	9	1 (n.c.)
	0.5	9	7	1 (s), 1 (n.c.)
	0.2	9	6	3 (n.c.)
100	2	4	4	
	1	9	7	2 (n.c.)
total		218	129	89

Table 5.1 shows an overview of all (218) measured Au-P3HT-Au junctions. The total yield of working devices was ~60%. A device is considered as “working” when it shows a non-linear I - V characteristic that is stable over two consecutive sweeps within a factor of 2. Junctions that were either non-conductive (n.c.), unstable (us) or shorted (s) were discarded. A non-conductive device is defined as a junction that shows current values in the noise level of the measurement equipment (10^{-12} A). A device is considered unstable when it exhibits a continuous increase/ decrease in current. A shorted junction has a linear I - V characteristic, typically in a resistance regime of a few 100 Ω. The relatively high working device yield indicates that the fabrication method is less destructive than direct metal evaporation, as even very thin layers in the sub-10 nm regime were successfully contacted and measured.

The current density versus voltage (J - V) characteristics of Au-P3HT-Au devices for different P3HT thicknesses are shown in Figure 5.3. We calculated J by dividing the measured current (I) by the nominal junction areas, and averaging the logarithmic value of J over all junction diameters for each P3HT thickness. The logarithmic average was taken due to the large spreading of the current values. A few junctions were exhibiting very high currents which would otherwise have too much influence on the average value. This is a way of plotting data used in molecular junctions before [40, 41]. The bars represent the standard deviation of the $\log J$ values and provide an indication of the spread in J for devices with the same P3HT thickness.

Figure 5.3. Electrical characterization of Au-P3HT-Au devices in 2-point configuration at RT in vacuum ($< 10^{-4}$ mbar) between ± 0.5 V. The curves were obtained by taking the logarithmic average of the current densities for each P3HT thickness, respectively. Black: 5 nm P3HT (steps: 0.005 V), red: 10 nm P3HT (steps: 0.005 V), green: 40 nm P3HT (steps: 0.02 V), blue: 100 nm (steps: 0.05 V).

Backward and forward J - V sweeps were done and no significant hysteresis was observed, the two sweeps fall on top of each other. The current densities are in the order of 10^2 to 10^6 A/m², depending of the P3HT thickness, which is relatively high for organic junctions and comparable or higher than in P3HT diodes [42]. We observe clearly distinct values of J for different P3HT thicknesses. The J - V characteristics for the different junction diameters are shown in Figure 5.4 and Figure 5.5. It was observed that the current densities for P3HT thicknesses of 10

nm, 40 nm and 100 nm slightly varied with respect to the junction diameter showing the trend of higher J values for larger diameters.

Figure 5.4. Electrical characterization of Au-P3HT-Au devices in 2-point configuration at RT in vacuum ($< 10^{-4}$ mbar) between ± 0.5 V with steps of 0.005 V for (a) 5 nm P3HT and (b) 10 nm. The curves were obtained by taking the logarithmic average of the current densities for each junction diameter, respectively. The graphs on the right side show the corresponding distribution of $\log(I/J)$ at -0.5 V. The different colours stand for the junction diameter: black: 2 μm , red: 1 μm , green: 500 nm, orange: 400 nm, purple: 300 nm, blue: 200 nm.

We attribute this to an area at the circumference of the P3HT pillar that might be affected during RIE and wedging transfer by oxygen and water. We assume that this effect has a stronger impact on smaller pillar diameter since the ratio of affected to non-affected area is larger in this case. This trend was not observed for the devices with 5 nm P3HT. An explanation for this could be that this

extremely thin organic layer was less affected by oxidation due to a shorter etching time.

Figure 5.5. Electrical characterization of Au-P3HT-Au devices in 2-point configuration at RT in vacuum ($< 10^{-4}$ mbar) for (a) 40 nm P3HT between ± 2 V with steps of 0.02 V and (b) 100 nm P3HT between ± 5 V with steps of 0.05 V. The curves were obtained by taking the logarithmic average of the current densities for each junction diameter, respectively. The graphs on the right side show the corresponding distribution of $\log(|J|)$ at (a) -2 V and (b) -5 V. The different colours stand for the junction diameter: black: 2 μm , red: 1 μm , green: 500 nm, blue: 200 nm.

Although top and bottom contacts are made from the same metal (Au), we observe a slightly asymmetric J - V behavior, which we attribute to differences in the top and bottom Au-P3HT interfaces. P3HT was spin-coated onto UV/ozone cleaned bottom electrodes and subsequently annealed, while the top electrodes were applied by wedging transfer onto the P3HT which was exposed to air and water. The energy level alignment between the Au work function and the P3HT HOMO is

influenced by the interface and can thus be changed during processing [36]. Also, the local packing of the P3HT chains at either interface is likely to be different. It is known that there is a strong dependence of the charge transport on the local packing [43, 44]. P3HT thin films contain crystalline areas, formed by $\pi - \pi$ interchain stacking, that are surrounded by an amorphous matrix [33]. The structure of the first nanometers is expected to be different from the bulk of the film [45]. This plays especially a role in vertical devices, while it is less critical for planar structures where, e.g. in an organic field-effect transistor, the current flows in a thin region above the dielectric between the source and drain contacts.

In order to ensure that our fabrication methods allows for reliable, reproducible charge transport measurements we performed stability measurements. The stability was checked with several consecutive *I-V* sweeps and repeated measurements after 21 days to investigate aging at ambient conditions, as illustrated in Figure 5.6.

Continuous *I-V* sweeping showed that the curves were highly reproducible and did not short after several measurements (Figure 5.6 (a, b)). The junctions were also stable over a time window of three weeks, keeping the devices at ambient conditions between the measurements the devices. Some junctions showed only very small variations in current (Figure 5.6 (c)), while others showed slight decrease in current over time (Figure 5.6 (d)).

Figure 5.6. Stability of the Au-P3HT-Au devices measured at RT in vacuum ($< 10^{-4}$ mbar) between ± 0.5 V with steps of 0.005 V (a, c, d) and ± 5 V with steps of 0.05 V (b). (a) 40 consecutive I - V sweeps of a device with 10 nm P3HT and a junction diameter of 1 μm ; (b) 10 consecutive I - V sweeps of a device with 100 nm P3HT and a junction diameter of 2 μm . I - V sweeps over a time window of three weeks for a device with (c) 5 nm P3HT and a junction diameter of 500 nm and (d) 5 nm P3HT and a junction diameter of 1 μm , respectively.

Charge transport in P3HT is generally accepted to be characterized by thermally activated hopping mechanism [46-48]. This implies that the conductance increases with increasing temperature.

Hopping transport is generally described in literature with the Miller-Abrahams model [49]:

$$v_{ij} = v_0 e^{-\frac{2r_{ij}}{a}} \begin{cases} \exp\left(-\frac{\epsilon_j - \epsilon_i}{k_B T}\right) & \epsilon_j > \epsilon_i \\ 1 & \epsilon_j \leq \epsilon_i \end{cases} \quad (5.1)$$

with ν_0 being the attempt hopping frequency, r_{ij} the distance between site i and j , a the average localization radius and e_i and e_j the respective localized energy levels of the sites [50].

Temperature-dependent measurements were performed between 295 K and 150 K with steps of 50 K. The J - V curves during the cooling-down and warming-up cycles show almost no differences and exhibit excellent stability. In Figure 5.7 (a) the current density (in logarithmic scale) for 5 nm P3HT devices is plotted as a function of the inverse temperature, also known as an Arrhenius plot. In the case of thermally assisted hopping transport the activation energy E_a can be extracted from a linear fit of the Arrhenius plots. The transition rate for a single hopping step defined according to the following equation [47]:

$$k = k_0 e^{-\frac{E_a}{k_B T}}, \quad (5.2)$$

with k_B as the Boltzmann constant. The slope of this linear fit is equal to $-\frac{E_a}{k_B T}$. Although there is almost no temperature dependence for devices with 5 nm P3HT, we calculated an activation energy for 5 nm P3HT thickness of 5.1 meV and 14 meV for bias voltages of ± 0.38 V to ± 0.1 V, respectively. The Arrhenius plots of 10 nm, 40 and 100 nm thick P3HT devices show a clear dependence on temperature (see Figure 5.7 (b) and Figure 5.8). The activation energies for 100 nm thick P3HT extracted from the Arrhenius plots are between 78 meV and 48 meV for bias voltages of ± 5 V and ± 1 V, and for 40 nm thick P3HT between 41 meV and 65 meV for bias voltages of ± 2 V and ± 0.4 V, respectively. 10 nm P3HT had activation energies between 19 meV and 25 meV for ± 0.5 V and ± 0.3 V, respectively. The calculated activation energies are comparable to literature data with reported values between 22 meV and 146 meV [47, 51-54].

Figure 5.7. Left: Arrhenius plots of Au-P3HT-Au devices with (a) 5 nm and (b) 10 nm thick P3HT measured between RT and 150 K for different bias voltages. The curves were obtained by taking the logarithmic average of the current densities of all junction diameter, respectively. Right: Distribution of $\log(|J|)$ at (a) -380 mV and (b) -500 mV, the full and dashed bars represent the $\log(|J|)$ values measured in the cooling-down cycle and the during warming-up cycle, respectively.

Figure 5.8. Left: Arrhenius plots of Au-P3HT-Au devices with (a) 40 nm and (b) 100 nm thick P3HT measured between RT and 150 K for different bias voltages. The curves were obtained by taking the logarithmic average of the current densities of all junction diameter, respectively. Right: Distribution of $\log(I/I)$ at -2 V, the full and dashed bars represent the $\log(I/I)$ values measured in the cooling-down cycle and the during warming-up cycle, respectively.

In Figure 5.9 the absolute value of the current density measured at the different temperatures as a function of applied voltage, in the negative voltage regime (current flowing from bottom to top), is plotted on a double-logarithmic scale for 4 representative devices with different P3HT thickness.

The temperature-dependent J - V characteristics were simulated with the drift-diffusion model described in ref. [55]. The model makes use of a mobility function $\mu(T, c, F)$ depending on temperature T , and on the local charge-carrier concentration $c(x)$ and electric field $F(x)$ (x is the distance from the injection electrode), as calculated for thermally assisted hopping in between localized sites

with a site density N_t and random on-site energies taken from a Gaussian density of states (DOS) with standard deviation σ [55]. In the absence of an injection barrier, the work function of the metal is aligned with the center of the DOS and we have $n(0)=n(L)=N_t/2$ as boundary conditions for the solution of the drift-diffusion equation, where L is the P3HT thickness. In the presence of injection barriers φ_1 and φ_2 at the injecting and collecting contact, respectively, we obtain the boundary conditions $n(0)$ and $n(L)$ by evaluating the Gauss-Fermi integral [55].

From the modelling we derive a room temperature zero-concentration, zero-field mobility $\mu_0 = \mu(T = 294\text{ K}, 0, 0) \times 10^{-9} \text{ m}^2/\text{Vs}$, in accordance with other (vertical) devices [56], a site density $N_t = 1.5 \times 10^{26} \text{ m}^{-3}$ and a width of the Gaussian DOS $\sigma = 0.75 \text{ eV}$.

In the modeling, we concentrated on the thickest devices, for which the continuum drift-diffusion model is expected to work best and for which the spread in the data (see Figure 5.3) is the least. One can see in Figure 5.9 (a) and (b) that for representative devices with P3HT thicknesses of 100 nm and 40 nm an excellent modeling of the data is possible. We observed the best agreement of modelled and measured J - V curves when no injection barrier was introduced ($\varphi_1 = \varphi_2 = 0$), which indicates that the injection barrier is very low ($\sim 0.1 \text{ eV}$ or less). The low injection barrier is an indication of the good quality of our devices and the prospect of high current density applications. Based on the abovementioned values for the work function of Au (5.1 eV) and the HOMO energy of P3HT (5.2 eV) we would indeed expect injection barrier of 0.1 eV, but it is known that contaminations of the Au surface can easily lead to injection barriers that are considerable higher.

Figure 5.9 (c) and (d) show measured J - V curves of representative devices with P3HT thicknesses of 10 and 5 nm, together with modeled curves using exactly the same parameters as for the thicker devices. We observe that the overall shape of the curves and their temperature dependence are still rather well described. In particular, the much weaker temperature dependence than in the thicker devices is reproduced. This is a direct consequence of the low injection barrier: because of the low injection barrier even at low temperatures a significant amount of holes diffuse from the metal contact into the P3HT. The much higher average carrier density than in the thicker devices leads to a much weaker temperature

dependence, in accordance with the theoretical prediction [49]. We checked that an increased injection barrier in the modeling increases the temperature dependence, finally leading to activated transport with the injection barrier as activation energy. The weak temperature dependence of the J - V curves for devices with small P3HT thickness is thus a direct indication of the good carrier injection in our devices.

However, a clear shortcoming of the modeling is that the modeled J - V curves are 1 to 2 order of magnitude too high. We checked that such a large difference cannot be explained by an actual P3HT thickness that is higher than the nominal thickness (an unreasonably large deviation would have to be assumed) or by thickness variations in the P3HT film. The most reasonable explanation seems to be the ordering of the P3HT close to the Au electrodes. It is reported in literature that the first few layers of P3HT on a silicon oxide substrate often have a higher amount of edge-on orientation compared to the bulk, which has randomly dispersed π -stacked aggregates [57]. The edge-on orientation facilitates charge transport in the direction along the substrate, but severely impedes it in the vertical direction. In the case that also on Au electrodes in our devices the first few nanometers are in edge-on orientation, the conductivity of the devices with 10 nm and 5 nm P3HT thickness would be much less than in the simulations, in accordance with our finding. For the thicker devices the effect will be much weaker, because the conductivity is then governed by that of the bulk.

Figure 5.9. Experimental (symbols) and modelled (lines) current density J versus applied voltage V (negative voltage regime) characteristics at different temperatures for typical devices with (a) 100 nm, (b) 40 nm, (c) 10 nm and (d) 5 nm P3HT thickness and a junction diameter of 2 μm . Full line: drift-diffusion modeling with room-temperature (294 K) mobility $\mu_0 = 7 \times 10^{-9} \text{ m}^2/\text{Vs}$, volume density of molecules $N_t = 1.5 \times 10^{26} \text{ m}^{-3}$, width of Gaussian DOS $\sigma = 75 \text{ meV}$. $\epsilon_r = 4.4$ was used for the relative dielectric constant of P3HT.

5.4 Conclusions

In this Chapter, the fabrication and characterization of vertical Au-P3HT-Au junctions with thin organic layers (5 - 100 nm) has been shown. The P3HT was gently top-contacted by means of wedging transfer. To the best of our knowledge, this is the first time that a soft-landing technique has been applied to thin films of organic semiconductors. We were able to pattern sub- μm vertical Au-P3HT-Au pillars by

utilizing the wedge-transferred Au top contacts as etch masks for directional dry etching of the P3HT thin film. SEM images showed that the P3HT was well protected by the top contacts and that there was a sharp interface between the metal and the organic layer suggesting that metal does not penetrate through the P3HT. The high working device yield of 60% indicates that the top-contacting is very soft, allowing for charge transport through very thin organic films. The junctions are robust under high current densities and reveal thermally assisted hopping transport characteristics. Excellent accordance was observed for experimental and modelled data for P3HT thicknesses of 100 nm and 40 nm. The calculated current densities for P3HT thicknesses of 10 nm and 5 nm are higher than the measured values, which we attribute to a different orientation of the chains in the P3HT thin film close to the Au electrodes compared to the bulk. In the case of very thin layers the first few layers have a stronger influence on the charge transport than in thicker layers where the charge transport is dominated by the bulk. We conclude that carrier injection in our devices is very good, yielding the prospect of new types of very thin and highly conducting organic devices.

The fabrication technique can be utilized to characterize other organic materials like high mobility *n*-type organic semiconductors [58] or molecular monolayers like ferrocenes with switching characteristics. Next to the organic layer it is also possible to vary the electrode material and exchange the metal with ferromagnetic or superconductive materials. The next step for these devices is the application of a side-gate around the pillar structures for the fabrication of vertical organic field-effect transistors.

Experimental

For all devices we used single side polished p-type Si <100> wafers were purchased from Okmetic. Regio-regular poly(3-hexylthiophene-2,5-diyl), cellulose acetate butyrate (average Mn $\approx$ 30 kDa) and bromobenzene ($\geq$ 99.5% (GC)) were purchased from Sigma Aldrich and used as received.

Electrode Fabrication

The wafers were cleaned for 10 minutes in nitric acid, HNO_3 (99%), rinsed with DI water in a quick dump rinse, followed by 10 minutes cleaning in HNO_3 (69%) at 95°C, quick dump rinsing and spin-drying under nitrogen flow.

Bottom electrodes were patterned on a Si wafer with 200 nm thermally grown SiO_2 by photolithography using an image reversal resist (Ti35 ES) for metal lift off. Therefore, hexamethyldisilazane (HMDS) was spin-coated (4000 RPM) as an adhesion layer followed by Ti35 ES (4000 RPM). The photoresist was pre-baked for 120 sec at 95°C and exposed for 18 sec (EVG, EV620 Mask Aligner, Hg-lamp 12 mW/cm^2) through a photomask. After degassing for > 30 min the photoresist was post-baked for 120 sec at 120°C followed by a flood exposure (60 sec, without mask). The photoresist was developed in Olin OPD 4262 (40 sec) and rinsed with DI water in a quickdump rinser. In order to remove thin resist residuals the wafers were cleaned with UV/ozone (PR-100, UVP inc) for 10 min. The metal electrodes were electron-beam evaporated (BAK 600, Balzers), with a deposition rate of between 0.01 and 0.2 nm/s ($< 2 \cdot 10^{-6}$ mbar). For the bottom electrodes 2 nm of Ti were evaporated as an adhesion layer followed by 20 nm of Au. The bottom substrates were cleaned with UV/ozone and rinsed with ethanol before spin-coating of P3HT to ensure clean and oxide-free electrodes.

To create the top contacts, the electron-beam resist poly(methyl methacrylate) (PMMA A4) was spin-coated at 4000 RPM for 30 minute and baked for 3 minutes at 160°C. Top contact structures were written on p-type Si <100> wafer with native SiO_2 by electron-beam lithography (Raith150-TWO GmbH) with an aperture size of 60 μm , an acceleration beam of 20 kV and a working distance of 10 mm. The PMMA was developed in a mixture of methyl isobutyl ketone (MIBK): isopropanol (IPA) (1:3) for 30 sec followed by 30 sec in IPA and dried under nitrogen flow. Prior to metal evaporation, the samples were treated with UV/ozone cleaning (PR-100, UVP inc) for 2 minutes to guarantee a clean native silicon surface without resist residuals. 70 nm of Au were evaporated to form top contacts. Metal lift-off was performed in VLSI acetone for 10 minutes with low-power sonication. Subsequently, the samples were rinsed with VLSI IPA and dried under nitrogen flow.

Organic Semiconductor Preparation

The region-regular P3HT was dissolved in bromobenzene (2, 10, 20 mg/ml) at 80°C for > 4 hours under stirring. After letting it cool down to room temperature under stirring, the solution was filtered through a 0.2- μ m syringe filter. Before spin-coating of P3HT, the substrates were cleaned with VLSI acetone and IPA for 10 minutes, respectively, followed by rinsing with VLSI ethanol to remove possible Au oxide. The P3HT solution was spin-coated for one minute at speeds of between 5000 RPM and 500 RPM leading to thicknesses from 5 nm to 100 nm. After spin-coating, the P3HT film was annealed at 100°C for 1 hour to let the solvent evaporate. The resulting thickness was measured by atomic force microscopy and a surface profiler.

Wedging Transfer and Pillar Etching

To enable wedging transfer, the top contacts were cleaned for 10 minutes with UV/ozone treatment to remove thin resist residues and to increase the hydrophilicity of the native silicon oxide layer. The substrate was dipped into a solution of cellulose acetate butyrate (CAB) dissolved in ethyl acetate (~30 mg/ml). The CAB layer was allowed to dry for two minutes and was subsequently removed at the edges of the substrate by dipping it into ethyl acetate. When the device was dipped under an angle of about 70° into Milli-Q water, the water penetrated at the interface between the hydrophilic SiO₂ substrate and the hydrophobic CAB polymer. The CAB polymer was thereby lifted-off including the Au structures due to the low adhesion of Au to the SiO₂. The metal structures embedded in the CAB polymer floating at the water interface were transferred onto the new substrate with the Ti/Au bottom electrodes covered by the thin film of P3HT. Therefore, the substrate was held under an angle in the water underneath the CAB with the metal top electrodes, allowing it to gently make contact with the P3HT layer. The devices were dried under ambient conditions overnight. After drying the CAB polymer was removed using ethyl acetate. P3HT does not dissolve in this solvent and was thus not affected by this step.

The wedge-transferred top contacts were utilized as etch masks during directional dry etching by oxygen plasma (20 sccm, 100 mTorr, 10 Watt, 30-60 sec depending on the P3HT thickness) in a reactive ion etch (RIE) system. The

directional dry etch enables the formation of vertical pillars, and the P3HT is thereby removed everywhere except under the top contacts.

HSQ planarization and application of large contact pads for wire bonding

Hydrogen silsesquioxane (HSQ) (DC XR 1541-006 from Dow Corning) was spin-coated at 1000 RPM and cured for 120 sec at 120 °C resulting in 160 nm thick film on the bottom electrodes and 80 nm on top of the pillars. Planarization of HSQ was done by dry reactive ion etching in CHF₃, He, O₂ plasma (Adixen AMS100DE) at -10°C and a pressure of $8 \cdot 10^{-3}$ mbar. The etch rate was 70 nm/min. When the top of the pillars was opened the etching was stopped and 100 nm Au with 2 nm Ti as an adhesion layer were evaporated (BAK 600, Balzers; deposition rate between 0.05 and 0.2 nm/s ($< 2 \cdot 10^{-6}$ mbar)). This top Au layer was photolithographically patterned. Therefore, HMDS is spin-coated (4000 RPM) prior to Olin 17 (4000 RPM). The photoresist was baked for 120 sec at 95°C before exposure. The photoresist was exposed for 4 sec (EVG, EV620 Mask Aligner, Hg-lamp 12 mW/cm²) through a photomask and post-baked for 120 sec at 120°C followed developing in Olin OPD 4262 (60 sec) and rinsed with DI water in a quickdump rinser. Reactive ion beam etching (Oxford i300) with Ar ions was utilized to pattern the top Au layer.

The distance between the Au dots was chosen in such a way that only one dot was placed between the bottom electrode and the large top contacts that were applied in the last fabrication step.

Electrical Measurements

The electrical *I-V* measurements were done in a low-temperature probe-station (Janus ST-500) connected to a custom-built low-noise electronics (IVVI-DAC rack, Quantum Transport designed instrumentation, designed by Ing. Raymond Schouten from Delft University of Technology) [59] in vacuum ($< 10^{-4}$ mbar) controlled by a LabView program.

The temperature dependent transport measurements were done in a He compressor (Oxford Instruments) in two-terminal configuration connected to the low-noise measurement electronic set-up.

SEM and AFM Imaging

For imaging of the pillars and for thickness determination of the P3HT film, atomic force microscopy (AFM) under ambient conditions with a Veeco (Bruker) Dimension 3100 was used. Images were recorded in tapping mode using a rectangular silicon cantilever (nanosensors PPP-NCHR) with a tip diameter of ≈ 7 nm and a spring constant of 42 N/m. Furthermore, a surface profiler Bruker Dektak 8 with a 2.5 μm stylus was utilized for measurement of the P3HT thickness.

The cross-section of the pillars was imaged by high-resolution scanning electron microscopy (FEI, Sirion), FEI Focused Ion Beam System (FIB) and Zeiss Merlin HR-SEM.

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Chapter 6

Fabrication of vertical organic field-effect transistors

In this Chapter, the fabrication of vertical organic field-effect transistors (VOFETs) is described. Metal- organic semiconductor- metal pillar structures were fabricated as described in the previous chapter. These pillars were embedded in an oxide layer grown by atomic layer deposition forming the gate oxide followed by defining of the gate electrodes completely surrounding the pillar structures. Preliminary experiments did not reveal gate action yet.

6.1 Introduction

Properties like solution-processability, suitability for low-cost electronics and flexibility raise increasing interest in organic semiconductors. Future applications are organic light emitting diodes [1], solar cells [2, 3], sensors [4, 5] and organic field-effect transistors (OFETs) [6]. As mentioned in the previous chapter, high current densities are required for application in organic light-emitting diodes [7, 8] and in OFETs for low-cost electronics [9, 10], which can be achieved by decreasing of the active (organic) channel lengths.

OFET structures are different compared to the devices investigated in Chapter 5, as a third electrode, the gate contact, is introduced which tunes the conductance of the organic semiconductor. OFETs exist in many different configurations. The most common OFETs have a planar structure where the organic semiconductor is deposited onto lithographically predefined source and drain contacts on top of a bottom gate electrode separated by an dielectric layer from the source and drain electrodes [11]. When transistor dimensions are scaled-down, the performance is generally improved. However, the influence of the contact resistance on the device performance gets stronger than for large scale devices and weakens the expected improvement due to down-scaling [12-14]. If the gate electrode is applied on top of the organic semiconductor like it is the case for staggered thin film transistors (TFTs), the charge transfer can take place over a larger area which means it expands over the source/drain electrode edges resulting in a lower contact resistance [12, 15, 16]. In this respect, vertical transistor configurations with an organic thin film sandwiched between two metal contacts are very attractive because they allow very short channel lengths. The field from the side-gate is thereby like in the case of staggered TFTs not shielded by the source and drain contacts. In literature vertical ambipolar transistors with a 4 nm thin self-assembled monolayer are presented with a centered gate electrode [17, 18]. In this design, the gate electrode is in the middle of the device surrounded by the organic layer (self-assembled monolayer of proteins). The top contact (drain electrode) was thereby applied by indirect metal evaporation.

A large number of reported vertical organic transistors have a lateral bottom gate and a lateral source contact and are referred to as organic Schottky

barrier or organic permeable base transistors [13]. Most vertical organic transistors with a field-effect (VOFETs) reported in literature are fabricated with a step edge on which the organic semiconductor is vapor-deposited or deposited from solution with bottom as well as top gate electrodes [19-21]. The gate contact is generally formed along the full length of the organic film, so that the charge carriers can flow between the source and drain contacts in a conductive channel comparable to the mechanism known from planar OFETs [13].

In this Chapter, a fabrication scheme for the construction of vertical OFETs with metal- organic semiconductor- metal pillar structures and a side-gate electrode is introduced. In this way, the two-terminal devices discussed in Chapter 5 were extended to three-terminal devices in which the gate electrode is supposed to tune the conductive channel of the organic semiconductor. The organic semiconductors were gently top contacted by wedging transfer. The gate electrode is entirely surrounding the pillars which is expected to induce a very homogeneous electric field by the gate over the pillar.

6.2 Results and Discussion

6.2.1 Device fabrication

Vertical organic field-effect transistors with poly(3-hexylthiophene) (P3HT) as the active layer were fabricated according to the basic process flow as shown in Figure 6.1. Pd-P3HT-Pd pillars were prepared by wedging transfer and dry etching as described in Chapter 5 (Figure 6.1 (a-d)). Instead of Au used in previous devices, Pd was used as an electrode material due to compatibility with atomic layer deposition (ALD). The top contacts were written by electron-beam lithography (EBL) with a bilayer e-beam resist. The usage of a bilayer was necessary to achieve good lift-off because the top contacts for devices with a side gate had to be thicker compared to devices without gates. The reason for this is that back-etching in later process-steps becomes extremely difficult when the top contact is too thin. Top contacts were transferred onto thin films of P3HT by wedging transfer, therefore no adhesion layer was utilized to achieve low adhesion to the SiO₂ substrate.

Figure 6.1. Process flow for VOFETs. (a) bottom electrodes (Ti/Pd) on SiO₂ substrate by photolithography; (b) spin-coating of P3HT; (c) wedging transfer of EBL patterned Pd dots; (d) RIE O₂ for pillar formation; (e) ALD of Al₂O₃; (f) Al gate electrodes patterned by photolithography; (g) spin-coating of HSQ and back-etching to open the top contacts; (h) RIBE to mechanically remove the Al/Al₂O₃ on top of the pillars; (i) second HSQ spin-coating and back-etching followed by definition of large top contact pads by photolithography.

However, for 150 nm thick Pd structures this led to problems since stress occurred during evaporation. As a result, the structures were bending up at the edges. We minimized this bending effect by water cooling of the sample holder during metal evaporation, and by decreasing the diameter for the transferred dots (see scanning electron microscopy (SEM) images in Figure 6.2).

Figure 6.2. SEM images of 150 nm thick Pd dots on a Si/SiO₂ substrate written by EBL with a bilayer resist without an adhesion layer evaporated with water-cooling of the sample holder. Images show the focus on (a) 2 μm diameter dot, (b) 1 μm diameter dot, (c) 500 nm diameter dot.

After wedging transfer of these dots onto thin films of spin-coated P3HT on the Pd bottom electrodes, the P3HT was etched with reactive ion etching (RIE O₂). The whole pillar structures were subsequently embedded in a 20 nm thick layer of Al₂O₃ grown by ALD forming the gate oxide (Figure 6.1 (e)). The process was performed at 100°C to ensure that the organic semiconductor was not damaged. Around these pillars a gate electrode (Al) was evaporated and structured by photolithography (Figure 6.1 (f)). A SEM image of a Pd-P3HT-Pd devices with ALD-Al₂O₃ gate oxide and Al side-gate is shown in Figure 6.3. One can see that the oxide layer grows conformal on the Pd as well as the organic layer. The top contact of the pillar serves as a shadow mask for the gate electrodes, a clear, desired disconnection between the gate next to the pillar structure and the metal on top of the pillar was observed.

Figure 6.3. SEM image (false colour) of a 20 nm Pd/ 60 nm P3HT/ 50 nm Pd cross-section embedded in a 20 nm thick ALD- Al_2O_3 layer and a 20 nm Al side-gate (orange: Pd; red: P3HT; blue: ALD- Al_2O_3 ; green: Al).

As both materials, Al_2O_3 and Al, were also deposited on top of the pillar, the layers had to be removed there in order to get electrical connection to the top contact of the VOFET. Hereby, the device was embedded in hydrogen silsesquioxane (HSQ) and etched back until the Al on top of the pillar was exposed (Figure 6.1 (g)). In the following step, the Al and Al_2O_3 were mechanically removed by reactive ion beam etching (RIE) with Ar ions (Figure 6.1 (h)). The equipment is connected to a secondary ion mass spectrometer (SIMS), so that it can be detected when the Pd is reached. In order to verify that the Al_2O_3 layer was completely etched, the pillar structures were imaged with a conductive-probe atomic force microscope. Mechanical etching also removed most of the HSQ. In order to ensure good insulation between the gate electrode and the top contacts, a second layer of HSQ was spin-coated and etched back till the Pd top contact was open. In the last step, large Ti/Pd contact pads were deposited and patterned by photolithography to contact the VOFETs for electrical characterization (Figure 6.1 (i)).

As already briefly mentioned, bending of the top Pd layer was a problem for the VOFET fabrication. The Pd dot still functioned as a mask for the underlying P3HT during RIE O_2 , however due to the bending a gap occurred at the edges of the dots. In Figure 6.4 a cross section SEM image of a test device on a silicon substrate

reveals that the ALD- Al_2O_3 grows into this gap and thereby largely increases the dielectric thickness in the upper part of the pillar structure.

Figure 6.4. SEM image (false colour) of a Si substrate/ 60 nm P3HT/ 150 nm Pd cross-section embedded in a 20 nm thick ALD- Al_2O_3 layer and a 20 nm Al side-gate (orange: Pd; red: P3HT; blue: ALD- Al_2O_3 ; green: Al).

Devices with thinner top contacts did not show any effect of stress during e-beam evaporation. Nevertheless, these devices were unpractical for further fabrication since the HSQ layer which was spin-coated and etched back till the top contacts were opened up was too thin in this case. The Al/ Al_2O_3 layers on top of the pillars were removed by RIBE. RIBE is mechanical etching and therefore also removes the HSQ that was supposed to protect the gate electrodes. In the case of thin Pd top contacts the HSQ was removed before the Al_2O_3 layer on top of the pillar structures was etched completely so that also the gate electrodes were etched away.

All future devices should be fabricated with thick layers that were evaporated with substrate cooling and small diameters in order to reduce the effect of bending. The electrical measurements discussed in the following section were done on devices with bended top contacts. The layer thicknesses were 20 nm Pd for the bottom electrodes with 2 nm Ti as an adhesion layer, 60 nm P3HT, 150 nm Pd top contacts, 20 nm ALD- Al_2O_3 , 20 nm Al gate electrodes and 2 nm Ti, 100 nm Pd for the large top contact pads. Before deposition of the large top contact pads, the devices were investigated with conductive probe atomic force microscopy (AFM) to ensure that the ALD- Al_2O_3 was entirely removed.

6.2.1 Electrical characterization

Thicknesses of Al_2O_3 layers were verified with high-resolution SEM as well as ellipsometry. The breakdown voltage of 20 nm Al_2O_3 was ~ 15 V which was measured on a devices with Pd bottom contacts and Al top contacts with a junction area of $5 \times 5 \mu\text{m}^2$, leakage through the oxide started ~ 10 V (see Figure 6.5). A value of ~ 15 V is comparable with breakdown voltages of ALD- Al_2O_3 reported in literature [22]. In most cases higher process temperatures ($\sim 300^\circ\text{C}$) are used during Al_2O_3 growth, since our Al_2O_3 was grown at 100°C in order to avoid damage of the organic semiconductor, a lower breakdown voltages was expected compared to layers grown at higher temperatures.

Figure 6.5. Electrical characterization of the 20 nm thick Al_2O_3 grown by ALD at 100°C between (a) ± 10 V and (b) ± 15 V. Measurements were performed at ambient conditions on cross-bar structures with Pd bottom electrodes covered with Al_2O_3 and Al top contacts. The junction area was $5 \times 5 \mu\text{m}^2$.

The VOFET devices were electrically characterized in vacuum ($<10^{-4}$ mbar) at room temperature in a probe station connected to custom-built low-noise electronics. Current-voltage (I - V) characteristics were obtained at different gate bias voltages V_G . There was no dependence of the source-drain current on the applied gate voltage (see Figure 6.6). The gate voltage was applied between the gate and the bottom electrode.

Figure 6.6. Electrical characterization of the vertical OFET with 60 nm of P3HT, a junction diameter of 1 μm and 20 nm ALD- Al_2O_3 as gate oxide at room temperature in vacuum ($<10^{-4}$ mbar). The I - V curves were recorded between ± 2 V with 0.01 V steps and the gate voltage was applied between ± 10 V.

There can be several reasons for the fact that there was no observable gate action so far. In Figure 6.3 and Figure 6.4 one can see that there is a small overhang of the top contact with respect to the underlying P3HT layer. Due to this overhang the evaporated gate electrode was relatively far away from the pillar structure so that the electric field of the gate did not have the desired effect on the organic semiconductor. In addition, the gate contact was very thin, which as well might reduce the gate effect. Another possibility could be that the applied bias voltage (± 10 V) was not high enough to electrostatically tune the carrier concentration in the conductive channel. Higher gate bias voltages were not possible due to leakage of the gate oxide between the gate and bottom electrode above ± 10 V.

The samples can be placed under an angle with respect to the metal source during evaporation in order to get a more conformal deposition of the gate electrode around the pillar structure. In this case the gate electrode is closer to the

conductive channel (on one side of the pillar), so that its electric field has a stronger influence on the organic semiconductor. A SEM image of a test device in which the Al gate was evaporated under an angle of 45° is shown in Figure 6.7. It can be seen that the Al is completely covering the whole channel on one side of the device.

Figure 6.7. SEM image (false colour) of a Si substrate with 20 nm Pt/ 100 nm P3HT/ 150 nm Pd cross-section embedded in a 20 nm thick ALD-Al₂O₃ layer and a 30 nm Al side-gate (orange: Pd; red: P3HT; blue: ALD-Al₂O₃; green: Al). The Al layer was evaporated under an angle of 45° .

It is furthermore recommended to decrease the pillar diameter. This does not only reduce bending of the top contacts but also the gate effect should be higher. Our vertical transistors can in principle be considered as rolled-up planar OFETs in which only a thin conductive channel occurs at the interface with the dielectric upon application of a gate bias.

6.3 Conclusion and Outlook

In this Chapter, the fabrication of vertical organic field-effect transistors with P3HT as the active channel was shown. Pd-P3HT-Pd pillar structures were fabricated by wedging transfer and reactive ion etching. These structures were embedded in Al₂O₃ conformally grown by ALD followed by deposition of the side gates. The devices were embedded in HSQ, which was etched back till the top contacts were opened up. The Al/Al₂O₃ layer on top of the pillars was successfully

etched back to the Pd to enable the deposition of large contact pads for electrical characterization. Electrical measurements revealed no gate effect for the VOFETs yet. Possible explanations are that the gate electrode was too far away from the pillar structure and/or that the applied gate bias was not high enough in order to achieve a strong electric field from the gate electrode to tune the conductive channel of the organic semiconductor.

The scaling laws of FETs suggest a ratio of between the channel length and the thickness of the gate-dielectric of ≥ 10 to achieve good gating effect [23]. As discussed in Chapter 5, in our P3HT devices we observed that, due to a low injection barrier, charge carriers are diffusing into the organic semiconductor from the electrodes even without gate voltage. Therefore, we are expecting a limited contact resistance even with screening of the gate voltage near the source and drain contacts.

It is recommended to evaporate the gate metal under an angle to achieve a more conformal layer closer to the pillar structures and over the whole length of the organic semiconductor. In order to see which gate voltages are required for tuning of the conductive channel, it is recommended to fabricate planar OFET devices with Al as a bottom gate and ALD- Al_2O_3 as the dielectric. On top of these gate electrodes source and drain contacts should be patterned by EBL having the same dimensions as the “rolled-up” VOFETs viz. the width of the nanogap should be equal to the P3HT thickness of the VOFET and the length should be identical with the circumference of the pillars. Although this is a different design structure, it will give an idea about the gate voltage needed to influence the charge transport in the conductive channel.

Experimental

For all devices we used single side polished p-type Si <100> wafers purchased from Okmetic. Regio-regular poly(3-hexylthiophene-2,5-diyl), cellulose acetate butyrate (average Mn $\approx$ 30 kDa) and bromobenzene ($\geq$ 99.5% (GC)) were purchased from Sigma Aldrich and used as received.

Electrode Fabrication

The wafers were cleaned for 10 minutes in nitric acid, HNO₃ (99%), rinsed with DI water in a quick dump rinse, followed by 10 minutes cleaning in HNO₃ (69%) at 95°C, quick dump rinsing and spin-drying under nitrogen flow.

Bottom electrodes were patterned on a Si wafer with 200 nm thermally grown SiO₂ by photolithography using an image reversal resist (Ti35 ES) for metal lift off. The lithography procedure for the bottom electrodes was the same as explained in Chapter 5. In order to remove thin resist residuals the wafers were cleaned with UV/ozone (PR-100, UVP inc) for 10 min. The metal electrodes were electron-beam evaporated (BAK 600, Balzers), with a deposition rate of between 0.01 and 0.2 nm/s ($< 2 \cdot 10^{-6}$ mbar). For the bottom electrodes 2 nm of Ti were evaporated as an adhesion layer followed by 20 nm of Pd. The bottom substrates were cleaned with UV/ozone and rinsed with ethanol before spin-coating of P3HT to ensure clean and oxide-free electrodes.

To create the top contacts, a bilayer EBL resist was utilized to achieve good lift-off results of relatively thick Pd dots. The copolymer (EL9) and the EBL resist poly(methyl methacrylate) (PMMA A4) were both spin-coated at 4000 RPM for 30 minute and baked for 3 minutes at 160°C, respectively. Top contact structures were written on p-type Si <100> wafer with native SiO₂ by EBL (Raith150-TWO GmbH) with an aperture size of 60 μ m, an acceleration beam of 20 kV and a working distance of 10 mm. The PMMA was developed in a mixture of methyl isobutyl ketone (MIBK): isopropanol (IPA) (1:3) for 30 sec followed by 30 sec in IPA and dried under nitrogen flow. Prior to metal evaporation, the samples were treated with UV/ozone cleaning (PR-100, UVP inc) for 2 minutes to guarantee a clean native silicon surface without resist residuals. 150 nm of Pd were e-beam evaporated with a water-cooled sample holder to form top contacts. Metal lift-off was performed in

VLSI acetone for 5 minutes without sonication. Subsequently, the samples were rinsed with VLSI IPA and dried under nitrogen flow.

Organic Semiconductor Preparation

The region-regular P3HT was dissolved in bromobenzene (20 mg/ml) at 80°C for > 4 hours under stirring. After letting it cool down to room temperature under stirring, the solution was filtered through a 0.2- μm syringe filter. Before spin-coating of P3HT, the substrates were cleaned with UV/ozone for 10 minutes, followed by rinsing with VLSI ethanol to remove possible oxide on the metal surface. The P3HT solution was spin-coated for one minute at speeds of between 6000 RPM and 1000 RPM leading to thicknesses from 30 nm to 100 nm. After spin-coating, the P3HT film was annealed at 100°C for 1 hour to let the solvent evaporate. The resulting thickness was measured by atomic force microscopy and a surface profiler.

Wedging Transfer and Pillar Etching

Wedging transfer of the Pd dots onto P3HT and subsequent pillar etching pillar etching by RIE O₂ (20 sccm, 100 mTorr, 10 Watt, 30-60 sec depending on the P3HT thickness) was performed as described in the experimental section of Chapter 5.

Formation of side-gates

The Al₂O₃ gate dielectric was grown in a load-lock equipped atomic layer deposition (ALD) reactor (Picosun). The thermal ALD process was performed at 100°C with two precursor materials: trimethylaluminum Al(CH₃)₃ (TMA) and water. The precursors are alternating pulsed in the reactor starting with TMA. The reactor is purged after every cycle with N₂. Subsequently, 20 nm Al were electron-beam evaporated (BAK 600, Balzers), with a deposition rate between 0.05 and 0.15 nm/s. For patterning of the Al gate electrodes wet etching was performed. The etching properties of Al and Al₂O₃ in the developer Olin OPD 4262 were utilized. HMDS was spin-coated (4000 RPM) prior to Olin 17 (4000 RPM). The photoresist was baked for 120 sec at 95°C before exposure and was exposed for 4 sec (EVG, EV620 Mask Aligner, Hg-lamp 12 mW/cm²) through a photomask and post-baked for 120 sec at 120°C followed developing in Olin OPD 4262 (60 sec). The samples were kept in the

developer until the unprotected Al areas were etched away which could be seen by eye. Afterwards the samples were rinsed with DI water. The remaining photoresist pattern was stripped in acetone and IPA. Hydrogen silsesquioxane (HSQ) (DC XR 1541-006 from Dow Corning) was spin-coated at 1000 RPM and cured for 120 sec at 120 °C. Planarization of HSQ was done by dry reactive ion etching in CHF₃, He, O₂ plasma (Adixen AMS100DE) at -10°C and a pressure of 8×10^{-3} mbar. The etch rate was 70 nm/min. When the top of the pillars was opened the etching was stopped. For removal of the Al and Al₂O₃ on top of the pillar, RIBE (Oxford i300) was utilized.

HSQ planarization and application of large contact pads for wire bonding

Hydrogen silsesquioxane (HSQ) (DC XR 1541-006 from Dow Corning) was spin-coated and etched back in CHF₃ plasma (in CHF₃, He, O₂ plasma, -10°C, 8×10^{-3} mbar) till the top of the pillar structures was opened up as described in the experimental part of Chapter 5. Subsequently 100 nm Pd with 2 nm Ti as an adhesion layer were evaporated (BAK 600, Balzers; deposition rate between 0.05 and 0.2 nm/s ($< 2 \times 10^{-6}$ mbar)) and photolithographically patterned with the Olin 17 resist as described in Chapter 5. Reactive ion beam etching (Oxford i300) with Ar ions was utilized to pattern the top Pd layer.

The distance between the Pd dots was chosen in such a way that only one dot was placed between the bottom electrode and the large top contacts that were applied in the last fabrication step.

Electrical Measurements

The electrical *I*-*V* measurements were done in a low-temperature probe-station (Janus ST-500) connected to a custom-built low-noise electronics (IVVI-DAC rack, Quantum Transport designed instrumentation, designed by Ing. Raymond Schouten from Delft University of Technology) [24] in vacuum ($< 10^{-4}$ mbar) controlled by a LabView program.

SEM and AFM Imaging

For imaging of the pillars and for thickness determination of the P3HT film, atomic force microscopy (AFM) under ambient conditions with a Veeco (Bruker) Dimension 3100 was used. Images were recorded in tapping mode using a rectangular silicon cantilever (nanosensors PPP-NCHR) with a tip diameter of ≈ 7

nm and a spring constant of 42 N/m. Furthermore, a surface profiler Bruker Dektak 8 with a 2.5 μm stylus was utilized for measurement of the P3HT thickness. For inspection if the $\text{Al}/\text{Al}_2\text{O}_3$ was completely removed from the top of the pillar structures conductive probe AFM was utilized. Images were taken in contact mode with a platinum silicide on n^+ -silicon probe (nanosensors, Pt-Si-CONT-20). Contact mode can be utilized without damage to the pillar structures due to the very soft tip which has a cantilever length of $450 \pm 10 \mu\text{m}$, a resonance frequency of 6 -21 kHz and a force constant of 0.02 – 0.77 N/m.

The cross-section of the pillars was imaged by high-resolution scanning electron microscopy (FEI, Sirion), FEI Focused Ion Beam System (FIB) and Zeiss Merlin HR-SEM.

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Fabrication of nanogaps by edge lithography for DNA detection

In this chapter, a method for large-area nanogap fabrication is presented. Metal electrodes with very controllable thicknesses were thereby evaporated onto pre-defined undercuts formed by wet etching of silicon. Nanogaps especially find application in molecular electronics where molecules are assembled between two metallic electrodes in so-called molecular junctions. Other application areas are sensors for biological samples. We plan to use our chips as nanoscale sensors for sequence specific detection of deoxyribonucleic acid (DNA). This is especially important for disease identification.

Preliminary results on electrode surface functionalization and trapping of DNA molecules are shown. DNA itself is not conductive, a process scheme for DNA metallization is discussed. Electrical measurements show that the DNA was metallized, while unspecific metallization was prevented.¹

¹ The work described in this chapter was done in collaboration with Erwin Berenschot and Dilu G. Mathew. Many thanks to Erwin for all support during fabrication and for designing of all 3D images. Surface modification and DNA metallization were performed by Dilu during his MSc thesis.

7.1 Introduction

As already discussed in Chapters 4 to 6, molecules are expected to be employed as rectifiers, switches and transistors [1-4]. In order to be able to investigate the properties of molecules, they have to be electrically contacted. Electrical characterization can be done by scanning tunneling microscopy (STM) or conductive-probe atomic force microscopy (CP-AFM) [5, 6]. However, these methods only enable characterization of the molecules, but do not allow the implementation of (single) molecules into electronic devices. A nanogap device consists of two metallic contacts which are separated by a nanometer-sized gap. In this gap molecules can be assembled. Nanogaps play a crucial role in molecular nanoelectronics. A large variety of nanogaps already exists. Exemplary techniques for the fabrication of nanogaps are mechanical break junctions [7], electron-beam [8] or focused ion beam lithography [9], shadow mask evaporation under an angle [10], and electromigration [11]. More examples for nanogap fabrication can be found in the review articles of reference [1, 4].

Nanogaps are moreover utilized as biosensors to recognize biological samples. Examples are the detection of nucleic acids or proteins at very low concentrations in which molecules are translocated through nanogaps/ nanopores while the ionic current is continuously recorded or in which the electrodes are functionalized for antigene/antibody detection [12, 13]. For the implementation of nanogaps for biomedical chips, the fabrication has to be highly efficient, mass producible and inexpensive. Techniques like electron-beam or focused ion beam lithography are consequently less attractive.

In this Chapter, we present a method to fabricate a large number of nanogaps on a chip by utilizing edge lithography and photolithography. The etching properties of Si <111> were used for the formation of sharp undercuts. Metal electrodes were subsequently e-beam evaporated on top of these undercuts and thereby form the nanogap. The size of the nanogap can be easily controlled by the thickness of the metal. The fabrication is relatively straightforward and enables the construction of laterally displaced vertical nanogaps over a large area in a short time. We are planning to functionalize the metal electrodes to detect specific sequences of single-stranded deoxyribonucleic acid (DNA) molecules with the final

goal to deliver a chip which is capable of trapping sequence-specific, hypermethylated DNA (hmDNA) in these gaps. Hypermethylated DNA occurs in cancer cells and is utilized as a marker for early- stage cancer detection [14, 15].

Exemplary methods for detection of hmDNA include polymer chain reaction (PCR) [16], surface plasmon resonance sensors [17], ion-sensitive field-effect transistors [18], and electrochemical biosensors [19]. With our chips we aim for the electrical detection of hmDNA.

The basic idea is that the metal surfaces are first functionalized with thiolated single-stranded DNA molecules (thiolated oligonucleotides) with sequences that are associated with specific kinds of cancer. In order to trap the target DNA over the nanogap, the two electrodes will be functionalized with two different sequence-specific oligonucleotides to which the target DNA can attach. Therefore, the thiolated oligonucleotides will be electrochemically stripped on one electrode [20] and be replaced by the second thiolated oligonucleotides. Pre-concentrated single-stranded, hmDNA will subsequently be introduced and be trapped between the two electrodes by hybridization if the target DNA has complementary sequences with the thiolated oligonucleotides on the electrodes. The pre-concentrated DNA will be delivered from urine samples from which hmDNA will be extracted and denatured to single-stranded DNA by heating. The extraction of hm-DNA from the sample solution will be done with SiO₂ pillars functionalized with methyl-binding domain (MBD) proteins. The MBD proteins are expected to immobilize the hm-DNA to the pillars. After elution of the hm-DNA with a salt solution, denaturation will be performed by heating. We would like to produce a biosensor chip that gives reliable results in a short time. In order to check if there is hmDNA inside the sample, electrical characterization will be performed. DNA itself is not conductive and for this reason, we will metallize the DNA after trapping. Electrical measurements either reveal open circuits which means that no hmDNA is detected or low resistance which indicates that the sample contains hmDNA. The process for functionalization of the metal electrodes, trapping of hmDNA by hybridization and DNA metallization is illustrated in Figure 7.1.

Figure 7.1. Surface functionalization of the metal electrodes for trapping of hmDNA followed by DNA metallization for electrical detection. (a) Au metal electrodes functionalized with thiolated sequence-specific single-stranded DNA; (b) electrochemical stripping of the thiolated DNA on one electrode and replacing it by the second thiolated sequence-specific single-stranded DNA, (c) trapping of the target DNA and (d) metallization of trapped DNA.

In the project described here, we did not yet investigate hmDNA but started to test the proof-of-principle of the devices. Therefore, the surface treatment of the metal electrodes was investigated and biotin tagged DNA was trapped inside the nanogaps. Tests for metallizing DNA without unspecific metallization inside the nanogaps were performed.

In the following sections, the fabrication of nanogaps, surface functionalization, trapping and metallization of DNA and electrical characterization are discussed.

7.2 Results and Discussion

7.2.1 Fabrication of nanogaps

As substrates p-type Si <111> wafers with 10 nm thermally grown SiO₂ were used. Si <111> was chosen because of its etch profile with a negative undercut. The wafers were cleaned in an ultraclean-line (UCL) UV/ozone steam to remove any organic contaminations prior to oxidation. Oxidation was performed in a furnace at 900°C for 10 min. A thicker SiO₂ layer is unfavorable because the 1% hydrogen fluoride (HF) which was used for wet etching can diffuse into the photoresist and damage the lithography pattern. It is therefore recommended to etch not longer than 3 min. The thickness was checked by ellipsometry. In the next step, the first photolithography step (with a positive photoresist) was done to pattern the SiO₂ layer. The exposed areas of the SiO₂ layer were subsequently etched in 1% HF (etch rate: 4 nm/min), etching stops at the Si substrate.

Figure 7.2. Schematic images of the etch profile of Si <111> after (a) TMAH etch and after removal of the SiO₂ etch mask (light blue: SiO₂).

After stripping of the photoresist in acetone and isopropanol, the Si was etched in tetramethylammonium hydroxide (25% TMAH, etch rate: 25 nm/min) forming the desired undercut. The etching time was depending on the required size of the gap. The reason for first patterning the SiO₂ layer instead of directly etching

Si is that in this way line-roughness is eliminated resulting in perfectly sharp edge profiles as illustrated in Figure 7.2 (a). The SiO₂ etch pattern was removed in 1% HF leaving clean Si undercuts (Figure 7.2 (b)). Directly etching of Si would mean that the Si substrate is not oxidized before photolithography and that the photoresist is used as an etch mask for the Si underneath. This would cause rough edge profiles.

In the following step, the wafers were again homogeneously oxidized. The oxide thickness was increased to 20 nm because the SiO₂ served as an insulating layer between the two metal electrodes that were later deposited. For thermally grown SiO₂ a breakdown field of ~1 V/nm is assumed. The oxide was grown in a furnace at 950°C for 10 min.

For definition of the metal electrodes a second photolithography was done. The image reversal resist TI35 ES was therefore utilized due to its undercut which gives better results for lift-off procedures than positive resists with straight sidewalls. Prior to metal evaporation the patterned wafers were treated with UV/ozone cleaning to remove any resist residuals in the developed areas. Metal was electron-beam evaporated with a rate between 0.01 and 0.2 nm/min. Pt and Au were investigated as electrode material with a 2 nm thin Ti adhesion layer. The thickness of Pt and Au was varied depending on the required gap size. SEM images of the nanogaps before and after metal evaporation are shown in Figure 7.3.

Pt electrodes showed a smoother surface compared to Au electrodes. Furthermore, Au is a softer material and more prone to electromigration. Especially for the formation of gaps < 10 nm, Pt is favorable. For the purpose of trapping DNA inside the gaps, however Au electrodes were used because the surface modification gave better results on Au compared to Pt. Therefore, Au was used for all following experiments.

As a proof-of-concept, we first produced nanogaps with trapped DNA molecules that were not hypermethylated. Therefore, we utilized biotin tagged DNA that would attach to the streptavidin functionalized metal electrodes. The nanogaps were between 15 and 20 nm for these devices. Nanogaps < 15 nm were not necessary due to the length of the DNA molecules (80 base pairs (bp), ~27 nm) used for the experiments.

Figure 7.3. Cross-section images of the undercut (a) after thermal oxidation (red: SiO₂) and (b) after metal evaporation (yellow: metal); on the right side the corresponding SEM images are shown (metal: Pt).

7.2.2 Surface functionalization of the metal electrodes

The surface of the metal electrodes was first treated with a biotinylated SAM with thiol head groups (N-(1-mercapto-11-undecyl)-biotin amide, MUBA) that form chemical, covalent bonds with Au surfaces. Biotinylated thiol molecules are known to form disordered monolayers which hinder good binding of the streptavidin to the biotin [21]. However, when a mixture of biotinylated thiols and 11-mercapto-1-undecanol (MUD, used as a spacer SAM) is utilized, a well-organized, closely packed monolayer is expected [21, 22]. Therefore, we investigated a mixed monolayer of MUBA and MUD to achieve good streptavidin-biotin binding. The chemical structures of MUBA and MUD molecules are shown in Figure 7.4. First contact angle measurements of the SAMs were performed on five different places of the substrates. The contact angle of MUBA on Au was 53.7° and 11.05° for MUD on Au, both values are in agreement with literature [21, 23].

Figure 7.4. Chemical structure of MUD and MUBA molecules [21, 24].

After SAM formation, the functionalized electrodes were incubated in a phosphate buffer saline solution (PBS) containing streptavidin ($1\ \mu\text{M}$ concentration). This results in streptavidin functionalized metal electrodes (Figure 7.5 (a)). The double-stranded test DNA that we used for the experiments was tagged with biotin at both ends which have a strong affinity to the streptavidin. Therefore, the biotin tagged DNA was expected to be trapped inside the nanogap (Figure 7.5 (b)). The concentration of DNA was varied between $1\ \mu\text{M}$ and $500\ \text{nM}$. In order to detect if the DNA was bridging the nanogap, the DNA was metallized (Figure 7.5 (c)).

Figure 7.5. Schematics of (a) surface treatment of the Au electrodes with biotinylated SAMs and streptavidin, (b) trapping of biotin tagged DNA over the nanogap and (c) metallization of the DNA for electrical measurements.

In the following two sections, the surface functionalization characterized by X-ray photoelectron spectroscopy (XPS) and the DNA metallization are discussed. For XPS measurements SAMs were formed on unpatterned Ti/Au and Ti/Pt substrates. Surface functionalization on Pt indicated an oxidation of the metal. Therefore, all devices for trapping of DNA were performed with Au electrodes. The ratio between MUBA and MUD was varied between 1:1 and 1:10. The percentages of the detected elements of the XPS analysis are given in Table 7.1.

Table 7.1. Element concentration in percentage of carbon (C), nitrogen (N), oxygen (O) and sulphur (S) on Au substrates for different ratios of the two SAMs (MUBA:MUD) measured by XPS analysis. The concentration for each element is also given with respect to the Au concentration for comparison between the different SAM mixtures.

Ratio MUBA:MUD	C	C/Au	N	N/Au	O	O/Au	S	S/Au	Au
1:1	54.64	2.05	10.1	0.38	5.73	0.21	2.82	0.11	26.68
1:2	52.62	1.9	9.01	0.32	7.05	0.25	3.31	0.12	28.02
1:4	53.08	1.5	4.11	0.12	5.57	0.16	2.67	0.08	34.57
1:5	51.9	1.5	5.22	0.15	6.33	0.19	2.66	0.08	33.88
1:9	49.89	1.3	2.22	0.06	6.65	0.17	1.53	0.04	39.71
1:10	48.41	1.2	3.45	0.09	7.97	0.20	1.19	0.03	38.99
MUD only	47.22	1.1	0.97	0.02	5.63	0.13	3.08	0.07	43.09
MUBA only	55.8	2.1	8.93	0.34	6.42	0.24	2.38	0.09	26.46
Au only	37.33	0.8	5.29	0.11	4.93	0.10	3.44	0.07	49.01

From this table, especially the N signal gives information about the coverage of the surface by the two molecules, since nitrogen only occurs in MUBA molecules. One can see a decrease of the nitrogen content with increasing amount of MUD in the solution mixture, which indicates that also on the surface the density of MUD molecules increases. By looking at the pure MUBA and MUD monolayers,

it was observed that the Au signal attenuation is stronger for MUBA SAMs than for MUD SAMs, which can be attributed to a thicker monolayer [21].

In the following table (Table 7.2), the elementary concentrations of pure MUD and MUBA SAMs measured by XPS are compared to the expected concentrations according to the chemical structure. The Au content was thereby disregarded and all percentages were recalculated without the Au contribution of the substrate. The carbon content was in good agreement with the calculated values for both SAMs. The higher oxygen content of the MUD SAMs might be attributed to surface oxidation. The sulphur content measured by XPS was a bit lower than expected for both, MUD and MUBA SAMs, this could originate from the distance of the element to the surface of the SAM. Most of the sulphur atoms are at the interface between the molecule and the Au substrate, especially for MUD SAM, with the consequence that the S signal might be attenuated by the tail and functional group.

Table 7.2. Element percentage of pure MUD and MUBA SAMS obtained from XPS analysis, the expected elemental contents were calculated from the chemical structure.

Element (Binding energy (eV))	MUD SAM		MUBA SAM	
	calculated [%]	measured [%]	calculated [%]	measured [%]
C (284.8 ± 0.5)	84.61	82.99	75	74.52
N (400.0 ± 1.0)	-	1.70	10.71	13.82
O (532.3 ± 1.0)	7.69	9.89	7.14	7.82
S (162.5 ± 1.0)	7.69	5.41	7.14	3.85

Table 7.3 and Table 7.4 show the contents of carbon and oxygen species of MUD and MUBA SAMs obtained from XPS analysis of the C1s and O1s levels, respectively. Deviations from the calculated values, especially for the O=C-2N and C=O bonds of MUBA of the O1s level might be attributed with disordered monolayers in which the molecules are lying flat on the surface instead of standing up.

Table 7.3. Percentages of carbon species of pure MUD and MUBA SAMS obtained from XPS analysis, the expected elemental contents were calculated from the chemical structure.

C1s (Binding energy (eV))	MUD SAM		MUBA SAM	
	calculated [%]	measured [%]	calculated [%]	measured [%]
C-C-C (284.8 ± 0.5)	81.81	64.49	57.14	59.79
C-C-S or C-C-N (285.8 ± 0.3)	9.09	18.02	28.57	23.67
C-C-OH (286.7 ± 0.5)	9.09	12.98	-	-
N-C=O (287.5 ± 0.2)	-	-	4.76	9.15
2N-C=O or C-C=O (288.7 ± 0.5)	-	-	9.52	7.39
unattributed contribution	-	4.51	-	-

Table 7.4. Percentages of oxygen species of pure MUD and MUBA SAMS obtained from XPS analysis, the expected elemental contents were calculated from the chemical structure.

O1s (Binding energy (eV))	MUD SAM		MUBA SAM	
	calculated [%]	measured [%]	calculated [%]	measured [%]
C-C-OH (533.08 ± 0.05)	100	97.15	-	-
O=C-2N (531.44 ± 0.05)	-	-	50	73.36
C=O (532.51 ± 0.05)	-	-	50	26.64
unattributed contribution	-	2.85	-	-

The estimated mole fraction of MUBA (χ_2) can be extracted from the XPS analysis by the ratio of the N1s signal of the mixed SAM (MUD and MUBA) to the N1s signal of the biotinylated thiol (MUBA) [21]:

$$\chi_2 = \frac{N1s(MUD+MUBA)}{N1s(MUBA)} \quad (1)$$

In Figure 7.6 the SAM ratio on the surface (χ_2 Surface) is plotted as a function of the SAM ratio in solution (χ_2 Solution). The values for χ_2 Surface were determined from the XPS analysis. The black line shows a linear fit for the ratio range between 0 and 0.34 χ_2 Solution.

Figure 7.6. Relationship between the molar fraction on the surface (XPS data) versus the molar fraction in solution. The black line between 0 and 0.34 ratio of the χ_2 in solution shows a linear fit.

A good orientation of biotinylated molecules was reported for mixed monolayers in which the MUBA concentration was between 10 and 20 % on the surface (χ_2 Surface) [22, 25]. The experimental XPS data do not include such low concentrations, therefore the corresponding values were extracted by interpolation. 10 and 20 % of χ_2 Surface is 0.03 and 0.06 of χ_2 Solution, which corresponds to MUBA:MUD ratios of 1:15 to 1:30 in solution. In the case of pure MUBA SAMs or higher MUBA concentrations in mixed SAMs the monolayers are disoriented and MUBA molecules are expected to lie more often flat on the surface which sterically hinders good streptavidin binding. Good streptavidin binding for low biotinylated thiol and high spacer thiol molecule concentrations is known from literature [21, 22, 25].

7.2.3 Metallization of trapped DNA over the nanogaps

For DNA trapping 20 – 50 μL of biotin tagged DNA solution was drop-casted onto the chips. Before electrical measurements to detect trapped DNA, the DNA had to be metallized. Several approaches exist for metallization of DNA. Metallization procedures range from formation of silver nanowires [20, 26], palladium nanowires [27], platinum nanowires [28], copper nanowires [29] to metallization with Au nanoparticles [30]. For metallization of DNA trapped over the nanogaps we utilized the scheme presented by Braun *et al.*, which consists of three steps [26]: (1) accumulation of silver ions, (2) silver reduction and (3) silver growth enhancement. In the first step, the sample was immersed in a basic aqueous solution of silver salt (AgNO_3 at 0.1 M in aqueous ammonia buffer at pH 10.5).

Other positive ions like Na^+ ions which are already attached to the negatively charged phosphate backbone of the DNA are exchanged with the silver ions. This exchange is also called silver ion accumulation. In the second step, the silver reduction, metallic silver aggregates on the DNA backbone are formed in a basic hydroquinone solution by reduction of the silver ions (50 mM hydroquinone in aqueous ammonia buffer at pH 10.5). In the third step, the DNA was further metallized by electroless deposition of silver ions from acidic solution of excess silver ions and hydroquinone as a reducing agent. The silver aggregates of the second step thereby served as nucleation centres for the silver enhancement (0.1 M AgNO_3 , 50 mM hydroquinone in citrate buffer at pH 3.5). In Figure 7.7 preliminary current-voltage (I - V) curves of trapped DNA with varied concentration and different metallization times are shown. The DNA concentration was 500 nM and 1 μM and the metallization time was chosen 10 and 15 min for the first two steps and 2 and 3 min for the third step, respectively. A reference sample without DNA was measured in order to verify that there was no unspecific metallization between the nanogaps.

Figure 7.7. Preliminary electrical characterization of the trapped DNA with different concentration and metallization times. Black: reference device without DNA; red: 500 nM DNA concentration and metallization times for the three steps of (1) 10 min, (2) 10 min, (3) 3 min; blue: 500 nM DNA concentration and metallization times of (1) 15 min, (2) 15 min, (3) 3 min; green: 1 μ M DNA concentration and metallization times of (1) 15 min, (2) 15 min, (3) 3 min. The red and blue curves show averages of four devices, the green curve is the average of two devices and the black curve shows one measurement.

From the curves it can be seen that devices without DNA were not metallized. An increase in conductance was observed for increased DNA concentration and longer metallization times. The I - V curves showed non-linear behaviour which can be attributed to non-uniform metallization along the DNA molecule as well as oxidation of the silver nanowires. Non-linear I - V characteristics of metallized DNA were reported before [20, 26].

7.3 Conclusions

Nanogaps were fabricated by edge lithography and e-beam metal evaporation over pre-defined gaps. The size of the nanogaps can be tuned by the etching time and the metal thickness. These nanogaps were used for trapping of

biotin tagged DNA by functionalizing the Au electrodes with biotinylated SAMs with thiol head groups. The biotin-streptavidin affinity was employed to bind streptavidin to the surface. The surface functionalization was characterized by contact angle and XPS analysis revealing good binding of the streptavidin for mixtures of MUBA and MUD SAMs which was attributed to more densely packed monolayers compared to disordered pure MUBA monolayers. The biotin tagged DNA was subsequently trapped over the nanogap utilizing again the biotin-streptavidin affinity. The DNA molecule itself is not conductive, therefore the trapped DNA was metallized for electrical characterization. An increase in conductivity was observed after metallization, while there was no conductance for junctions without DNA molecules that were exposed to the same metallization steps. However, it has to be stressed that these results were based on a set of only four devices which does not allow drawing of conclusions. Therefore, a large amount of devices has to be characterized in order to achieve statistically relevant data.

As pointed out, these were preliminary results towards a chip for the electrical detection of hmDNA. It was shown that DNA can be trapped in the nanogaps and detected after metallization. In the future, the electrodes will be functionalized with thiolated sequence-specific single-stranded DNA for the detection of pre-concentrated single-stranded hmDNA. A lot of research needs to be done in order to achieve reliable detection of hmDNA. It is from crucial importance that unspecific metallization is avoided that would lead to unreliable results.

Other applications of the fabricated nanogaps might be molecular junctions for application in organic electronics. The gap size can be accurately tuned in the sub 10 nm range as shown in the SEM image. The undercut onto which the metal electrodes were evaporated was covered with a layer of thermally grown SiO₂. In the case of doped Si substrates the nanogaps bridged by molecules might even work as an organic transistor in which the substrate could be exploited as a back gate with the SiO₂ as the gate insulator. We have already shown that we can also fabricate nanogaps with widths in the sub- μm regime by electron-beam lithography, which could lead to extremely small molecular transistors.

Experimental

p-type Si <111> wafers were dry oxidized in a high-temperature atmospheric furnace for 10 min at 900°C (10 nm SiO₂, first oxide layer) and 10 min at 950°C (20 nm SiO₂, second oxide layer). Prior to oxidation the wafers were cleaned in an ultraclean line (UCL) UV/ozone steam to remove any organic contaminations. Thicknesses of thermally grown SiO₂ layers were measured with a Woollam M-2000UI ellipsometer.

The SiO₂ layer was patterned by photolithography. Hexamethyldisilazane (HMDS) was spin-coated at 4000 RPM to enhance the adhesion of the photoresist to the SiO₂. The positive resist OIR Olin 907-17 was subsequently spin-coated at 4000 RPM followed by a pre-exposure bake for 120 sec at 95°C, exposure was done for 4 sec with a standard photomask and the post bake was done at 120°C for 120 sec. Developing was done for 60 sec in Olin OPD 4262 followed by rinsing with DI water and blow dry with nitrogen. The exposed areas of the SiO₂ layer were subsequently etched in 1% HF (etch rate: 4 nm/min), etching stops at the Si substrate. The photoresist was stripped in acetone and isopropanol. Si was etched in tetramethylammonium hydroxide (25% TMAH at 70°C, etch rate: 25 nm/min) forming the desired undercut with varied etching times depending on the desired gap size.

Electrodes were patterned with an image reversal resist (Ti35 ES) by metal lift off. Therefore, HMDS was spin-coated (4000 RPM) as an adhesion layer followed by Ti35 ES (4000 RPM). The photoresist was pre-baked for 120 sec at 95°C and exposed for 18 sec (EVG, EV620 Mask Aligner, Hg-lamp 12 mW/cm²) through a photomask. After degassing for > 30 min the photoresist was post-baked for 120 sec at 120°C followed by a flood exposure (60 sec, without mask). The photoresist was developed in Olin OPD 4262 (40 sec) and rinsed with DI water in a quickdump rinser. In order to remove thin resist residuals the wafers were cleaned with UV/ozone (PR-100, UVP Inc.) for 10 min. The metal electrodes were electron-beam evaporated (BAK 600, Balzers), with a deposition rate of between 0.01 and 0.2 nm/s (< 2*10⁻⁶ mbar). The thickness of the Ti adhesion layer was 2 nm and the thickness of the Au/Pt was varied depending on the required size of the nanogap.

The cross-sections of the nanogaps were imaged by high-resolution scanning electron microscopy (FEI Focused Ion Beam System (FIB)).

Biotinylated SAMs of N-(1-mercapto-11-undecyl)-biotin amide (99%, Prochimia, Poland) and 11-mercapto-1-undecanol (99%, Sigma-Aldrich, Germany) were formed from solution in HPCL grade ethanol (Merck, Germany) at an overall concentration of 1mM. Chemicals were used without further purification. The devices were incubated in Ar atmosphere for 24 h in the thiol solution and subsequently rinsed with ethanol and DI water and dried under nitrogen flow. Afterwards the samples were sonicated in ethanol, again rinsed with water and dried under nitrogen flow.

Streptavidin (MW $\approx$ 60kDa, lyophilized powder, $\geq$ 13 units/mg protein, Sigma Aldrich, Germany) was stored at -20°C, for surface functionalization it was dissolved in PBS at a concentration of 1 mg/mg. Solutions were stored at 4°C. The PBS powder (pH 7.4 at 25°C, Sigma Aldrich, Germany) was dissolved in DI water at 0.01 M (NaCl 0.138 M, KCl 0.0027 M). The chips with biotinylated metal electrodes were incubated in streptavidin solution for 30 min under gentle sonication and subsequently rinsed with PBS Tween (Sigma Aldrich, Germany; Tween® is a nonionic detergent) followed by DI water and blow dry under nitrogen flow.

Lyophilized biotin tagged double-stranded DNA (80 bp) with was obtained from Eurofins Scientific, The Netherlands. 100 μ M solutions were prepared by adding Milli-Q water and centrifugation. Further dilution to achieve the desired concentration were done with PBS buffer. For DNA trapping 20 – 50 μ L of DNA solution was drop-casted onto the chips. After 30 min of incubation the chips were first rinsed with PBS Tween followed by PBS and blow dry under nitrogen flow.

XPS analysis was done with a PHI Quantera SXM spectrometer (Physical Electronics). The samples were investigated 2 h after SAM formation and kept in a nitrogen box until loading to the XPS chamber. The SAMs were formed on unpatterned 2 nm Ti/20 nm Au and 2 nm Ti/20 nm Pt substrates. For the analysis and X-ray of Al K α , monochromatic at 1486.6 eV, with 2.6 mA, 50 W power and a beam size of 200 μ m was utilized.

Contact angles (θ) of the SAMs were measured with Milli-Q water (18.2 M Ω *cm) on a Krüss G10 contact angle measuring instrument, which was equipped with a CCD camera.

The electrical I - V measurements were performed in a low-temperature probe-station (Janis ST-500) connected to a Keithley 2400 semiconductor characterization system at ambient conditions controlled by a home-build LabView program.

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Top-down nanofabrication of high-density ordered arrays of Si-nanocrystals and nanochannels

In this Chapter, the fabrication of ordered high-density arrays of silicon nanocrystals by exclusively wet etching is demonstrated. Nanolithography (Displacement Talbot Lithography (DTL) and electron-beam lithography (EBL)) was utilized to pattern a 2 nm thin SiO₂ layer which subsequently serves as an etch mask for all further etching steps. The V-grooves furthermore allow for the fabrication of nanochannels by atomic layer deposition of Al₂O₃.¹

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8.1 Introduction

Silicon quantum dots (Si-QDs) are currently attracting a lot of attention due to their enormous application possibilities in the fields of for example quantum electronics, spintronics, photonics, photovoltaics, biology, and nonvolatile memories [1-4]. Porous silicon emits photoluminescence in the visible range and nanostructured silicon is expected to show increased photoluminescence due the quantum confinement [5-8]. The reason for the increased photoluminescence is that the indirect bandgap of bulk silicon is altered into a direct bandgap in quantum confined silicon structures [9, 10]. Silicon nanocrystals can be synthesized by bottom-up as well as top-down fabrication techniques [11-16].

In this Chapter, we describe the top-down fabrication of high-density single-crystalline silicon tetrahedral nanocrystals with dimensions <15 nm by chemical anisotropic etching for application in photonics and electronics. The top-down fabrication of low-density single-crystalline silicon nanocrystals with dimensions down to 25 nm by chemical anisotropic etching based on the photolithographical machining of nanotetrahedra was reported in earlier studies by Berenschot *et al* [17]. For optical measurements a high density of silicon nanocrystals is required which is not achievable with UV-contact lithography. We report on the further development of nanocrystals in arrays with high-density nanocrystals realized by combining chemical anisotropic etching with Displacement Talbot Lithography (DTL, PhableR) [18, 19] and electron-beam lithography (EBL). Hereby, the density of silicon nanocrystals was increased from $10^7/\text{cm}^2$ to $10^{10}/\text{cm}^2$, while the size was reduced to sub-15 nm. The DTL method enables wafer-scale nanopatterning in a very short time. We elaborate on the tuning of the duty-cycle for doubling of V-grooves. The doubled V-groove method by DTL was moreover employed for the fabrication of nanochannels.

8.2 Experimental Methods

We describe the fabrication of silicon nanocrystals made of single-crystalline nanotetrahedra. In alkaline solutions silicon is known to etch anisotropically with a deep etch rate minimum of <111>-oriented surfaces because the <111> face is also during etching atomically flat [20]. For this reason steps are required on the <111> faces in order to continue the etching [21, 22]. Octahedra and tetrahedra structures can be machined by utilizing suitable masks and etching conditions [17].

We started with a silicon <100> wafer with 10 nm thick silicon nitride (Si_3N_4) deposited by low-pressure chemical vapor deposition (LPCVD). The wafer was subsequently patterned by nano-photolithography (Phable 100R tool from Eulitha). This technique is similar to conventional photolithography in which a photoresist is exposed to UV light. However, in the case of DTL the resolution is not diffraction limited thereby enabling large-area, periodic sub-micrometer patterns [18]. DTL enables nanometer-sized structures on the wafer scale which are defined by a mask. For nano-photolithography a bottom antireflection coating (BARC, AZ Barli-II 200) was spin-coated at 3000 rpm for 45 sec followed by a prebake at 185 °C for 1 min. Subsequently, the photoresist PFI88 (diluted 1:1 in propylene glycol monomethyl ether acetate (PGMEA)) was spin-coated at 4000 rpm for 45 sec and prebaked at 90 °C for 1 min. We utilized a phase-shift line mask with a periodicity of 500 nm that resulted in 250 nm periodicity in the photoresist. Exposure was done at $1\text{mW}/\text{cm}^2$ with different exposure doses of 75, 85, 95 and 105 mJ, the target cycle was 20 sec with one precycle, a polarizer was used, the DTL-range was $3\text{ }\mu\text{m}$ and the gap between the wafer and the mask was $\sim 65\text{ }\mu\text{m}$. The post-exposure bake was performed at 110 °C for 1 min. Afterwards the resist was developed for 60 sec in Olin OPD 4262. Both layers, BARC and PFI88, have a thickness of $\sim 160\text{ nm}$. We patterned periodic lines of different line widths over an area of $3\times 3\text{ cm}^2$ as shown in Figure 8.1. The spacings and lines are tuned by the exposure doses.

Figure 8.1. Photograph of a wafer patterned by DTL over an area of $3\times 3\text{ cm}^2$ (middle of the wafer).

For transfer of the PFI88 photoresist pattern into the Barli-II 200, the BARC layer was etched with reactive ion beam etching (RIBE) with oxygen (20 sccm, 180 s) prior to etching the underlying Si_3N_4 . The Si_3N_4 was etched by reactive ion etching (RIE) with $\text{CH}_3 - \text{O}_2$ plasma according to the pattern by nano-photolithography (25

Watt, 25 sccm CHF_3 , 5 sccm O_2 , 30 s). After stripping the BARC and resist with an oxygen plasma, the exposed silicon surface areas (lines) were converted hydrophobic by 50% hydrogen fluoride (HF) etching (10 s) and subsequently V-grooves were anisotropically etched in aqueous potassium hydroxide (20 wt% KOH at room temperature for 5:30 min, etch rate for Si <100>: 20-25 nm/min) using the structured Si_3N_4 as an etch mask (Figure 8.2 (a)). The flat silicon (001) surface was converted into V-grooves bounded by two <111> planes according to the Si_3N_4 pattern [20]. These V-grooves can straightforwardly be doubled. Local oxidation of silicon (LOCOS at 900°C for 35 min, resulting in 21 nm SiO_2) was used to protect the already etched V-grooves and the Si_3N_4 was selectively etched in 1% HF (20 s) to strip the thin oxide layer from Si_3N_4 , subsequently in phosphoric acid (H_3PO_4 , 85%) at 140°C (13 min) to remove the Si_3N_4 and again in 1% HF to remove the interfacial layer between the Si_3N_4 and silicon and to render the silicon hydrophobic (Figure 8.2 (b)). In the next step, the 2nd anisotropic etching was done in tetramethylammonium hydroxide (TMAH, 25% at 70°C for 1 min, etch rate for Si <100>: 0.3 $\mu\text{m}/\text{min}$) to double the pattern (Figure 8.2 (c)). Si <111> can also be etched in KOH when 2-propanol is added to the KOH solution [23, 24]. In aqueous KOH solution, $\text{HO}(\text{H}_2\text{O})_3^-$ ions attach to the (111) planes and thereby protect the (111) planes against OH^- ion attack originating from the KOH [25]. This is the reason for the low etch rate. The addition of 2-propanol exchanges these hydrated ions with alcohol molecules and thereby enables an increased etch rate [23]. We used TMAH instead of KOH due to the stronger selectivity with respect to silicon oxide and because etching of Si<111> is possible in a straightforward way [26, 27]. The etch rate of Si <111> in 25% TMAH at 70°C is 15-20 nm/min [28]. After doubling of the V-grooves the remaining oxide was stripped in 50% HF (Figure 8.2 (d)). 19 nm of Si_3N_4 was deposited by LPCVD followed by dry oxidation to form a thin layer of SiO_2 (Figure 8.2 (e, f)). Every second V-groove was rounded which originates from the LOCOS oxide. Anisotropic etching in combination with LOCOS has been reported for the fabrication of wedge-shaped emitters [29].

Figure 8.2. Patterning of doubled V-grooves [29]. (a) Patterning of the silicon <100> wafer with 10 nm Si₃N₄ by DTL, and etching of V-grooves using Si₃N₄ as mask; (b) LOCOS followed by stripping of Si₃N₄; (c) doubling of the V-grooves; (d) oxide stripping, every second V-groove is rounded due to LOCOS; (e) LPCVD of Si₃N₄; (f) oxidation.

In the second patterning linear V-grooves were patterned with 90° rotation by electron-beam lithography (EBL) (Figure 8.3 (b)). Poly(methyl methacrylate) (PMMA) (A2) was spin-coated at 2000 RPM and baked for 3 min at 160°C as EBL resist. EBL writing (Raith 150) was done with 20 kV, 10 μm aperture, 10 mm working distance and a dose of 160 μC/cm² with step size of 0.02 μm. Developing of the PMMA was done in a 1:3 mixture of MIBK:IPA for 30 sec followed by rinsing with IPA (VLSI) for another 30 sec and spin-drying under N₂. EBL was used to pattern the thin oxide layer. After 1% HF etching for 40 sec of the oxide, the PMMA was removed in acetone and isopropanol, and the structured oxide was utilized to etch the underlying Si₃N₄ in 85% H₃PO₄ at 140°C (Figure 8.3 (c)). SiO₂ is stable in H₃PO₄ for more than 70 minutes. Si₃N₄ has an etch rate of ~0.7 nm/min in H₃PO₄ at 140°C and the selectivity with respect to SiO₂ is more than 40X. The etching was stopped after 44 min and the Si₃N₄ was removed everywhere except in the concave corners (Figure 8.3 (d)). After removal of the SiO₂ layer, the patterned Si₃N₄ was utilized for anisotropical etch of the exposed silicon in KOH (20% at room temperature for 5:30 min, etch rate of Si <100>: 20-25 nm/min) (Figure 8.3 (e)). New <111> planes were thereby formed under the Si₃N₄ mask. The etching is slowed down by the (111) faces that are pinned under the vertex which is formed by the top of the first etched and by silicon nitride protected V-grooves. The second <111> faces are originating

from the pinning of the (111) face with the bottom line of the first etched V-grooves [17]. We then continued the fabrication with so called edge lithography, i.e. retraction of Si_3N_4 [30]. For this isotropic etch, 50% HF was used because of the high selectivity with respect to silicon (Figure 8.3 (f)). The nitride pull-back process is strongly dependent on the geometry of the anisotropically etched silicon. The size of the nanocrystal that will later be formed is determined by the length of the pull-back of nitride and the slow etch rate of Si $\langle 111 \rangle$. The open Si $\langle 111 \rangle$ planes were locally oxidized (LOCOS) before the Si_3N_4 was selectively removed in H_3PO_4 (85%, at 140°C for 25 min, etch rate of Si_3N_4 : 0.7 nm/min; oxide was stripped in 1% HF in advance) (Figure 8.3 (g, h)). The last (4th) anisotropic etching step was again done in 20% KOH at room temperature for 6 minutes and resulted in the creation of the silicon nanocrystals (Figure 8.3 (i)). It was important that the native oxide was properly removed before etching of silicon, otherwise the process will not start which is always the case for etching in KOH. The resulting structures are the SiO_2 patterns from LOCOS with the silicon nanotetrahedra in the tips surrounded from three sides with oxide.

Figure 8.3. Schematic of the Si nanocrystal fabrication. (a) Doubled V-grooves with Si_3N_4 and SiO_2 layer; (b) EBL lines 90° rotated with respect to the V-grooves; (c) etching of SiO_2 , removal of EBL resist followed by patterning of the Si_3N_4 layer (d); (e) removal of remaining SiO_2 and anisotropic etching; (f) retraction of Si_3N_4 by edge lithography; (g) LOCOS; (h) selective etching of Si_3N_4 ; (i) anisotropic etching creating silicon nanocrystals.

8.3 Results and Discussion

8.3.1 Fabrication of nanocrystals

In Figure 8.4, scanning electron microscopy (SEM) images of line patterns in the photoresist PFI88 with 250 nm periodicity are shown for different exposure doses. The variation of the exposure dose enables the tuning of the lines/spacings. The PFI88 lines cannot be wider than half of the period since an underexposure is not possible because the resist pattern is not fully opened in that case. For all used exposure doses steep, vertical resist patterns were observed independent on the development time. Overexposure on the other hand is possible, resulting in thinner lines and wider spacings.

Figure 8.4. SEM images of typical line patterns defined in PFI88 (with Barli-II BARC) for exposure doses of (a) 75 mJ (spacing width: 130 ± 14 nm, line width: 117 ± 13 nm), (b) 85 mJ (spacing width: 148 ± 8 nm, line width: 96 ± 7 nm), (c) 95 mJ (spacing width: 161 ± 5 nm, line width: 86 ± 7 nm) and (d) 105 mJ (spacing width: 167 ± 7 nm, line width: 77 ± 11 nm).

The transfer of the photoresist layer into the BARC was done by RIBE (5 sccm Ar, 10 sccm O₂, 50-55 mA). RIBE results in widening of the decreased line width and increased spacing (see Figure 8.5). The spacing width defined in the PFI88/Barli-II 200 layers increased linearly with ca. 17.5 nm/min and correspondingly the line widths decreased with this rate. For the 250 nm periodicity

line patterns an etch rate of 35 ± 4 nm/min was found for the photoresist PFI88 and 44 nm/min for the BARC Barli-II 200.

Figure 8.5. SEM images of the line pattern in PFI88/Barli-II (a) prior and (b) after treatment with RIBE for 3.5 min. The exposure dose of the photoresist was 75 mJ which corresponds to a spacing width of 130 ± 14 nm and line width of 117 ± 13 nm. After RIBE the measured spacing width was 167 ± 7 nm and the line width was 77 ± 11 nm.

In Figure 8.6 the tuning of the duty-cycle of the doubled V-grooves is shown schematically and with corresponding SEM images. The PFI88 pattern cannot be 1:1 transferred into the BARC layer as discussed above which means that the lines will always have a shorter width compared to the spacings after RIBE. However, a duty cycle of the V-grooves of 50% can still be achieved by tuning of the (111) planes. For exposure of the photoresist a dose of 75 mJ was used resulting in spacings of 130 nm and line widths of 117 nm. The depth of the second V-grooves and thus the duty-cycle can be controlled by the etching time. A short TMAH etch of 1 min resulted in quite shallow second V-grooves. We tuned the duty cycle of the zig-zag structures to 50% by additional 5 min of etching.

Figure 8.6. Tuning of the duty-cycle of the second V-grooves. (a) shallow V-grooves after 1 min etching in TMAH; (b) duty-cycle of 50% after 6 min of TMAH etching with corresponding SEM images of the V-grooves in top view (c) and as a cross section (d, e).

The shape of the bottom of the V-grooves was different for the first and second etching step. From the high-resolution SEM image of the cross section of the conformal deposited Si_3N_4 layer in Figure 8.7 it can be seen that every second groove had a rounded silicon mold with ‘atomic’ sharp <111> plane intersections next to it. We attribute this to the LOCOS step prior to the doubling of the V-grooves.

Figure 8.7. SEM cross sectional image of doubled V-grooves with Si_3N_4 layer with alternating rounded and sharp grooves.

After EBL and patterning of the Si_3N_4 layer, Si_3N_4 nanowires were found either at the bottom of each or of every second V-groove. The number of these nanowires remaining in the concave corners can be controlled by the corner lithography etch factor (E_f) [31]. There can either be 3, 2 or 0 nanowires in three successive grooves depending on both the etch factor and the shape of the V-

groove (Figure 8.8). For a short etching time ($E_f = 1.0$) nanowires were formed in every V-groove, a longer etching time resulted in every second valley with nanowires ($E_f = 1.3$). The nanowires remained in the 'atomic' sharp intersection since the silicon nitride was thicker in these valleys while the nitride was completely removed in the rounded V-grooves. When the devices are overetched ($E_f = 1.78$) it is expected that the nanowires will be removed in each V-groove.

Figure 8.8. Effect of the etch factor (E_f) on the 3rd anisotropic KOH etching step. After Si_3N_4 corner lithography there can be 3, 2 or 0 Si_3N_4 nanowires remaining in the concave corners depending on the corner lithography etch factor. $E_f = 1.3$ which forms 2 nanowires is dependent on the radius of the silicon mold.

In Figure 8.9, SEM images of our devices after the third anisotropic etch are shown for an etch factor of 1.3 with Si_3N_4 nanowires in every second V-groove. The images presents horizontal lines patterned by DTL and vertical lines structures by EBL with highly ordered arrays of $100 \times 100 \mu\text{m}^2$. The first three images (a, b, c) show structures with 200 nm lines/spacing and the last figure (d) shows the results for 100 nm lines/spacing.

Figure 8.9. SEM images after the third anisotropic etching step in KOH showing the large arrays for 200 nm (a-c) and 100 nm (d) lines/spacing, respectively.

On these structures the retraction etch of the Si_3N_4 was performed as depicted in Figure 8.10 (a) followed by the last anisotropic etching in KOH. The final devices with the silicon nanocrystals embedded from three sides in the SiO_2 scaffold are shown in Figure 8.10 (b).

Figure 8.10. SEM images (a) after retraction of Si_3N_4 and (b) the final devices with silicon nanocrystals after anisotropic etching for 200 nm and 100 nm lines/spacing, respectively.

8.3.2 Fabrication of nanochannels

With the combination of DTL and KOH wet etching, we also fabricated nanochannels with widths of 25 nm and openings < 10 nm. Hereby, a silicon <100> wafer with 10 nm Si_3N_4 was patterned with lines of 100 nm and spacings of 150 nm by DTL. The pattern was transferred into the Si_3N_4 layer by RIE (25 sccm CHF_3 , 5 sccm O_2 , 25 Watt, 10 mTorr, for 1 min). After stripping of the resist and BARC layer and 10 sec dipping in 50% HF to remove the oxide on the surface, 150 nm deep V-grooves were etched in KOH (20%, at room temperature, for 6 min) (see Figure 8.11 (a)). Subsequently, 12 nm of oxide was thermally grown. The thin oxide on the Si_3N_4 was removed by 1% HF followed by stripping of the Si_3N_4 in 85% H_3PO_4 at 160°C for 5 minutes. In the second KOH etch (20%, at RT, for 4 min), the V-grooves were doubled forming the nanochannels (Figure 8.11 (b)). The width of the nanochannels can be enlarged by an additional etch in TMAH which also reveals SiO_2 ridges (Figure 8.11 (c)). The structures were subsequently covered with a conformal 5 nm thick Al_2O_3 film by atomic layer deposition (ALD) to further narrow the top-openings and the channel helping to realize achievable confinement in those nanochannels (Figure 8.11 (d)). In the last step, 2 nm of Pd (40 mA, 0.08 nm/s) was electron-beam evaporated under an angle of 38° with 0.2 nm Ti as an adhesion layer (36 mA, 0.03 nm/s) to show that outside of the channels was still accessible without damaging interior of the channels (Figure 8.11 (e)). We are planning to fill these nanochannels

with self-assembled monolayers for investigating one-dimensional molecular charge transport.

Figure 8.11. SEM images of nanochannels. (a) V-grooves etched in KOH, (b) doubling of the V-grooves in KOH, (c) widening of the nanochannels with TMAH etch, (d) ALD of Al_2O_3 , (e) nanochannels after metal evaporation.

8.4 Conclusions

In conclusion, we have demonstrated the fabrication of ordered arrays of high-density silicon nanocrystals by DTL, EBL and wet etching which can be produced on the wafer scale. The density of silicon nanocrystals was increased from earlier reported work from $10^7/\text{cm}^2$ to $10^{10}/\text{cm}^2$, and the nanocrystal size was reduced to sub-15 nm. A combination of corner lithography and directional deposition methods offers the possibility to individually contact silicon nanocrystals in wafer-scale process. High-density arrays in combination with individual contacting may find application in new optical sensing and computing applications. The DTL and wet etching procedure was furthermore utilized for the manufacturing of nanochannels. The V-grooves were thereby conformably covered with an Al_2O_3 layer grown by ALD and a metal layer was evaporated under an angle from both

sides. In future, these nanochannels will be utilized for the investigation of one-dimensional molecular charge transport by introducing molecules into these nanochannels.

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Appendices

Appendix 1: Process flow for metal- molecular monolayer- metal junctions by wedging transfer

	Process	Comments
Patterning of bottom and top electrodes		
1	Lithography- Olin908-Ti 35 ES (#lith140) NL-CLR-WB21 Procedure for 3.5 μm thickness <ul style="list-style-type: none"> • dehydration bake: 10 min • coating: HMDS: 4000 rpm, 30 sec • coating: Ti35 ES: 4000rpm, 30sec • prebake: hotplate 95°C, 120sec • Exposure parameters: 20sec • stabilisation step: roomtemp., >30 min • reversal bake: 120°C, 120sec • Flood exposure: 60 sec <i>Flood exposure should be carried out without a mask in the maskaligner</i> • development: OPD 4262, 60 s • quick dump rinse, DI, <0.1μs • spin drying • visual microscopic inspection 	Si <100> wafer Masks: Flip-chip Bottom / Flip-chip Top (MnF group)
2	UV/Ozone (#surf100) NL-CLR-UV PRS 100 reactor patterns for wet-chemical etching. <ul style="list-style-type: none"> • Time = 30 min 	
3	Evaporation of Au (#film144) NL-CLR-Balzers BAK 600 <ul style="list-style-type: none"> • 100 nm Au (rotation) • Voltage: 10 kV • Emission Current: see MIS logbook • Base pressure: < 1.0$\cdot 10^{-6}$ mbar • Deposition rate 0.2 – 0.4 nm/s 	
4	Lithography- Lift-off NL-CLR-WB11 Use beaker and wafer holder <ul style="list-style-type: none"> • photoresist stripper (PRS 2000) for 60 min • rinse with DI water • spin drying 	
Template-stripping of bottom electrodes		
1	Formation of an anti-sticking layer Use dedicated desiccator <ul style="list-style-type: none"> • 0.05 ml 1H,1H,2H,2H-Perfluorodecyltrichlorosilane (PFDTs) • place the substrates with bottom electrodes in the desiccator • pump down the desiccator for 10 min • leave the sample in vacuum for another 50 min 	MnF lab

2	Application of glass slides by means of an optical adhesive (OA) <ul style="list-style-type: none"> • clean glass slides for 30 min in piranha (3:1 → sulfuric acid (H_2SO_4) : hydrogen peroxide (H_2O_2)) and thoroughly rinse with DI water • apply one droplet of the OA on top of the bottom electrodes and place the glass slide above • cure the OA for 2 h under a UV-lamp 	Bottom electrodes can be template-stripped by placing a scalpel under the edge of the glass-slide and gently remove the glass-slide including the electrodes from the wafer
Wedging transfer of top contacts		
1	Wedging transfer <ul style="list-style-type: none"> • prepare a solution of cellulose acetate butyrate in ethyl acetate (30 mg/ml) with 0.1 volume % of 1-dodecanethiols • dip the substrate with the top contacts into the cellulose polymer and let it dry for 3 min • remove the cellulose polymer at the sides of the substrate with ethyl acetate • for wedging transfer slowly dip the substrate into water under an angle of about 70°, the cellulose polymer including the top electrodes will lift-off and float at the water interface; by lowering of the water level, the top contacts can be transferred to a new substrate (the bottom electrodes covered with a self-assembled monolayer of alkanethiols) 	MnF lab

Appendix 2: Process flow for two-terminal vertical organic semiconductor pillar devices

	Process	Comments
Patterning of bottom electrodes		
1	Cleaning in Ozone Steam (UCP) (#clean100) NL-CLR-WB12 Purpose: removal of organic and inorganic traces. Settings: 2 cycles (overall time: 40:20 min, clean time: 22:50 min)	Si <100> wafer
2	Etching in HF (1%) (#etch217) NL-CLR-WB12 Purpose: strip the native SiO ₂ after cleaning the silicon substrates in Ozone Steam. Beaker 2: HF 1% Time = 1 min	Obligatory for the silicon monitor wafer of the furnace (if applicable).
3	Quick Dump Rinse (QDR) (#rinse121) NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers	
4	Substrate drying (#dry122) NL-CLR-WB Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
5	Clean TLC furnace cleaning (#film195) NL-CLR- A-stack: Furnaces A2,A3,A4 Applications: UCL gate-oxide • Temp.: 1150°C • Gas: O ₂ , 4 liter • TLC: 115 sccm • Ramp: 10°C/min • Cooldown: 7,5°C/min	
6	Dry Oxidation of Silicon (UCL gate oxide) (#film176) NL-CLR-Tempress-furnace A2 • Standby temperature: 700°C • Temp range.: 800 - 1100°C • Gases: O ₂ / N ₂	Process: DRY1100°C (4:40 hours: 303 nm)
7	Lithography-Olin908-Ti 35 ES (#lith140) NL-CLR-WB21 Procedure for 3.5 µm thickness • dehydration bake: 10 min • coating: HMDS: 4000 rpm, 30 sec • coating: Ti35 ES: 4000rpm, 30sec • prebake: hotplate 95°C, 120sec • Exposure parameters: 20sec • stabilisation step: roomtemp., >30 min • reversal bake: 120°C, 120sec • Flood exposure: 60 sec	Mask: bottom electrodes (there is a mask for a full wafer and another mask for 11x11 mm ² samples) Ti35 ES will in future not be available anymore, alternatively the positive photoresist Olin17 can be used in combination with a lift-off resist (LOR) and a mask for pos. resist

		<p><i>Flood exposure should be carried out without a mask in the maskaligner</i></p> <ul style="list-style-type: none"> • development: OPD 4262, 40 s • quick dump rinse, DI, <0.1µs • spin drying • visual microscopic inspection 	
8	UV/Ozone (#surf100)	<p>NL-CLR-UV PRS 100 reactor</p> <ul style="list-style-type: none"> • Time = 300 s 	
9	Evaporation of Ti (#film144)	<p>NL-CLR-Balzers BAK 600</p> <ul style="list-style-type: none"> • 2 nm Ti (no rotation) • Voltage: 10 kV • Emission Current: see MIS logbook • Base pressure: < 1.0*e⁻⁶ mbar • Deposition rate: 0.01 nm/s 	Emission current was first ramped up to ~40 mA and then ramped down to ~32 mA; this enables a very low deposition rate
10	Evaporation of Au (#film144)	<p>NL-CLR-Balzers BAK 600</p> <ul style="list-style-type: none"> • 20 nm Au (no rotation) • Voltage: 10 kV • Emission Current: see MIS logbook • Base pressure: < 1.0*e⁻⁶ mbar • Deposition rate 0.1 – 0.2 nm/s 	
11	Lithography- Lift-off (#litho144)	<p>NL-CLR-WB11</p> <p>Use ultrasonic bath</p> <p>Use beaker and wafer holder</p> <ul style="list-style-type: none"> • Beaker 1: Acetone (gentle sonication) > 10 min • Beaker 2: Isopropanol VLSI > 10min 	
12	Substrate drying (#dry120)	<p>NL-CLR-WB</p> <p>Single substrate drying:</p> <ol style="list-style-type: none"> 1. Use the single-wafer spinner settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples) 	
13	Dicing of a Silicon wafer (#back101)	<p>NI-CLR- Dicing room</p> <p>Use Disco DAD dicing saw or Load point Micro Ace 3</p> <p>Saw type NBC-Z 2050 for silicon wafers</p> <p>Select in blade menu: NBC-Z-2050</p>	samples of 11x11 mm ² (setting for dicing: 11.05 mm)
Patterning of dots for wedging transfer			
1	Dicing of a Silicon wafer (#back101)	<p>NI-CLR- Dicing room</p> <p>Use Disco DAD dicing saw or Load point Micro Ace 3</p> <p>Saw type NBC-Z 2050 for silicon wafers</p> <p>Select in blade menu: NBC-Z-2050</p>	samples of 11x11 mm ² (setting for dicing: 11.05 mm) of a Si <100> wafer
2	Electron-beam lithography (EBL)	<p>NL-CLR-WB23 (polymers)</p> <ul style="list-style-type: none"> • PMMA A4, 2000 rpm for 30 sec, baking: 3 min at 160°C • EBL writing: 20 kV, 60 µm aperture • develop 30 sec in MIBK:IPA (1:3), rinse with IPA and blow dry with nitrogen gun 	Dot diameters: 2 µm – 200 nm, the distance between the dots has to match with the width of the bottom electrodes → adjust the EBL design

			For decreased dot diameters a smaller aperture should be used
3	Evaporation of Au (#film144)	NL-CLR-Balzers BAK 600 <ul style="list-style-type: none"> • 70 nm Au (no rotation) • Voltage: 10 kV • Emission Current: see MIS logbook • Base pressure: < 1.0*10⁻⁶ mbar • Deposition rate 0.1 – 0.2 nm/s 	Au from NE-group in a special crucible was used, it enables evaporation at a lower emission current which is better for small structures in the PMMA resist
4	Lithography- Lift-off (#litho144)	NL-CLR-WB11 Use beaker and small sample holder <ul style="list-style-type: none"> • Beaker 1: Acetone (no sonication!) > 2 min • Beaker 2: Isopropanol VLSI > 2min 	
5	Substrate drying (#dry120)	NL-CLR-WB Single substrate drying: Use the nitrogen gun (fragile, small samples)	
Spin-coating of P3HT			
1	UV/Ozone (#surf100)	NL-CLR-UV PRS 100 reactor <ul style="list-style-type: none"> • Time = 600 s • rinse for 2 min with VLSI ethanol to remove possible oxide on the metal surface 	Cleaning of bottom electrodes prior to spin-coating of P3HT
2	Coating of P3HT	NL-CLR-WB23 (polymers) <ul style="list-style-type: none"> • 500 - 6000 rpm for 60 sec, baking: 3 min at 160°C • annealing: 60 min at 100°C • clean spin-coater 	
3	RIE of polymers - standard (#etch109)	NL-CLR-TETsKe Dirty chamber + Styros electrode <ul style="list-style-type: none"> • Electrode temp.: 10°C • O₂ flow: 20 sccm • pressure: 10 mTorr • power: 30 W 	Shadow mask to protect the patterned areas; P3HT is only remove at the upper part of the sample to enable a hydrophilic area required for wedging transfer Time: depending on the P3HT thickness
Wedging transfer and Pillar etching			
1	UV/Ozone (#surf100)	NL-CLR-UV PRS 100 reactor patterns for wet-chemical etching. <ul style="list-style-type: none"> • Time = 600 s 	necessary for rendering the SiO ₂ substrate of the EBL (Au) dots hydrophilic; otherwise the dots will not lift-off from the substrate
2	Wedging transfer	<ul style="list-style-type: none"> • cellulose acetate butyrate (CAB) in ethyl acetate at a concentration of 30 mg/ml • stirring for ~30 min • dip-coat the substrates with the Au dots into the cellulose and let it dry for a minute; remove the cellulose at the edges of the substrate to allow the water to penetrate between the hydrophobic transfer polymer and hydrophilic substrate • lift-off of the cellulose with the Au dots in Milli-Q water and transfer onto P3HT-coated bottom electrodes 	NE fumehood in MnF lab

		<ul style="list-style-type: none"> • dry overnight at ambient conditions • remove cellulose in ethyl acetate for 5 min, blow dry with nitrogen gun 	
3	RIE of polymers - standard (#etch109)	NL-CLR-Tetske Dirty chamber + Styros electrode <ul style="list-style-type: none"> • Electrode temp.: 10°C • O₂ flow: 20 sccm • pressure: 100 mTorr • power: 10 W 	Time: depending on the P3HT thickness > check with optical microscope
Deposition and patterning of large contact pads for electrical characterization			
1	HSQ spin-coating	NL-CLR-WB23 (polymers) HSQ is stored in the fridge <ul style="list-style-type: none"> • 1000 rpm • baking for 3 min at 120°C 	HSQ thickness: ~160 nm
2	DRIE of HSQ (#etch157)	NL-CLR- AdixenDE Layer thickness: 160 nm SH Temp.: -10°C - Pos.: 120 mm Flows: CHF ₃ : 60 sccm – O ₂ : 10 sccm - He: 150 sccm Pressure: $8 \cdot 10^{-3}$ mbar Source G. W.: 200 W SH Gen W.: 100 W Etch rate of HSQ: ~70nm/min	Check by AFM if the top contacts are opened up
3	Chamber clean Adixen DE (#etch201)	NL-CLR-AdixenDE Chamber clean to remove fluorocarbon needed after every 20 min processing SH Temp: any- Pos.: 150 mm - He pres.: 10 mbar Flow O ₂ : 200 sccm APC: 100% / Pressure: $1.5 \cdot 10^{-2}$ - $6.0 \cdot 10^{-6.5}$ mbar ICP: 2000 Watt CCP: 50 Watt (RF) Clean with a plain Si wafer in the etch tool Cleaning time: 30 minutes	
4	Evaporation of Ti (#film144)	NL-CLR-Balzers BAK 600 <ul style="list-style-type: none"> • 2 nm Ti (no rotation) • Voltage: 10 kV • Emission Current: see MIS logbook • Base pressure: < $1 \cdot 10^{-6}$ mbar • Deposition rate: 0.01 nm/s 	Emission current was first ramped up to ~40 mA and then ramped down to ~32 mA; this enables a very low deposition rate
5	Evaporation of Au (#film144)	NL-CLR-Balzers BAK 600 <ul style="list-style-type: none"> • 100 nm Au (no rotation) • Voltage: 10 kV • Emission Current: see MIS logbook • Base pressure: < $1.0 \cdot 10^{-6}$ mBar • Deposition rate 0.1 – 0.2 nm/s 	
6	Coating of Olin OiR 907-17 (#litho101)	NL-CLR-WB21 Coating: Primus spinner <ul style="list-style-type: none"> • coating: HMDS: 4000 rpm, 30 sec • Olin OiR 907-17 	

		<ul style="list-style-type: none"> • 4000 rpm, 30sec Prebake: hotplate <ul style="list-style-type: none"> • Time: 90 sec • Temp.: 95 °C 	
7	Alignment & exposure of Olin OiR 907-17 (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner <ul style="list-style-type: none"> • Hg-lamp: 12 mW/cm² • Exposure time: 4sec 	Mask: top contacts
8	Development of Olin OiR resists (#litho200)	NL-CLR-WB21 After exposure bake : hotplate <ul style="list-style-type: none"> • Temperature: 120°C • Time: 60sec Development: OPD 4262 <ul style="list-style-type: none"> • 60 sec for developing of the photoresist 	
9	Rinse with DI water	NL-CLR-WB	
10	Substrate drying	NL-CLR-WB use nitrogen gun	
11	RIBE etching Oxford i300 (#etch299)	NL-CLR-Oxford RIBE i300 Motor Platen drive: 5 rpm Platen position: 0° Cooling Cool gas: 5 Torr Platen temperature: 15 °C (active cooling) Neutralizer Ar flow: 5 sccm Current: 100 mA RF generator Power: 300 Watt Beam Ar flow: 5 sccm O ₂ flow: 10 sccm Current: 50 mA Voltage: 300 Volt Accelerator: 300 Volt	Etching until Ti peak disappears

Appendix 3: Process flow for vertical organic semiconductor pillar devices with side-gate

	Process	Comments	
Patterning of bottom electrodes			
1	Cleaning in Ozone Steam (UCP) (#clean100)	NL-CLR-WB12 Purpose: removal of organic and inorganic traces. Settings: 2 cycles (overall time: 40:20 min, clean time: 22:50 min)	Si <100> wafer
2	Etching in HF (1%) (#etch217)	NL-CLR-WB12 Purpose: strip the native SiO ₂ after cleaning the silicon substrates in Ozone Steam. Beaker 2: HF 1% Time = 1 min	Obligatory for the silicon monitor wafer of the furnace (if applicable).
3	Quick Dump Rinse (QDR) (#rinse121)	NL-CLR-Wetbenches Purpose: removal of traces of chemical agents. Recipe 1 Quick dump rinsing (QDR) Recipe 2 Cascade rinsing for fragile wafers	
4	Substrate drying (#dry122)	NL-CLR-WB Single substrate drying: 1. Use the single-wafer spinner settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
5	Clean TLC furnace cleaning (#film195)	NL-CLR- A-stack: Furnaces A2,A3,A4 Applications: UCL gate-oxide • Temp.: 1150°C • Gas: O ₂ , 4 liter • TLC: 115 sccm • Ramp: 10°C/min • Cooldown: 7,5°C/min	
6	Dry Oxidation of Silicon (UCL gate oxide) (#film176)	NL-CLR-Tempress-furnace A2 • Standby temperature: 700°C • Temp. range: 800 - 1100°C • Gases: O ₂ / N ₂	Process: DRY1100°C (4:40 hours: 303 nm)
7	Lithography- Olin908-Ti 35 ES (#lith140)	NL-CLR-WB21 Applications e.g. Lift off of Ti, Pt Procedure for 3.5 µm thickness • dehydration bake: 10 min • coating: HMDS: 4000 rpm, 30 sec • coating: Ti35 ES: 4000 rpm, 30sec • prebake: hotplate 95°C, 120sec • Exposure parameters: 20sec • stabilisation step: roomtemp., >30 min • reversal bake: 120°C, 120sec • Flood exposure: 60 sec	Mask: bottom electrodes (there is a mask for a full wafer and another mask for 11x11 mm ² samples) Ti35 ES will in future not be available anymore, alternatively the positive photoresist Olin17 can be used in combination with a lift-off resist (LOR) and a mask for pos. resist

		<p><i>Flood exposure should be carried out without a mask in the maskaligner</i></p> <ul style="list-style-type: none"> • development: OPD 4262, 35s • quick dump rinse, DI, <0.1µs • spin drying • visual microscopic inspection 	
8	UV/Ozone (#surf100)	NL-CLR-UV PRS 100 reactor patterns for wet-chemical etching. <ul style="list-style-type: none"> • Time = 300 s 	
9	Evaporation of Ti (#film144)	NL-CLR-Balzers BAK 600 <ul style="list-style-type: none"> • 2 nm Ti (no rotation) • Voltage: 10 kV • Emission Current: see MIS logbook • Base pressure: < 1.0*e⁻⁶ mBar • Deposition rate: 0.01 nm/s 	Emission current was first ramped up to ~40 mA and then ramped down to ~32 mA; this enables a very low deposition rate
10	Evaporation of Pd (#film144)	NL-CLR-Balzers BAK 600 <ul style="list-style-type: none"> • 20 nm Pd (no rotation) • Voltage: 10 kV • Emission Current: see MIS logbook • Base pressure: < 1.0*e⁻⁶ mbar • Deposition rate 0.1 – 0.2 nm/s 	
11	Lithography- Lift-off (#litho144)	NL-CLR-WB11 Use ultrasonic bath Use beaker and waferholder <ul style="list-style-type: none"> • Beaker 1: Acetone (gentle sonication) > 10 min • Beaker 2: Isopropanol VLSI > 10min 	
12	Substrate drying (#dry120)	NL-CLR-WB Single substrate drying: 1. Use the single-wafer spinner Settings: 2500 rpm, 60 sec (including 45 sec nitrogen purge) 2. Use the nitrogen gun (fragile wafers or small samples)	
13	Dicing of a Silicon wafer (#back101)	NI-CLR- Dicing room Use Disco DAD dicing saw or Load point Micro Ace 3 Saw type NBC-Z 2050 for silicon wafers Select in blade menu: NBC-Z-2050	samples of 11x11 mm ² (setting for dicing: 11.05 mm)
Patterning of dots for wedging transfer			
1	Dicing of a Silicon wafer (#back101)	NI-CLR- Dicing room Use Disco DAD dicing saw or Load point Micro Ace 3 Saw type NBC-Z 2050 for silicon wafers Select in blade menu: NBC-Z-2050	samples of 11x11 mm ² (setting for dicing: 11.05 mm) of a Si <100> wafer
2	Electron-beam lithography (EBL)	NL-CLR-WB23 (polymers) <ul style="list-style-type: none"> • Copolymer EL9, 2000 rpm for 30 sec, baking: 3 min at 160°C + PMMA A4, 2000 rpm for 30 sec, baking: 3 min at 160°C • EBL writing: 20 kV, 60 µm aperture 	Dot diameters: 2 µm – 200 nm, the distance between the dots has to match with the width of the bottom electrodes → adjust the EBL design

		<ul style="list-style-type: none"> developing: 30 sec in MIBK:IPA (1:3), rinse with IPA and blow dry with nitrogen gun 	For decreased dot diameters a smaller aperture should be used
3	Evaporation of Pd (#film144)	NL-CLR-Balzers BAK 600 <ul style="list-style-type: none"> 150 nm Pd (no rotation) Voltage: 10 kV Emission Current: see MIS logbook Base pressure: $< 1.0 \cdot 10^{-6}$ mbar Deposition rate 0.1 – 0.2 nm/s 	Pd is evaporated with water-cooled substrate holder to minimize stress in the structures
4	Lithography- Lift-off (#litho144)	NL-CLR-WB11 Use beaker and small sample holder <ul style="list-style-type: none"> Beaker 1: Acetone (no sonication!) > 2 min Beaker 2: Isopropanol VLSI > 2min 	
5	Substrate drying (#dry120)	NL-CLR-WB Single substrate drying: Use the nitrogen gun (fragile, small samples)	
Spin-coating of P3HT			
1	UV/Ozone (#surf100)	NL-CLR-UV PRS 100 reactor <ul style="list-style-type: none"> Time = 600 s rinse for 2 min with VLSI ethanol to remove possible oxide on the metal surface 	Cleaning of bottom electrodes prior to spin-coating of P3HT
2	Coating of P3HT	NL-CLR-WB23 (polymers) <ul style="list-style-type: none"> 500 - 6000 rpm for 60 sec, baking: 3 min at 160°C annealing: 60 min at 100°C clean spin-coater 	
3	RIE of polymers - standard (#etch109)	NL-CLR-Tetske Dirty chamber + Styros electrode <ul style="list-style-type: none"> Electrode temp.: 10°C O₂ flow: 20 sccm pressure: 10 mTorr power: 30 W 	Shadow mask to protect the patterned areas; P3HT is only removed at the upper part of the sample to enable a hydrophilic area required for wedging transfer Time: depending on the P3HT thickness
Wedging transfer and Pillar etching			
1	UV/Ozone (#surf100)	NL-CLR-UV PRS 100 reactor patterns for wet-chemical etching. <ul style="list-style-type: none"> Time = 600 s 	necessary for rendering the SiO ₂ substrate of the EBL (Pd) dots hydrophilic; otherwise the dots will not lift-off from the substrate
2	Wedging transfer	<ul style="list-style-type: none"> cellulose acetate butyrate (CAB) in ethyl acetate at a concentration of 30 mg/ml stirring for ~30 min dip-coat the substrates with the Pd dots into the cellulose and let it dry for a minute; remove the cellulose at the edges of the substrate to allow the water to penetrate between the hydrophobic transfer polymer and hydrophilic substrate lift-off of the cellulose with the Pd dots in Milli-Q water and transfer onto P3HT-coated bottom electrodes 	NE fumehood in MnF lab

		<ul style="list-style-type: none"> • dry overnight at ambient conditions • remove cellulose in ethyl acetate for 5 min, blow dry with nitrogen gun 	
3	RIE of polymers - standard (#etch109)	NL-CLR-TEtske Dirty chamber + Styros electrode <ul style="list-style-type: none"> • Electrode temp.: 10°C • O₂ flow: 20 sccm • pressure: 100 mTorr • power: 10 W 	Time: depending on the P3HT thickness > check with optical microscope
Patterning of gate oxide, gate oxide and deposition of large contact pads for electrical characterization			
1	Atomic layer deposition (ALD)	Loadlock Picosun <ul style="list-style-type: none"> • process temperature: 100°C • precursor materials: trimethylaluminum Al(CH₃)₃ (TMA) and water • Al₂O₃ thickness: 20 nm 	Always prepare also samples with a full layer of ALD-Al ₂ O ₃ , they are later required for the SIMS detector during RIBE
2	Evaporation of Al (#film127)	NL-CLR-Balzers BAK600 <ul style="list-style-type: none"> • 50 nm Al • Voltage: 10 kV • Emission current: see MIS logbook • Base pressure: < 1.0*10⁻⁶ mbar • Deposition rate: 0.1 – 0.2 nm/s 	Always prepare also samples with a full layer of ALD-Al ₂ O ₃ -Al, they are later required for the SIMS detector during RIBE
3	Dehydration bake (#litho001)	NL-CLR-WB21/22 Dehydration bake at hotplate <ul style="list-style-type: none"> • Temp.: 120°C • Time: 5min 	
4	Coating of Olin OiR 907-17 (#litho101)	NL-CLR-WB21 Coating: Primus spinner <ul style="list-style-type: none"> • coating: HMDS: 4000 rpm, 30 sec • coating: Olin OiR 907-17: 4000 rpm, 30 sec Prebake: hotplate <ul style="list-style-type: none"> • Time: 90 sec • Temp.: 95 °C 	
5	Alignment & exposure of Olin OiR 907-17 (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner <ul style="list-style-type: none"> • Hg-lamp: 12 mW/cm² • Exposure time: 4sec 	Mask: gate electrodes
6	Development of Olin OiR resists (#litho200)	NL-CLR-WB21 After exposure bake : hotplate <ul style="list-style-type: none"> • Temperature: 120°C • Time: 60sec Development: OPD4262 <ul style="list-style-type: none"> • 60 sec for developing of the photoresist • leave the sample in OPD4262 until the Al is completely etched (can be seen by eye) 	
7	Rinse with DI water	NL-CLR-WB	
8	Substrate drying	NL-CLR-WB use nitrogen gun	

9	Remove Olin OiR 907-17	NL-CLR-WB11 Use ultrasonic bath Use beaker and small sample holder • Beaker 1: Acetone > 10 min • Beaker 2: Isopropanol VLSI > 10min	
10	HSQ spin-coating	NL-CLR-WB23 (polymers) HSQ is stored in the fridge • 1000 RPM • baking for 3 min at 120°C	
11	DRIE of HSQ (#etch157)	NL-CLR- AdixenDE Layer thickness: 160 nm SH Temp: -10°C - Pos: 120 mm Flows: CHF ₃ : 60 sccm – O ₂ : 10 sccm - He: 150 sccm Pressure: 8 10 ⁻³ mbar Source G. W.: 200 W SH Gen W.: 100 W Etch rate of HSQ: ~70nm/min	Check by AFM if the top contacts are opened up
12	Chamber clean Adixen DE (#etch201)	NL-CLR-AdixenDE Chamber clean to remove fluorocarbon NEEDED after every 20 min processing SH Temp: any- Pos.: 150mm - He pres.: 10 mbar Flow O ₂ : 200 sccm APC: 100% / Pressure: 1.5 10 ⁻² - 6.0*10 ^{-6.5} mbar ICP: 2000 Watt CCP: 50 Watt (RF) Clean with a plain Si wafer in the etch tool Cleaning time: 30 minutes	
13	RIBE etching Oxford i300 (#etch299)	NL-CLR-Oxford RIBE i300 Motor Platen drive: 5 rpm Platen position: 0° Cooling Cool gas: 5 Torr Platen temperature: 15 °C (active cooling) Neutralizer Ar flow: 5 sccm Current: 100 mA RF generator Power: 300 Watt Beam Ar flow: 5 sccm O ₂ flow: 10 sccm Current: 50 mA Voltage: 300 Volt Accelerator: 300 Volt	>the Al and ADL-Al ₂ O ₃ on top of the dots is removed by RIBE to open up the dots >Place a dummy sample next to the real sample to enhance the SIMS signal >check with conductive-probe AFM if the dots are open
14	HSQ spin-coating	NL-CLR-WB23 (polymers) HSQ is stored in the fridge • 1000 RPM • baking for 3 min at 120°C	

15	DRIE of HSQ (#etch157)	NL-CLR- AdixenDE Layer thickness: 160 nm SH Temp: -10°C - Pos: 120 mm Flows: CHF ₃ : 60 sccm – O ₂ : 10 sccm - He: 150 sccm Pressure: 8 10 ⁻³ mbar Source G. W.: 200 W SH Gen W.: 100 W Etch rate of HSQ: ~70nm/min	Check by AFM if the top contacts are opened up
16	Chamber clean Adixen DE (#etch201)	NL-CLR-AdixenDE Chamber clean to remove fluorocarbon NEEDED after every 20 min processing SH Temp: any- Pos: 150mm - He pres: 10 mbar Flow O ₂ : 200 sccm APC: 100% / Pressure: 1.5 10 ⁻² -6.0*10 ^{-6.5} mbar ICP: 2000 Watt CCP: 50 Watt (RF) Clean with a plain Si wafer in the etch tool Cleaning time: 30 minutes	
17	Evaporation of Ti (#film144)	NL-CLR-Balzers BAK 600 • 2 nm Ti (no rotation) • Voltage: 10 kV • Emission Current: see mis logbook • Base pressure: < 1e-6 mBar • Deposition rate: 0.01 nm/s max. thickness: 500nm	Emission current was first ramped up to ~40 mA and then ramped down to ~32 mA; this enables a very low deposition rate
18	Evaporation of Pd (#film144)	NL-CLR-Balzers BAK 600 • 100 nm Pd (no rotation) • Voltage: 10 kV • Emission Current: see mis logbook • Base pressure: < 1e-6 mBar • Density 19.3 g/cm ³ • Deposition rate 0.1 – 0.2 nm/s max. thickness: 500nm	
19	Coating of Olin OiR 907-17 (#litho101)	NL-CLR-WB21 Coating: Primus spinner • Coating: HMDS, 4000rpm, 30sec • Coating: Olin OiR 907-17, 4000rpm, 30sec Prebake: hotplate • Time: 90 sec • Temp.: 95 °C	
20	Alignment & exposure of Olin OiR 907-17 (#litho301)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ² • Exposure time: 4sec	Mask: top contacts
21	Development of Olin OiR resists (#litho200)	NL-CLR-WB21 After exposure bake : hotplate • Temperature: 120°C • Time: 60sec Development: OPD4262 • 60 sec for developing of the photoresist	

22	Rinse with DI water	NL-CLR-WB	
23	Substrate drying	NL-CLR-WB use nitrogen gun	
24	RIBE etching Oxford i300 (#etch299)	NL-CLR-Oxford RIBE i300 Motor Platen drive: 5 rpm Platen position: 0° Cooling Cool gas: 5 Torr Platen temperature: 15 °C (active cooling) Neutralizer Ar flow: 5 sccm Current: 100 mA RF generator Power: 300 Watt Beam Ar flow: 5 sccm O2 flow: 10 sccm Current: 50 mA Voltage: 300 Volt Accelerator: 300 Volt	Etching until Ti peak disappears

Figure 1. (a) Mask for photolithography for two-terminal devices and gated pillar devices; (b) zoom-in on one junction (black: bottom electrode; red: gate electrode; purple: top contact).

Appendix 4: Process flow for nanogaps by edge lithography

	Process		Comments
	Substrate	Wafer 100 mm, P-type, <111>, OSP, 525 µm thickness, 5 – 10 Ohm cm resistivity
1	Cleaning ozone/steam (UCL) (#clean142)	NL-CLR-WB12 Application of organic and inorganic contamination for UCL applications (metal free). Standard program: is 5 cleaning cycles, this suffices to remove also 1.7 µm olin Oir resist. 1 rinse cycle consists of 3 subcycles of 1 min ozone/steam followed by 5s DI spray. Afterwards the reactor is filled one time with DI and subsequently dumped; a clean reactor free of gasses is obtained after each cycle. parameters: • time: 45 min • temp. reactor 95 °C. • temp. demiwater 80 °C	
2	Dry Oxidation of Silicon (UCL) (#film175)	NL-CLR-Tempress-furnace A2 Standby temperature: 700°C • Temp range.: 800 up to 1100°C • Gas: O ₂ • Flow: 4l/min • Ramp: 10°C/min • Cooldown: 7.5 °C/min • Standard programs: UCL-2 950 °C (time variable) UCL-1 1100 °C (time variable) Thickness: 10 nm	Recipe: ISFET900, 10min, includes a cleaning step before oxidation
3	Dehydration bake (#lith102)	NL-CLR-WB21/22 dehydration bake at hotplate • temp. 120°C • time: 5min	Continue immediately with the priming step!
4	Coating Olin Oir 907-17 (#lith105)	NL-CLR-WB21 Coating: Primus spinner • coating: HMDS, 4000 rpm, 30 sec • coating: Olin Oir 907-17, 4000 rpm, 30sec Prebake: hotplate • time 90 sec • temp 95 °C
5	Alignment & Exposure Olin Oir 907-17 (#lith121)	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ² • Exposure Time: 4sec	Mask 1: Etching (inverse)
6	Development Olin Oir resist (#lith111)	NL-CLR-WB21 After exposure Bake : hotplate • time 60sec • temp 120°C development: developer: OPD4262 • time: 30sec in beaker 1 • time: 15-30sec in beaker 2

7	Quick Dump Rinse (QDR) (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
8	Substrate drying (#clean120)	NL-CLR-WB Single wafer dryer • speed: 2500 rpm, 60 sec with 30 sec N ₂ flow	
9	Postbake Olin OiR resist (#lith109)	NL-CLR-WB21 postbake: Hotplate • temp 120°C • time 10min	
10	Inspection by optical microscope (#metro101)	NL-CLR- Nikon Microscope • dedicated microscope for lithography inspection	
11	SiO₂ etching in 1% HF	Etch rate: 4 nm/min Time: 2:30 min (depending on SiO ₂ thickness)
12	Quick Dump Rinse (QDR) (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
13	Substrate drying (#clean120)	NL-CLR-WB Single wafer dryer • speed: 2500 rpm, 60 sec with 30 sec N ₂ flow	
14	Lithography - Lift-off procedure for metals (#Lith144)	NL-CLR- Wet-Bench 11 Use ultrasonic bath 1 Use metal beaker and wafer holder • Beaker 1: Acetone VLSI , >10 min • Beaker 2: Isopropanol VLSI > 10min • Spin drying
15	Quick Dump Rinse (QDR) (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
16	Substrate drying (#clean120)	NL-CLR-WB Single wafer dryer • speed: 2500 rpm, 60 sec with 30 sec N ₂ flow	
17	Si etching in TMAH (25%, 70°C)	Etch rate: 25 nm/min Time: 3 min (time depends on the required etch depth)
18	Quick Dump Rinse (QDR) (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec	

		2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 Ω M	
19	Substrate drying (#clean120)	NL-CLR-WB Single wafer dryer • speed: 2500 rpm, 60 sec with 30 sec N ₂ flow	
20	1% HF etch of SiO₂	etch rate: 4 nm/min etch time: ~5 min; to remove the SiO ₂ mask
21	Quick Dump Rinse (QDR) (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 Ω M	
22	Substrate drying (#clean120)	NL-CLR-WB Single wafer dryer • speed: 2500 rpm, 60 sec with 30 sec N ₂ flow	
23	Cleaning ozone/steam (UCL) (#clean142)	NL-CLR-WB12 parameters: • time: 45 min • temp. reactor 95 °C. • temp. demiwater 80 °C	
24	Dry Oxidation of Silicon (UCL) (#film175)	NL-CLR-Tempress-furnace A2 Standby temperature: 700°C • Temp range.: 800 up to 1100°C • Gas: O ₂ • Flow: 4l/min • Ramp: 10°C/min • Cooldown: 7.5 °C/min • Standard programs: UCL-2 950 °C (time variable) UCL-1 1100 °C (time variable) Thickness: ~20 nm	Recipe: ISFET950, 10 min (check logbook)
25	Coating Ti 35 ES	NL-CLR-WB21 Coating: Primus spinner • HMDS 4000 rpm • Ti 35 ES • spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate • time 120 sec • temp 95 °C	
26	Alignment & Exposure Ti35ES	NL-CLR- EV620 Electronic Vision Group EV620 Mask Aligner • Hg-lamp: 12 mW/cm ² • Exposure Time: 18 sec • roomtemp., >30 min • Electronic Vision Group EV620 Mask Aligner (Hg-lamp: 12 mW/cm ²); Exposure Time: 60 sec Flood exposure should be carried out without a mask in the maskaligner	Mask 2: Contact pads

27	Development Olin OiR resist (#lith111)	NL-CLR-WB21 After exposure Bake : hotplate • time 60sec • temp 120°C development: developer: OPD 4262 • time: 20 sec in beaker 1 • time: 20 sec in beaker 2	
28	Quick Dump Rinse (QDR) (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 Ω M	
29	Substrate drying (#clean120)	NL-CLR-WB Single wafer dryer • speed: 2500 rpm, 60 sec with 30 sec N ₂ flow	
30	Inspection by optical microscope (#metro101)	NL-CLR- Nikon Microscope • dedicated microscope for lithography inspection	
31	Evaporation of Ti/Au (#fim144)	NL-CLR-Balzers BAK 600 • 2 nm Ti • Au (thickness depending on required nanogap-size) • Voltage: 10 kV • Emission Current: see MIS logbook • Base pressure: < 1.0*10 ⁻⁶ mbar • Deposition rate 1-10 A/s	
32	Lithography - Lift-off procedure for metals (#Lith144)	NL-CLR- Wet-Bench 11 Use ultrasonic bath 1 Use metal beaker and wafer holder • Beaker 1: Aceton VLSI , >10 min • Beaker 2: Isopropanol VLSI > 10min	
33	Quick Dump Rinse (QDR) (#clean119)	NL-CLR-Wet benches Recipe 1 QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec Recipe 2 cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 Ω M	
34	Substrate drying (#clean120)	NL-CLR-WB Single wafer dryer • speed: 2500 rpm, 60 sec with 30 sec N ₂ flow	
35	Inspection by optical microscope (#metro101)	NL-CLR- Nikon Microscope • dedicated microscope for lithography inspection

Figure 2. (a) Mask for photolithography for a chip of 11x11 mm² (purple: mask for etching; green: mask for metal electrodes); (b) zoom-in on electrodes with different widths.

Summary and Outlook

The implementation of organic building blocks into nanoelectronics devices is finding increased interest due to the huge potential for low-cost, large-area, flexible electronics. In Chapters 4 to 6 the fabrication and characterization of vertical hybrid inorganic-organic nanoelectronics devices was covered. For top-contacting of self-assembled monolayers (SAMs) of *n*-alkanethiols and thin films of the organic semiconductor poly(3-hexylthiophene) (P3HT) the water-based technique called wedging transfer was utilized.

In Chapter 4, large-area, symmetric metal-molecular monolayer-metal junctions were investigated as a proof-of-concept for the soft top-contacting method. SAMs were formed on ultrasmooth bottom electrodes. To our knowledge this was the first time that a floating method was shown to work on metal/metal contacts, while previous molecular junctions with soft-landed top electrodes were only reported on Si or oxidized Al as bottom contacts. This contacting method enables the fabrication of symmetric, large-area molecular junctions, with a relatively high yield and allows for statistically relevant numbers of electrical measurements to be obtained in a practical manner. An exponential dependence of the current density was observed as a function of the monolayer thickness with a decay coefficient β of $0.72 \pm 0.09 \text{ nm}^{-1}$ determined at 1 V in accordance with β values reported in literature (from 0.51 to 1.16, with the majority between 0.73 and 1.11).

Following up on this work, two-terminal sub- μm sized vertical metal-P3HT-metal pillar structures were fabricated, described in Chapter 5. Organic thin films (5 nm to 100 nm) were deposited by spin-coating onto pre-defined bottom electrodes and top-contacted by wedging transfer. The transferred top-contacts were subsequently used as a shadow mask for the underlying P3HT during directional dry etching. Junctions with different P3HT thicknesses and pillar diameters were electrically characterized at room temperature and low temperatures (295 K to 150 K). The devices were characterized by a very good electrical reproducibility over several consecutive voltage sweeps and over a time window of 21 days. Experimental and modelled data for P3HT thicknesses of 100

nm and 40 nm were in excellent accordance. The higher calculated current densities for 10 nm and 5 nm of P3HT might be attributed to a different chain orientation of the P3HT film in close vicinity to the metal electrodes. The devices were characterized by a low injection barrier which is very beneficial for new types of thin film devices.

In Chapter 6, we describe the fabrication of vertical organic field-effect transistors. The two-terminal devices described in Chapter 5 were thereby embedded in a conformal oxide layer grown by atomic layer deposition functioning as the gate oxide. Subsequently, a side-gate was evaporated around the whole pillar structure. Electrical investigation of the vertical organic field-effect transistors did not yet reveal a gate effect. A possible explanation for this observation might be that the gate electrode was too far away from the pillar structure and/or the applied gate bias was not high enough to have a strong electric field from the gate electrode to tune the conductance of the organic semiconductor. It is recommended to evaporate the gate material under an angle and under rotation in order to form the metal layer closer to the vertical pillar structures and to increase the ratio between the channel length and the thickness of the gate-oxide for achieving a stronger electric field to tune the conductive channel of the organic film. The ability to tune the conductive channel of an organic semiconductor with a side-gate would open up a new design of OFET structures. The possibility to sandwich extremely thin organic layers between source and drain electrodes enables confinement in the vertical dimension. A nanoscale diameter of the pillar structure in combination with an applied side gate provides the possibility to also achieve confinement in the lateral dimension. Following this route, the fabrication of vertical organic semiconductor quantum dots might be possible with few-electron, few-hole conduction.

The fabrication technique for large-area molecular junctions as well as vertical pillar structures with and without a gate electrode can be extended to investigate other organic materials. Interesting SAMs to study are for example ferrocene molecules which are known to exhibit switching behavior. P3HT is a *p*-type organic semiconductor, highly conductive *n*-type organic materials could be characterized with our devices. Beside the organic active layer also the electrode materials can be relative straightforwardly exchanged with our device design. The

metal could be replaced by superconductive or ferromagnetic materials allowing for a wide variety of interesting experiments.

Chapter 7 discusses the fabrication of nanogaps by edge lithography for trapping of DNA molecules over these vertical gaps. Undercuts were wet etched into Si onto which subsequently metal electrodes were evaporated. The metal evaporation is highly tunable and consequently also the size of the nanogap in the sub-10 nm regime. The end goal of these devices will be the electrical detection of hypermethylated DNA (hmDNA) which occurs in cancer cell and is utilized as a marker for early stage cancer detection. However, before investigating hmDNA the proof-of-principle of the devices has to be tested. Therefore, the metal electrodes were functionalized with streptavidin molecules and biotin-tagged DNA was trapped over the nanogaps due to the streptavidin-biotin interaction. DNA molecules are not conductive, therefore we metallized the DNA for electrical characterization. The conductivity increased after metallization of the DNA while there was no conductance for junctions without DNA which were exposed to the same metallization conditions. These were very preliminary results on trapping and electrical detecting DNA over the nanogaps and before being able to reliably detect hmDNA, a better control over unspecific metallization is required. Next to trapping of DNA the nanogaps could furthermore be utilized for fabrication molecular junctions by binding SAMs in between the nanogaps. The Si substrate could thereby be utilized as a gate electrode enabling a transistor device.

In Chapter 8, the fabrication of ordered high-density arrays of sub-15 nm silicon nanocrystals with a combination of nanolithography and wet etching is described. Combining corner lithography with directional deposition methods could offer the possibility for individually contacting silicon nanocrystals on wafer-scale which may find application in new optical sensing and computing applications. We furthermore achieve nanochannels by combining displacement Talbot lithography and KOH etching and thereby achieving doubled V-grooves. The structures were subsequently covered with a conformal Al_2O_3 layer by atomic layer deposition to further shorten the openings and the channel helping to realize achievable confinement in those channels. These nanochannels can in near future be filled up with molecules and thereby provide the possibility of one-dimensional molecular transport through these channels.

Samenvatting

Organische halfgeleiders en moleculen worden in toenemende mate geïntroduceerd in nanoelektronische devices omdat zij het mogelijk maken om goedkope, flexibele elektronica op grote schaal te produceren. In de hoofdstukken 4 tot en met 6 wordt de fabricage en karakterisering van verticale, hybride anorganisch-organische, nanoelektronische devices behandeld. Voor het top-contacteren van zelf-geassembleerde monolagen (SAMs) van *n*-alkaanthiolen en dunne lagen van de organische halfgeleider poly(3-hexylthiophene) (P3HT) wordt de op water gebaseerde “wedging transfer”-methode gebruikt.

In hoofdstuk 4 worden symmetrische metaal-moleculaire monolaag-metaaljunctions met een groot oppervlak onderzocht als proof-of-concept voor de techniek om zacht-gelände topelektrodes te maken. Hiervoor werden SAMs gegroeid op ultra-gladde bodemelektrodes. Voor zover ons bekend is dit de eerste keer dat een “floating”-methode met succes op metaal/metaal contacten is gebruikt, eerder werk maakt alleen melding van moleculaire junctions met zacht-gelände topelektrodes op bodemelektrodes van Si of geëxideerd Al. De gebruikte methode maakt de fabricage van symmetrische moleculaire junctions over grote oppervlakken mogelijk met een relatief hoge opbrengst van werkende devices, waardoor er op een praktische manier een statistisch representatieve hoeveelheid metingen kan worden gedaan. De stroomdichtheid vertoonde een exponentiële afhankelijkheid van de monolaagdikte met een dempingscoëfficiënt β van 0.72 ± 0.09 n_c^{-1} gemeten bij 1 V. Deze waarde komt overeen met waardes gerapporteerd in de literatuur (van 0.51 tot 1.16 waarbij de meerderheid tussen 0.73 en 1.11 ligt).

Vervolgens is deze methode aangepast voor de fabricage van tweepolige, sub- μm , verticale metaal-P3HT-metaal pilaarstructuren, welke in hoofdstuk 5 worden beschreven. Dunne lagen organisch materiaal (5 tot 100 nm) worden gespincoat op bodemelektrodes en de topelektrodes zijn wederom aangebracht middels wedging transfer. De organische laag wordt gestructureerd middels directioneel droog etsen waarbij de topelektrodes als schaduwmasker worden gebruikt. Junctions met verschillende P3HT-diktes en pilaardiameters zijn elektrisch gemeten bij kamertemperatuur en bij lage temperatuur (295 K tot 150 K). De

devices vertonen zeer goed reproduceerbare elektrische eigenschappen, zowel tussen meerdere direct opeenvolgende metingen, als over een periode van 21 dagen. Experimentele en gemodelleerde data van 100 nm en 40 nm dikke P3HT-lagen komen uitstekend met elkaar overeen. De hogere berekende stroomdichtheden voor devices met 10 nm en 5 nm P3HT-dikte zijn waarschijnlijk het gevolg van veranderingen in de oriëntatie van ketens in de P3HT-film vlakbij de metaalelektrodes. De devices vertonen een lage injectiebarrière, een groot voordeel voor toepassing in nieuwe types van devices met dunne lagen.

In hoofdstuk 6 wordt de ontwikkeling van verticale, organische veldeffecttransistoren beschreven. De in hoofdstuk 5 behandelde devices worden daarbij middels atoomlaagdepositie omgeven door een conforme oxidelaag, die als gate-oxide fungeert. In de volgende processtap wordt een side-gate elektrode opgedampt rondom het pilaarvormige device. Bij elektrische karakterisering werd echter geen gate-effect waargenomen. Mogelijk is de afstand tussen de gate-elektrode en de pilaar te groot en/of het aangelegde elektrisch veld van de gate-elektrode niet hoog genoeg om de geleiding in de organische halfgeleider te beïnvloeden. Het is aan te raden om het gate-materiaal onder een hoek en terwijl het sample roteert op te dampen, zodat het metaal dicht bij het verticale device terecht kan komen. Verder kan de verhouding tussen de lengte van het geleidingskanaal en de dikte van de gate-oxide vergroot worden om een sterker elektrisch veld te kunnen aanleggen. De mogelijkheid om het geleidingskanaal van een organische halfgeleider te beïnvloeden met een side-gate zal een nieuw design van OFETs mogelijk maken. Het kunnen “sandwichen” van een extreem dunne, organische laag tussen twee elektrodes zal in de toekomst “confinement” in de verticale dimensie mogelijk maken. Als de diameter van de pilaarvormige devices in de orde van nanometers is, kan door gebruik van een side-gate ook “confinement” in de laterale dimensie worden gerealiseerd. Dit kan leiden tot de ontwikkeling van verticale, organische halfgeleider kwantumdots, die werken met de geleiding van slechts enkele elektronen of gaten.

De fabricage van moleculaire juncties op grote oppervlakken, en verticale pilaarstructuren met en zonder gate-elektrode kan verder worden uitgebreid door het gebruik andere materialen. Interessante SAMs zijn bijvoorbeeld ferroceenmoleculen, waarvan bekend is dat ze schakelgedrag vertonen. Het

gebruikte P3HT is een *p*-type organische halfgeleider, maar zeer goed geleidende *n*-type organische materialen zouden ook met ons device-design kunnen worden onderzocht. Naast het organische actieve materiaal is het ook relatief eenvoudig om het elektrode materiaal te variëren. Het metaal kan worden vervangen door bijvoorbeeld een supergeleidend of ferromagnetisch materiaal; dit zou zeer interessante experimenten toelaten.

Hoofdstuk 7 behandelt de fabricage van zogeheten nanogaps middels “edge”-lithografie met als doel het binden van DNA-moleculen aan deze verticale openingen. “Undercuts” worden in Si geëtst waarna metalen elektrodes worden opgedampt. Door de hoge nauwkeurigheid waarmee het metaal gedeponereerd wordt is de grootte van de nanogaps, zelfs in het bereik onder de 10 nm, goed controleerbaar. Het einddoel van deze devices is het elektrisch detecteren van hyper gemethyleerd DNA (hm-DNA), dat in kankercellen voorkomt en voor de vroege detectie van kanker kan worden gebruikt. Voordat we hm-DNA analyseren, hebben we eerst proof-of-principle tests van deze devices uitgevoerd. Hiervoor worden metaalelektrodes gefunctionaliseerd met streptavidinmoleculen waarna biotin-tagged DNA wordt gevangen over de nanogaps door de interactie tussen streptavidin en biotin. Omdat DNA-moleculen niet elektrisch geleidend zijn, hebben we het DNA gemetalliseerd alvorens elektrische metingen uit te voeren. Na metallisering nam de geleiding toe op devices met DNA, terwijl devices met nanogaps zonder DNA na hetzelfde proces geen geleiding vertonen. Dit zijn zeer voorbarige resultaten van DNA-binding en -detectie met behulp van nanogaps, en voordat er betrouwbaar hm-DNA gedetecteerd kan worden moet eerst de controle over specifieke metallisatie verbeterd worden. Behalve voor de detectie van DNA kunnen de nanogaps ook worden gebruikt voor de fabricage van moleculaire juncties door SAMs aan te brengen in de nanogaps. Het Si substraat kan hierbij worden gebruikt als gate-elektrode voor het ontwikkelen van een transistordevice.

In hoofdstuk 8 wordt de fabricage van “ordered high-density arrays” van sub-15 nm siliciumnanokristallen door een combinatie van nanolithografie en nat etsen beschreven. Door corner-lithografie en directionele opdampmethoden te combineren ontstaat de mogelijkheid om op oppervlakken ter grootte van een gehele wafer individuele nanokristallen te contacteren. Deze techniek zou bijvoorbeeld kunnen worden toegepast in diverse optische systemen. Verder

hebben we nanokanalen gemaakt met behulp van displacement-Talbotlithografie en KOH-etsen waardoor dubbele V-groeven ontstaan. De structuren zijn vervolgens, door middel van atoomlaagdepositie, bedekt met een conforme laag aluminiumoxide waardoor de openingen van de nanokanalen kleiner worden en er “confinement” in de kanalen mogelijk is. In de toekomst kunnen deze kanalen gevuld worden met moleculen en gebruikt worden voor eendimensionaal transport.

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