Embedding Electromagnetic Band Gap Structures in Printed Circuit Boards for Electromagnetic Interference Reduction

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by

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EMBEDDING ELECTROMAGNETIC BAND GAP
STRUCTURES IN PRINTED CIRCUIT BOARDS FOR
ELECTROMAGNETIC INTERFERENCE REDUCTION

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Summary

Due to the tendency of faster data rates and lower power supply voltage in the integrated circuit (IC) design, Simultaneously Switching Noise (SSN) and ground bounce become serious concerns for designers and testers. This noise can be a source of electromagnetic interference (EMI). It propagates through the power/ground planes on the printed circuit board (PCB) and it can couple to the nearby circuit affecting the performance of other devices. This noise results in antenna currents into connected cables and it can also increase the edge radiation from the PCB. In mixed signal systems it leads to sensitivity degradation or radio-frequency (RF) interference issues of radio-frequency circuits. This research work is focused on how to mitigate noise and reduce EMI by means of structuring the power plane of a PCB with Electromagnetic Band Gap (EBG) structures. A novel concept for ultra-wide-bandwidth suppression of SSN is proposed and implemented. This method consists of applying EBG cells with different stop bands creating noise isolation over a wide frequency region. The thesis starts with a general description of Power Distribution Network (PDN) of a PCB. It discusses the main challenges modern PCB designers are facing. Power and ground planes which are symmetric in shape and size create a resonating waveguide structure, an ideal path for SSN propagation. The mechanism of noise generation and propagation through the PDN and general approach of PDN noise reduction is discussed. Typically used methods include placement of EMI passives such as decoupling capacitors and ferrite beads and via stitching. The drawback of these methods is the limited frequency bandwidth they can cover, and the need to integrate additional components. Reduction of SSN noise by means of EBG was intensively studied over the last decades. However, most of the structures are effective only in a limited frequency band. Often they are embedded in a PCB as a separate layer or require extra vias which increase the manufacturing cost. In this work a new type of planar EBG structures was proposed as a means to avoid the generation and propagation of common-mode currents due to SSN in the power plane of PCBs, and thereby reducing their radiated emissions. The EBG also have beneficial effects on the differential-mode noise in PDN due to the SSN. To guide the design of EBGs for SSN reduction, several modelling techniques of the EBG structures based on results achieved with full-wave electromagnetic simulations by means of CST Microwave Studio and transmission matrix analysis are used. The dispersion diagram of the

proposed EBG structure is validated by insertion loss measurements of the prototype boards. It was shown that a power plane structure is needed only locally for circuitry decoupling by creating a low impedance current path. The effect of different PDN designs such as power plane, power track and 2 single-cell EBG structures and different sized cells EBG on the noise reduction in PCB with active components was investigated. Some high permittivity materials were implemented as a PCB substrate to create a large power-ground plane capacitance, and its effectiveness to reduce EMI was investigated.

Many researchers have investigated the effect of EBG using passive elements only. In this thesis not only the passive elements behaviour is discussed, but a design with active components was used too. The reduction in radiated electromagnetic fields and common mode currents of PCB with active components and various PDNs was studied. An equivalent circuit of active boards with a PDN was created with a SPICE circuit simulator. The proposed new EBG structure behaves as a wideband low pass filter reducing EMI. The key result of the work presented in this thesis is that by applying EBG structured power plane and supporting each individual electronic module on the board by its own power patch interconnected by - relatively- thin traces, instead of standard power ground plane couples which are identical and parallel to each other, can reduce SSN, common mode noise and radiated emission of the PCB.

Samenvatting

Door de steeds hogere datasnelheden, met frequentie componenten in het gigahertz gebied en de trend van afnemende voedingsspanningen in het ontwerp van geïntegreerde circuits (IC), zijn Simultaneous Switching Noise (SSN) en ground bounce ernstige problemen geworden voor ontwerpers en testers. Deze ruis kan een bron van elektromagnetische interferentie (EMI) zijn. De ruis geeft aanleiding tot impulsvormige stroompieken -transienten- in het voedingsnet op de print dat traditioneel bestaat uit voedings- en referentie vlakken. De velden behorend bij deze transienten kunnen dan koppelen met nabijgelegen circuits en de werking van andere componenten beïnvloeden. Deze ruis kan verder leiden tot antennestromen in aangesloten bekabeling en mogelijk tevens in een toename van velden vanuit de spleetantenne gevormd door voedingsvlak en referentievlak aan de rand van de printplaat resulteren. In PCB's met zowel analoge als digitale circuits kan het leiden tot afname van de gevoeligheid of radiofrequente (RF) interferentieproblemen in RF circuits. Dit onderzoek is gericht op reductie van voornoemde storingsproblemen en het verminderen ervan door middel van de structurering van het voedingsvlak van de printplaat met zogenaamde Electromagnetic Band Gap (EBG) structuren. Een nieuw concept voor onderdrukking van SSN wordt voorgesteld en toegepast. Deze methode bestaat uit aanbrengen van een aantal EBG structuren met verschillende stopbanden waardoor ruisonderdrukking over een breed frequentiegebied wordt bereikt. Het proefschrift begint met een algemene beschrijving van het voedingsdistributienetwerk van een printplaat. De belangrijkste uitdagingen voor huidige printplaatontwerpers worden besproken. Voeding- en referentievlakken zijn over het algemeen symmetrisch gevormd en creëren een resonante golfgeleiderstructuur; een ideaal pad voor de geleiding van SSN. We bespreken het vormingsmechanisme en de propagatie van ruis door het PDN en tevens de gangbare methodes voor onderdrukking van PDN ruis. Typische methodes bestaan uit de plaatsing van passieve EMI componenten zoals ontkoppel capaciteiten, ferrietkralen en extra printplaatdoorvoeren ("vias"). Het nadeel van deze methodes is de gelimiteerde frequentieband waarin ze werkzaam zijn en de noodzaak om additionele componenten te integreren in de printplaat. Vermindering van SSN ruis door middel van de toepassing van EBG structuren is uitvoerig bestudeerd in de laatste jaren. Echter, ook hiervoor geldt dat de meeste structuren alleen in een beperkt frequentiegebied effectief de SSN ruis onderdrukken. Vaak zijn

deze structuren geïntegreerd in de printplaat als een aparte laag, of vereisen het gebruik van extra vias waardoor de fabricagekosten toenemen. In dit werk wordt een nieuw type vlakke EBG structuur voorgesteld ter voorkoming van de common mode stroom door de, in eerste instantie differential mode SSN in het voedingscircuit van printplaten, in feite een reductie van de transfer-impedantie, waardoor de resulterende emissie afneemt. Voor het ontwerp van EBGs voor SSN onderdrukking zijn verscheidene modelleringstechnieken toegepast welke gebaseerd zijn op ‘full-wave’ elektromagnetische simulaties met het programma CST Microwave Studio en transmissiematrix analyse methodieken. De berekende dispersiediagrammen van de voorgestelde EBG structuur wordt gevalideerd door middel van insertion loss metingen op prototype printplaten. We tonen aan dat een voedingsvlakstructuur alleen lokaal noodzakelijk is om circuits te ontkoppelen door de vorming van een laag-impedant geleidingspad naar de capaciteit die de voedingsspanning binnen tolerantie moet houden. Het effect van verschillende PDN ontwerpen, zoals power plane, power track en 2 ééncellige EBG structuren en een EBG met verschillende celgroottes, op ruisonderdrukking in een printplaat met active componenten is bestudeerd. Enkele materialen met hoge permitiviteit zijn geïmplementeerd als printplaatsubstraat om een hogere voedingsvlakcapaciteit te realiseren en de invloed hiervan op onderdrukking van EMI is bestudeerd. Verscheidene onderzoekers hebben het effect van de toepassing van EBGs bestudeerd met gebruik van enkel passieve componenten. In dit proefschrift wordt niet alleen het gedrag met passieve elementen behandeld, maar wordt ook een ontwerp met actieve componenten bestudeerd. De afname van het uitgestraalde elektromagnetische veld en de common mode stroom van de printplaat met actieve componenten en verschillende PDN implementaties zijn onderzocht. Van deze printontwerpen is een SPICE simulatie opgezet die resultaten geeft die goed overeenkomen met de metingen. De nieuwe hier voorgestelde EBG structuur gedraagt zich als een laagdoorlaatfilter en vermindert EMI. Het belangrijkste resultaat van het hier gepresenteerde werk is dat de toepassing van een EBG-gestructureerd voedingsvlak en het gebruik van individuele power patches voor elke elektronische module op de printplaat welke doorverbonden zijn door – relatief – dunne sporen, een asymmetrische structuur, in plaats van een standaard voedings- en referentievlak combinatie die identiek en parallel (symmetrisch) aan elkaar zijn; de SSN, common mode ruis en uitgestraalde emissie van de printplaat kunnen verminderen

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1. Introduction

The realization of the first integrated circuit (IC) or chip, see Figure 1-1, by Jack Kilby at Texas Instruments in the summer of 1958 (awarded the physics Nobel prize in 2000) is a milestone event that marks the beginning of a new electronic era. Today, the huge technological progress since these early days is reflected in an abundance of electronic devices in a wide range of appliances: ICs can be found everywhere, e.g. in cars, television sets, computers and cellular phones, but also in planes and space ships. Essentially, this progress is enabled by our technological ability to create ever smaller structures in semiconductors, resulting in a higher density of components and increased functionality in electronic devices. This trend was recognized already in 1965 by Gordon Moore who stated that the number of components that could be incorporated per integrated circuit would increase exponentially over time [1]. Indeed, since 1970 the number of components per chip has doubled every two years; this trend has become known as “Moore’s Law” and still drives the semiconductor industry today.

Figure 1-1 (a) Jack Kilby’s first IC, (b) Kilby’s IC (enlarged), (c) Kilby inspecting a modern wafer carrying a multitude of chips. Figures adapted from [2] and [3]

1.1 The need for electromagnetically compatible devices

In our modern lives we are using more and more electronic devices and we take it for granted that they function properly in any given situation. However, being electrical in nature, these devices are both sources of electromagnetic energy as well as are susceptible to incoming electromagnetic energy. Since these devices often operate in close proximity to each other and often in closed environments, they can easily interfere with each other. To prevent such unwanted electromagnetic interference (EMI), each apparatus before entering the market has to be tested for meeting so called Electromagnetic Compatibility (EMC) standards. EMC is the ability of a system to operate in its environment without disturbing anything else in that environment, including itself.

A system is said to be electromagnetically compatible if [4]:

1. It does not cause interference with other systems in its electromagnetic environment;
2. It is not susceptible to emissions from other systems in its electromagnetic environment, and
3. It does not cause interference with itself.

Equipment can radiate itself or be susceptible to radiation. Three components are required for coupling of electromagnetic energy: source, coupling path and victim. There are four groups of electromagnetic interference phenomena: radiated emissions, radiated susceptibility, conducted emissions and conducted susceptibility. The term radiated is used for the propagation of electromagnetic waves through the air, while the term conducted is used for propagation through a physical medium such as a cable between two systems. Emission means to produce electromagnetic waves and propagate them either through the air (radiate) or through a physical medium such as a cable (conduct). Susceptibility is a sensitivity to electromagnetic waves received through the air (radiated) or through a cable (conducted).

No electrical product or installation can be designed seriously unless all aspects of EMC are properly taken into account. In general, it is cheaper to control EMC in the early stages of product design rather than awaiting results after conformance testing and then fixing EMC issues in the design. As there are many forms and consequences of EMI, EMC covers a very broad range of phenomena. For illustration, several striking examples of the possible effects of electromagnetic interference are provided here:

- An electric wheelchair moving on its own when a police officer in a nearby cruiser keyed the radio set [5];
- The lightning stroke causes many TVs to fail;
- Cash register in the supermarket blocking auto-lock system of the cars parked nearby on a parking lot [6];
- The compasses of an airliner going haywire while climbing past 9,000 feet when a passenger in row 9 was using an Apple Inc. iPhone [7];
- According to NASA, during test performed in 2004, a now-discontinued Samsung Electronics Co. wireless phone model's signal was powerful enough to block out global-positioning satellites [8];
- Blackberry wireless e-mail device having electrostatic discharge (ESD) problems shutting off in cold weather;
- A fire aboard the aircraft carrier USS Forrestal in 1967 killing 134 people due to an accidental rocket firing after a radar beam triggered an electronic malfunction [9].

The amount of such accidents is endless, every year similar issues appear in the press, and every new generation of engineers will be faced with EMC challenges with each new product and within each new installation.

1.2 The research project

The motivation for this research activity is the increasing cost of passive components that are needed to prevent EMC, with respect to the cost of the whole product. The aim of the work is to reduce the amount of these passives by applying novel materials and/or techniques in the realm of Electromagnetic Bandgap (EBG) Structures, to form low-pass filters by reshaping the power distribution conductors.

Traditionally passive devices such as decoupling capacitors are used to counteract EMI. Each of them has to be placed close to the IC, turning the Printed Circuit Board (PCB) into a network of capacitors. For example, the Nokia 6161 cellphone has 15 integrated circuits and 232 capacitors, 149 resistors and 24 inductors. These 405 passive components determine the area of the circuit, the size and the price of the product [10]. In some products the cost for passive EMI components and their placement can reach 73% of the total cost and this number is increasing rapidly. The sources of EMI mostly are currents flowing in electronic circuits mounted on PCBs. Some of the energy conveyed in these moving charges can be radiated directly away from the PCB (radiated emission) or conducted away via coupling pathways (conducted emission). For example, radiated emission can result from signal and return paths carrying the interference current and acting as a loop antenna, or can result from discontinuities in the PCB's transmission line structures, e.g. at the edges of the substrate which effectively act as a patch antenna [11], [12]. The interference current can be generated as Common-Mode (CM) from ground noise developed across the PCB or elsewhere in the equipment. An inappropriately designed power distribution network can serve as a coupling path for CM-current leaking into the connecting cables and thereby forming a source of emission. The fast signal rise times of digital logic circuits implying fast current surges in the devices' power supply lines contribute to increasing EMI. If many outputs are switched simultaneously, such as in a synchronous system, these transient currents flow in the power distribution network, causing voltage drops due to the finite impedance of the power and ground planes. At high frequencies the power-ground planes start to resonate leading to large impedances in the power distribution network which leads to voltage fluctuations towards the connected devices. This phenomenon is also known as Simultaneous Switching Noise (SSN), causing Signal Integrity (SI) and Power Integrity (PI) problems. The noise developed in the reference or ground plane results also in antenna currents in connected cables leading to EMI. This thesis is mainly focused on noise reduction in the Power Distribution Network (PDN) in PCBs with the objective to reduce radiated EMI. A typical PDN architecture, the noise generation and noise propagation in it, and the existing approach of reducing it, are discussed in more detail in Chapter 2.

The solution direction pursued in this thesis was inspired by recent research into a new class of materials known as "metamaterials". Metamaterials are artificially engineered (repeating) structures which are made out of several materials. Metamaterials have emerging physical properties that can strongly differ from the

individual constituent materials but that in fact stem from their exactly designed structures. For example, meta-materials can prohibit the propagation of electromagnetic waves within a particular frequency band, such as EBG structures. Other examples are (magnetic) metamaterials which could be used for extremely high-frequency power conversion, and so-called "left-handed" or "negative index" materials, which can be used for novel focusing properties at high frequencies, i.e. on-board antenna, or absorption [13]. Given that meta-materials can be used to engineer electromagnetic characteristics that are not to be found in natural materials, such novel structures may be helpful for devising new solutions to counter EMI. Chapter 3 proposes application of these meta-materials as novel EMC measures by embedding them in PCB substrates, replacing partly today's mounted passives. The EBG structures, a particular class of metamaterials, are described and analysed. The influence of EBG structures on resonance reduction in PDNs is studied. Finally, to guide the design of EBGs for SSN reduction, in Section 3.3 several modelling techniques of the EBG structures were introduced. These techniques are based on results achieved with full-wave electromagnetic simulations by means of CST Microwave Studio, and ABCD matrix analysis. Later in the thesis also distributed circuit elements will be used.

Chapter 4 investigates the influence of the layout and amount of EBG cells on its filtering behavior. Several design strategies of EBG structures with broader suppression band as developed by many researchers are proposed in this thesis.

Chapter 5 shows implementation of EBG structures in PDN of active PCB. Four active boards are built and measured to investigate the effect of the geometry of the PDN on the common mode noise generated by the board into its environment. The effect of the power plane, power track and EBG structures on the noise reduction in printed circuit boards with active components is investigated. Some experimental measurements of longitudinal noise voltage and radiated emission are also demonstrated in this chapter.

Electrical circuit analysis of an active board on two single-cell EBG is performed in Chapter 6. In the time-domain, adequate power integrity (PI) is demonstrated before common-mode (CM) analyses can be reasonably made. The CM simulation is performed in the time- and frequency-domain. Chapter 7 describes materials and shows combinations of EBGs and embedded capacitance material and its effect on noise. Finally, in Chapter 8 conclusions and recommendations for future research are given.

2. Noise generation in a power distribution network

In this chapter the mechanism of noise generation in a power distribution network (PDN) is described. Section 2.1 describes the typical PDN. In Section 2.2 challenges to the traditional PDN are discussed. In Section 2.3 an impact of the noise in a PDN is addressed. Finally, in Section 2.4 an overview of solutions to reduce noise in a PDN is given.

2.1 Traditional PDNs on a PCB

The active components on a PCB need a source of power (actually energy) with a voltage within close tolerances to operate. However, power supply units are often large and far removed from the power and ground terminals of individual ICs and other components on the board. For this reason, a suitable power distribution network (PDN) needs to be designed into PCBs. The main task of the PDN is to provide a stable and reliable constant voltage to the active devices on the board. Throughout the PCB, power is traditionally distributed using metal plates (power and ground planes) separated by a dielectric. Fast edge rates in the supply currents generate noise on the supply voltage, the amount depending on the impedance of the PDN. This impedance depends mainly on the geometry of the conductors, as well as on the PCB dielectric thickness and material properties. Dielectric material, also called substrate, is characterized by a dielectric constant (ϵ_r). This is the dielectric permittivity of a substrate relative to ϵ_0 , the dielectric permittivity of empty space, calculated using Equation (1) :

$$\epsilon_r = \frac{\epsilon}{\epsilon_0} \quad (1)$$

Where ϵ_r is dimensionless, ϵ_0 in [F/m], multiplied giving ϵ the total dielectric permittivity [F/m] of the material.

The relative dielectric constant relates the effect of an insulator on the capacitance of a conductor pair, to the capacitance of the conductor pair in vacuum. The dielectric constant affects the impedance of a transmission line: a high value of ϵ_r reduces this impedance and signals can propagate slower in materials that have a high ϵ_r . In a transmission line, like the power-ground plane combination in the PDN, the velocity

of propagation v of the electromagnetic energy is related to the dielectric constant of the substrate material with Equation (2) and is equal to:

$$v = \frac{c}{\sqrt{\epsilon_r \mu_r}} \text{ [m/s]} \quad (2)$$

where c is the speed of light in a vacuum (free space) $c=3 \cdot 10^8$ m/s and ϵ_r is the relative dielectric permittivity and μ_r is magnetic permeability of the medium through which the wave is propagating. Typically epoxy-glass material FR 4 is used as a dielectric for PCB substrates [14]. If we want to move charge on an interconnection on an FR 4 epoxy-glass board, then we can calculate an effective decoupling radius r using Equation (3):

$$r = vt = \frac{3 \cdot 10^8 \cdot t}{\sqrt{\epsilon_r \mu_r}} \text{ [m]} \quad (3)$$

Where t is time required to move charge in seconds. This actually means that for fast switching electronic circuits, the effective decoupling radius becomes small. In other words, then the energy needed to achieve a constant, or stable, voltage, can be supplied only from a short distance.

Only a small fraction of the power supply voltage is typically permitted as a ripple voltage; the active device's specification provides a voltage tolerance, typically in the order of 5% of the nominal voltage. The IC supply voltage(s) must stay within this tolerance at all times. Supply current transients can be shorter than a few hundred ps in modern high-speed digital systems and with falling supply voltages, the transient currents have a tendency to increase. And thus 5% of the voltage is a smaller number. For this reason, the impedance of the PDN should be kept as low as possible by design and an adequate amount of charge should be stored close enough to the IC supply pins, within the effective decoupling radius to prevent the voltage fluctuation from exceeding the tolerance. This is achieved by using power-ground plane combinations plus a network of storage capacitors at strategic (i.e. close enough) locations within the decoupling radius.

The inevitable connections between the storage capacitors and the IC supply pins should have the least possible inductance. In some situations, the required storage can be distributed over several capacitors that are effectively in parallel. That way, the total supply inductance seen by the IC is reduced. A power-ground plane combination is an ideal capacitor in that respect. The disadvantage is the value of that capacitor is too small within the effective decoupling radius with regular FR4 dielectrics and extra discrete capacitors are needed which can be achieved by using

high capacitance materials as PCB substrate. This is discussed in Chapter 7. Once adequate supply buffering is accomplished, the remaining noise voltage at the IC supply and the capacitors may spread over the rest of the PDN as conducted emissions. As a preventive measure an inductance, sometimes in the form of physical inductors and other necessary enhancements as local voltage converters, can be inserted to decouple this local noise source from the rest of the circuitry, thereby increasing the complexity of the PDN. In modern PCBs, the PDN interconnects a multitude of components. Figure 2-1 shows an example of such a PDN. The system power supply provides the required current at a relatively high voltage to the board. This voltage is then reduced through Voltage Regulator Modules (VRM) and supplied via interconnecting traces to the ICs. A network of decoupling capacitors is placed at various levels of the board (on-die, on-package, on the motherboard and around the VRM) and act as reservoirs of charge. Failure in delivering a voltage within tolerances results in loss of reliability and performance of the product and hence additional costs. In the next section the challenges which traditional PDN are facing are described.

Figure 2-1 PDN topology adapted from [15]

2.2 Challenges to traditional PDN concepts

Several trends in electronic circuitry design are challenging the performance of traditional power distribution networks. According to the International Roadmap on Semiconductors (IRS) [16], electronic devices will continue to become smaller; functionality and portability will increase. Integrated circuits will contain a large number of transistors: multi-terminal switches that can be turned ‘on’ or ‘off’ on the basis of an electrical control signal. The trend predicted by IRS is that the switching speed of these transistors will continue to rise, that they will operate on lower voltages and that they will dissipate less power. Figure 2-2 illustrates this expected supply voltage and power range of high performance transistors. As transistors become faster and smaller and ICs offer more advanced functionality, designers can push for smaller devices and this ultimately results in an increased density of passive and active components on PCBs.

Figure 2-2 (a) Supply voltage scaling (V_{dd}) of Logic High Performance Transistors
(b) Dynamic power scaling (CV^2) of Logic High Performance Transistors [16]

Another trend is the increasing use of so-called mixed signal systems, where digital and analog ICs are placed together on one board. High-amplitude signals are propagating through the board from digital circuits and these can affect the performance of sensitive analogue, often radio-frequency ICs and neighbouring circuits. The mechanism of noise generation and propagation in PDN, and the

conventional approach to reduce it, is the subject of Section 2.3 and 2.4 of this chapter.

2.3 Ground bounce and SSN

In traditional designs the power and ground planes are identical in shape and size. This eases the design of the power distribution towards devices, and it is commonly assumed to create a low impedance due to the capacitance between power and ground plane. But, except where special thin, high permittivity materials are used, the capacitance provided by the board itself is hardly enough to keep the IC voltages within tolerance and additional discrete capacitors must be added to achieve that goal. Another disadvantage is that a wide power plane parallel to a wide reference (ground) plane forms a symmetric transmission line. In [17] it is shown that a symmetric transmission line has a high transfer impedance as compared to a thin trace over a wide plane. The fast signal rise times of digital logic circuits imply fast current surges in the devices' power supply lines. If these currents are allowed to flow over a PDN with high transfer-impedance, these differential-mode (DM) noise currents will give rise to a relatively large amount of common-mode (CM) noise current that will flow over any wires or conductors connected to the PCB and possibly be emitted from them as radiated fields. If many outputs of transistors are switched simultaneously, such as in a synchronous system, these transient currents in the PDN are increased, causing voltage drops due to the finite impedance of the power and ground planes [18] in addition to possible ground-bounce on the ICs output lines [17 pp. 67-74]. Parallel ground planes also represent an unterminated waveguide which starts to resonate at high frequencies, where the PDN shows large impedances which lead to voltage fluctuations towards the connected devices or edge-radiation. This phenomenon is also known as simultaneous switching noise (SSN) or ground bounce [19] [20] [21]. SSN is related to the inductance present in a loop of the device ground and the system ground, and the amount of current sunk by each output. It can be calculated using Equation (4):

$$V_{SSN} = L_{eff} \cdot di / dt \quad (4)$$

di/dt is the time rate of change in transient current driving e.g. a capacitive load, L_{eff} is the (net partial) inductance of the electrical path from the ground/power IC pads to the package terminals defined by Equation (5)

$$L_{eff} = L_{bondwire} + L_{board} + L_{int} \quad (5)$$

L_{eff} is a sum of inductance of the via, chip interconnect (wire bonds and bonds pads) and the board inductance.

Inductive coupling of conductors and inductance of the power or ground path and amount of simultaneously switching outputs contribute to SSN. SSN increases Signal Integrity (SI) and Power Integrity (PI) problems, one of the biggest issues for designers. It can lead to loss of stored data, severe speed degradation, output glitches, and reduction in system-noise immunity [22]. Uncontrolled noise spikes reduce noise margins of the gate causing false switching of quiet gates. As mentioned, this noise results also in antenna currents in connected cables and radiation from the edge of the board leading to EMI. In all conditions, the design of a reliable noise free power delivery network becomes very important.

2.4 Methods to reduce SSN

SSN problems in terms of PI may be reduced by designing the PDN such that its impedance towards the active devices is below a specific target impedance. This involves computational optimization of the number and types of decoupling capacitors with optimum values of associated capacitance with low equivalent series inductance (ESL) [23] [24]. Such solutions are often not perfect because the current path between the capacitors and the device may result in parasitic inductance much higher than the ESL. On the other hand, ineffective decoupling of these storage capacitors with respect to the remaining PDN leads to excessive power bus noise as well as to excessive radiated emission, because the decoupling network itself acts as a series resonant circuit. So the use of discrete capacitors is not efficient at switching frequencies higher than a few hundred MHz [25], [26].

Another strategy to reduce the noise is to control resonances of the PDN by resistive edge termination of the PCB [27, 28] or by selecting the location of the via ports in a manner that eliminates certain resonances [29], or employing ferrite beads [30]. Segmentation of the power plane into power islands was also used to decrease ground bounce [31, 32] by using the higher impedance of the traces. In [24] it was proposed to etch a trench around the noise source and thus to create an island and to connect it to the rest of the board via inductors. This technique, however, suffers from the limitations imposed by the dominant lead inductance of the capacitors. Another approach is board zoning or board floor planning which implies location of components on the PCB to separate zones according to their functions. Another approach to reduce resonances is to employ EBG structures [33-38]. In order to

reduce SSN, EBG can be introduced as a separate layer between power and ground plane. Generally, EBGs are periodic structures consisting of dielectric and conductive material which in combination limit the propagation of electromagnetic waves in specific frequency bands. An overview of the existing EBG structures is given in Chapter 3. EBGs are divided into mushroom type EBG and planar EBG that vary in design and manufacturing process. They can be realized by implying micromachining holes or vias into dielectric slabs to create the two-dimensional (2-D) or three-dimensional (3-D) periodic variations of materials, often called “mushroom-like” EBG, or to be etched as periodic structure patterns on the ground or power plane or the signal strip of the microstrip line, the so called “planar” EBG [34, 35, 39, 40]. The suppression of resonances in power and ground planes by application of EBGs has been studied previously [40]. The combination of EBG structures and embedded capacitive material [37] or inductive material [41] can lead to the miniaturization of the EBG structure and improves its performance. To realize mushroom type EBG structures, three layers in a PCB are required which increases manufacturing cost. In general, EBG structures are periodic, and thus only effective in a small frequency band. The novel application of EBG structures as low-pass filters to decouple the DM noise sources, i.e. IC’s with storage capacitors, from the rest of the PDN, and thus to reduce the development of high-frequency CM noise, is the subject of the remaining parts of this thesis.

2.5 Summary

Several techniques are commonly used to reduce noise in power distribution networks. One of them is already more than 50 years old and it is adding EMI passives [42]. For low frequency noise larger electrolytic capacitors are used, for high frequency noise commonly surface mount ceramic capacitors connected directly to the power supply pins of the IC are required. This solution is time consuming because it requires preliminary calculations and considerations about number and values of these capacitors. Moreover, due to parasitic effects the decoupling network turns into a series resonant circuit. Capacitors must be placed as close to the IC as possible otherwise the inductance of the connecting trace will have a negative impact on the effectiveness of the decoupling, which means the placement of EMI passives should be considered during design stage. Ferrite beads are also used for decoupling at low frequencies (<100 kHz), above 100 kHz ferrites becomes resistive. Some ferrites, even before full saturation occurs, can be nonlinear

and therefore should be checked in a prototype if it is operating near this saturation region [43]. Because of increased cost of EMI passives a new approach to decoupling is suggested. It was proposed to use EBG structures to reduced radiated emission of PCB caused by power plane resonances. In some design the EBG structure has to be implemented as a separate layer, in some it contains vias or interconnecting traces in different shapes [44-47]. The main disadvantage is complexity and manufacturing cost and limited bandwidth of EBG structures. The approach followed in this thesis is to use the power plane as a wide-band EBG, instead of adding additional PCB layers.

3. EBG structures in the power distribution network

In this chapter the concept of Electromagnetic Band Gap (EBG) structures and their use in power distributions networks is analyzed. EBG structures are a particular application of the novel field of ‘metamaterials’: artificially engineered materials whose physical characteristics emerge from their microstructural design and which can be markedly different from the properties of the individual constituents [48]. In Section 3.1 a general introduction to metamaterials is given. The possibilities to use EBG structures as a means to avoid the generation of common-mode currents due to SSN in the power plane of PCBs and thereby reducing their radiated emissions are investigated. As such, the EBGs also have beneficial effects on the differential-mode noise in PDN due to the SSN. In Section 3.2 the mechanism of how noise propagation can be attenuated in an EBG-structured power plane is discussed. In the same section further study on usage of EBG structures for the reduction of resonances in the power distribution system of a printed circuit board is provided. Finally, to guide the design of EBGs for SSN reduction, in Section 3.3 several modelling techniques of the EBG structures based on results obtained from full-wave electromagnetic simulations by means of CST Microwave Studio are introduced. Section 3.5 describes the transmission (*ABCD*) matrix analysis of EBG structures in details.

3.1 Metamaterials

The atomic structure of a given material determines its physical properties. For example, metal reflects light since its constituent atoms have the ability to share their (outer) electrons; these ‘free electrons’ interact (shield) with incoming light, effectively resulting in the reflection of a particular spectrum of incoming light. Metamaterials are artificially engineered materials, which are composed of periodic or non-periodic arrangements of designed structures made from different materials. These structures can be considered to be formed of artificial “atoms” or “particles”, with sub-wavelength dimensions (smaller than the wavelength of the waves they affect). As a result, metamaterials get their properties not just because of the properties of ingredient materials, but especially from the combination of size, shape, design, and feasible arrangement of single artificial “particles” forming the metamaterial. This approach provides engineers with freedom to tailor metamaterial properties, both electric and magnetic and control the material characteristics as

desired. Metamaterials can have uncommon physical (e.g. electromagnetic, photonic) properties not readily available in nature. For instance, they can affect waves of light (electromagnetic radiation) or sound in an unconventional manner, creating material properties which are unachievable without these specially engineered geometric structures. For reference, Figure 3-1 demonstrates several examples of metamaterials, highlighting their typical build up being the (periodic) arrangement of particular structural units [49].

Figure 3-1 (a) Three-dimensional photonic crystal [50],
 (b) Negative index metamaterial array configuration [51],
 (c) Left-handed metamaterial [52], [53]

The theoretical basis for the creation of metamaterials with artificially engineered characteristics was developed already in the late 1960s by Victor Veselago [54]. Veselago proposed that materials theoretically can reverse their refractive index. He predicted the possibility of the creation of materials with negative values of their effective magnetic permeability (μ) and electric permittivity (ϵ). Still, it took several decades until the first practical realization of this theory when the Split Ring Resonator (SRR) particle was proposed [55] and only in 2000 the first metamaterials exhibiting simultaneously negative ϵ and μ were realized [53], [56]. In the late 1980s it was proposed to use photonic crystals (periodic sub-wavelength arrangements of materials with strongly differing refractive indices) due to their frequency selective properties to increase a laser's efficiency by inhibiting propagation of non-coherent radiation. Later on, photonic crystal channelized waveguides and resonators were designed which gave possibility to the large scale integration of optical based systems instead of conventional electronic semiconductor devices. Throughout the 1990s and the first decade of the 21st century, research was focused on downscaling

of the frequency of operation to the microwave and millimeter wave band, which made it possible to use metamaterials for different applications such as antennas, passive components, increased power amplifier efficiency, etc. [57].

3.2 EBG

The ability to engineer metamaterials' properties also spurred interest in their use for electronic applications. The aim of this thesis is to use specific metamaterials with electromagnetic properties to counter EMI in electronic devices. The drawback of metamaterials is that they often operate only in a particular limited wavelength range for which they are precisely designed and manufactured. Some metamaterials have to be designed with nanoscale accuracy to maintain their unique properties, which leads to extra costs. Hence, it would be a challenge to transfer most of the metamaterials into mass production and implement them in PCBs. An exception to this is a class of metamaterials called EBG structures. They consist of patterns of conductive materials laid down on a dielectric substrate. EBG structures are attractive since they are built using materials and processes commonly used for PCB manufacturing. This suggests that EBG-based EMI solutions may be compatible with PCB techniques and may allow for an economically viable approach. Through a suitable design, EBGs can prohibit the propagation of electromagnetic waves in a specific frequency range. The first EBGs, inspired by the creation of high impedance surfaces [58], were called mushroom type EBG.

They consist of three conductive layers. The top layer represents a power plane VDD, the bottom layer is a ground plane GND, and the layer in between is periodically etched into patches with through-vias to the ground plane, see Figure 3-2b. Initially these mushroom EBGs were used for antenna applications. Later, mushroom EBG design approaches were employed for noise isolation in digital systems [44]. To realize mushroom type EBG structures three layers are required which increase manufacturing cost. The size of an individual unit cell of EBG is also very small and limited by the desired frequency band suppression. Hence, they were adapted to another type of EBG structures. Planar EBGs, that consist of 2 conductive layers with dielectric sandwiched in between. Only one of the layers is periodically patterned into patches and interconnecting bridges and another one is usually kept solid for return currents. Figure 3-2 demonstrates an example of mushroom and planar EBG structures.

Figure 3-2 (a) Planar EBG, (b) Mushroom EBG

3.3 Planar, periodically patterned, EBG

It is easier and cheaper to manufacture planar EBG than mushroom type just using standard processes. Figure 3-2 demonstrates a general example of a 2 dimensional planar EBG structure described in [45] which is formed by capacitive patches of 10×10 mm connected via interconnecting traces of 1×1 mm. This board was created on a fiber glass epoxy (FR4) substrate with $\epsilon_r = 4.5$. The power and ground plane of this board are 109 mm by 54 mm in size. The copper thickness for power plane and ground plane is 0.036 mm and dielectric thickness is 0.11 mm. In this example, the EBG structure is etched on the power plane. Port 1 is located at $(38$ mm, 27 mm) and port 2 is located at $(82$ mm, 27 mm) with the origin $(0, 0)$ lying at the bottom left corner of the rectangle, as shown in Figure 3-3.

To describe the response of an N-port network to voltage signals at each port commonly scattering parameters or *S*-parameters are used. “Scattering parameters,” are a parameter set that relates to the traveling waves that are scattered or reflected when a n-port network is inserted into a transmission line. Let us consider a network with only two ports, an input port and an output port, like the network shown in Figure 3-3. Note: All the boards used in this thesis are listed in Appendix B.

Figure 3-3 Board 1. Example of a 2 dimensional planar EBG power plane on 109x54 mm PCB

Figure 3-4 General two-port network

The S -parameters (scattering parameters) of a network provide a clear physical interpretation of the transmission and reflection performance of the device. The S -parameters for a two-port network are defined using the reflected or emanating waves, b_1 and b_2 , as the dependent variables, and the incident waves, a_1 and a_2 , as the independent variables. The general equations for these waves as a function of the S -parameters is shown below:

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned} \quad (6)$$

The incident voltage at each port is denoted by " a ", while the voltage leaving a port is denoted by " b ". The first number in the subscript refers to the responding port, while the second number refers to the incident port. Thus S_{21} means the response at port 2 due to a signal at port 1. Using these equations, the individual S -parameters can be determined by taking the ratio of the reflected or transmitted wave to the incident wave with a perfect termination placed at the output [59].

The transmission coefficient S_{21} between two ports of Board 1 was simulated using CST Microwave Studio and plotted on **Error! Reference source not found.**

Figure 3-5 Transmission coefficient S_{21} of Board 1

This EBG patterned power plane was designed to suppress the coupling between two ports on the PCB, port 1 located at (27;38), would be suppressed when observing at port 2, which is located at (27;82). These observations are valid for 50 Ω systems, as the simulations are using a reference impedance of 50 Ω . It is designed as a stopband of this EBG structure. The disadvantage of this structure is limited suppression band and complexity in implementation in a real product.

The variation of the patches' shape and size, and perturbations of interconnecting traces (bridge lines) resulted in a myriad of EBG types with different suppression bands [60] [61] [62]. The typical electromagnetic behavior of various periodically patterned EBG types is that they create a network of capacitive and inductive elements by the repetition of many equal, even symmetric shapes, having the same resonances which act as a narrow band stop filter. All the patches have the same resonant frequency. In order to increase the bandwidth of EBG cascading two or more EBG structures with different unit cell periods that have different stopbands was proposed [63, 64]-[65]. The drawback of these designs is the cost and manufacturing complexity because several power/ground plane areas are occupied

to cascade different stop-band EBG. In this section the new two single cell EBG structure was proposed, it was etched on the power plane capable to reduce noise over a large frequency band. In Chapter 4 the new concept of EBG with different cell sizes is proposed and its effect on EMI reduction is studied.

The aim of this research project is to create an EBG structure effective in a broader frequency range, performing as a low pass filter. In the next section the fundamental mechanisms that govern the EBG's electromagnetic behavior is investigated in more details. Therefore the behavior of basic cell structures has been investigated.

3.4 Effect of two single-cell EBG structures on PDN resonances

PCB power and ground planes conventionally consist of large metal planes separated by a dielectric. Usually the power plane mirrors the ground plane and creates a transmission line sandwich which behaves as an electromagnetic resonant cavity. The dimensions of the planes can be multiples of the wavelength λ in the medium, and the thickness of the dielectric is much smaller than λ . At low frequencies, power and ground plane behave capacitive and at higher frequencies they show inductive behavior. Since the planar dimensions are multiples of λ , they behave as spatially distributed systems resonating at higher frequencies due to the reflections from the open edges. These resonances are called standing wave resonances [66]. The resonances in this structure are associated with an undesirable drop of impedance. If a logic gate switches, a current transient occurs in the power distribution system. This current flows through the power and ground plane and creates a noise voltage across the impedance of the plane causing noise voltages in the ground plane. This noise voltage creates common mode current emission either by direct radiation from the board or by coupling to connected cables. In addition, a transient current flowing around the loop formed by power and ground planes makes an efficient loop antenna. The frequency of the power plane resonance is determined by its physical size and dielectric constant of the insulator. Figure 3-6 shows an example of a standard PDN formed by a power and a ground plane, denoted Board 2, and its resonance behavior. It was designed on an EURO-card PCB ($100 \times 160 \text{ mm}^2$). The power plane ($50 \times 150 \text{ mm}^2$) and the ground plane ($100 \times 160 \text{ mm}^2$) are solid planes parallel to each other. Two SMA connectors were connected to the board. Their location is shown in Figure 3-6.

Figure 3-6 Board 2 standard power plane

Figure 3-7 Transmission coefficient S_{21} of Board 2, standard PDN

The transmission coefficient S_{21} of the board has been measured between port 2 and port 1 using a Vector Network Analyser (VNA) in the frequency range 10 MHz – 3

GHz and is plotted in Figure 3-7. There are several methods proposed to calculate the impedance matrix of unloaded power /ground plane structures [66], [67], [68]. The planes resonate at discrete frequencies when the length or width is a multiple of $\lambda/4$ and $\lambda/2$. For our design the input impedance of port 1 can be defined as

$$Z_{in} = Z_0 \left[\frac{Z_L + jZ_0 \tan \beta b}{Z_0 + jZ_L \tan \beta b} \right] \quad (7)$$

Z_L is the load impedance $= \infty$, because the far end is open, $\beta = 2\pi/\lambda$ is phase constant where $\lambda = v/f$, v is velocity of propagation, and f is the frequency. $a = 50$ mm is the length, $b = 150$ mm is the width of the plane. Substituting $b = \lambda/4$ in Equation (7) input impedance is $Z_{in} = 0$ at $f = 0.23$ GHz, which correspond to the resonance frequency. If $b = \lambda/2$, $Z_{in} = \infty$, then the anti-resonance frequency is at $f = 0.47$ GHz. If $a = \lambda/4$, $Z_{in} = 0$ then the resonance frequency is at $f = 0.7$ GHz. For $a = \lambda/2$; $Z_{in} = \infty$ at $f = 1.41$ GHz as anti-resonance frequency. The anti-resonance frequency for every excitation mode can be calculated using Equation (8) and it is listed in Table 3-1 :

Table 3-1 Calculations of resonances of Board 2

$f_{r,p}$ [GHz]	k	m
0.47	0	1
0.94	0	2
1.41	0	3
1.41	1	0
2.83	2	0
4.24	3	0
1.49	1	1
1.70	1	2
2.00	1	3
2.87	2	1
2.98	2	2
3.16	2	3
4.27	3	1
4.35	3	2

$$(f_r)_{km} = \frac{1}{2\pi\sqrt{\mu_0\epsilon_r\epsilon_0}} \sqrt{\left(\frac{k\pi}{a}\right)^2 + \left(\frac{m\pi}{b}\right)^2}, [\text{Hz}] \quad (8)$$

k, m are the mode numbers, ϵ_r relative dielectric permittivity, ϵ_0 vacuum permittivity, μ_0 vacuum permeability.

High impedances of the PDNs results in and increase of the PDN noise. As can be seen in Figure 3-7, the board resonates and its resonance frequency is determined by the mode number, dielectric constant of the insulator and physical size of the planes. Another source of PDN resonances are interactions of low loss inductances with low loss capacitances. The most troublesome interactions are usually the parasitic bonding wire inductances towards the integrated circuit (IC) die capacitance and the parasitic inductances to the PCB [69]. If the transistors in a device are switching then instantaneous energy, or actually charge, is needed to drive the circuitry. As described in Chapter 2, due to the finite velocity of propagation the charge can only be used when located within a finite radius from the devices being supplied, and large planes are often not needed as PDN for a single device [17]-[70]. The effective capacitance where this approachable charge is stored, is only the capacitance of an area within a finite radius r of the IC being decoupled as demonstrated on the board in Figure 3-8. This area with finite radius is called effective decoupling radius.

Figure 3-8 Effective decoupling radius

As was discussed in Chapter 2, the effective decoupling radius r can be calculated using Equation (3). Charge stored outside of effective decoupling radius cannot be moved fast enough to arrive at the IC during the switching transient. The presence of the power plane area outside the effective decoupling radius does not serve the active device. Hence, it is possible to place every noisy module on a power patch of sufficient dimensions, and interconnect these power patches using transmission lines which are able to feed the current supply to charge the local capacitance again for the next switching action, which actually creates a pattern that resembles the EBG

structure as in Figure 3-3. A patch is as large as it has to be to carry the components (size wise) and if the capacitance is too low, discrete capacitance has to be added. Electromagnetic separation of modules on a Printed Circuit Board (PCB) and between the board as a whole and its environment is facilitated by removing the conducted interference path that traditionally exist between these modules if solid power planes are used in combination with a solid -uninterrupted- ground (reference) plane. As it was shown before, the disadvantage of power planes that are identical to a ground plane while running in parallel, is the inherent symmetry of this power transportation provision. Although the structure resembles a (small, distributed) capacitor, the two conductors behave as a resonant structure if either width, length or both approximate a quarter wavelength of the transported high frequency currents. A geometrically symmetric transmission line has a high transfer impedance (Z_T) and may consequently generate larger undesired common mode currents into the environment from differential mode currents on, in this case, the PDN [17]. The structure with the lowest Z_T is a trace over a ground plane [71]. This does not mean power planes can or should be completely abandoned and replaced by power traces. Power planes are needed locally for circuitry decoupling at frequencies over 500 MHz [11]. The compromise is to provide a high speed PCB with one, uninterrupted, ground plane and several local power “patches” as needed for the individual electronic modules on the board, interconnected by -relatively-thin traces. The effectiveness of this approach is the subject (and outcome) of the experiments described in this thesis.

To demonstrate this effect, 2 PCBs ($30 \times 95 \text{ mm}^2$) have been designed on FR 4 substrate with thickness 1.6 mm. This Board 3 has a layout of a conventional power plane (Figure 3-9a) with a power and ground plane equal in shape and size ($30 \times 95 \text{ mm}^2$). 2 SMA connectors were connected to the board as shown on Figure 3-9a. On Board 4 the basic structure of a two single-cell EBG, as shown in Figure 3-9b, was created. It consists of two patches with size $30 \times 30 \text{ mm}^2$ interconnected by a thin power trace of 35 mm long and 0.25 mm wide. Until the dimensions become a part of a wavelength, the trace can be considered as a small inductance, while the patches can be considered as capacitors. The transmission coefficient S_{21} of these boards has been measured using a vector network analyser in the frequency range 10 MHz – 3 GHz. Figure 3-10 shows the measured transmission coefficient S_{21} measured between the 2 ports located in the center of each patch.

Figure 3-9 (a) Board 3: Standard power plane, (b) Board 4: Two single-cell EBG

Figure 3-10 Transmission coefficient S_{21} of Board3 and Board4

The noise isolation between 2 ports is more than -20 dB over a large frequency band. Around 1.4 GHz the transmission coefficient of the standard PDN and two single-cell EBG is around -44 dB. The difference between the conventional power plane and the EBG power structure is approximately 30 dB in a large part of the frequency spectrum measured, and the proposed EBG reduces resonances in the PDN. The deep anti-resonance at 2.4 GHz is an anti-resonance of the whole structure, i.e. over the length, and that is why there is less difference between standard PDN and two single-cell EBG structure at this frequency.

3.5 Analysis of basic EBG cell

The proposed structure was simulated using the full wave simulator CST. The results of simulations are compared with measurement data and plotted on Figure 3-11. The simulated results are generally consistent with the experimental data. The anti-resonance at 2.4 GHz is shifted to a higher value. It is related to the frequency dependencies of the FR-4 material, which were neglected in the CST model and to the couplings outside the EBG structures, which were neglected in CST.

Figure 3-11 Simulation of transmission coefficient S_{21} versus measurements of Board4

To investigate the contribution of each part of the single cell structure on S_{21} each part of the structure was simulated separately and plotted on one graph. The left patch (Figure 3-12b) was excited in the center using a lumped port with 50 Ω port

impedance. Port 2 of the left patch was placed on the edge of the patch on the place of connection with the line. The thin power trace, Figure 3-12c, was simulated using a waveguide port and its impedance was normalized to 50Ω . The right patch (Figure 3-12d) was excited with 50Ω port on the left edge and port 2 was located in the center of the patch.

Figure 3-13 – Figure 3-17 demonstrate S and Z parameters obtained in CST. Z parameters, also called impedance parameters, can be obtained with S parameters using formulas described in [72]. The structure is passive and symmetrical so characteristics are reciprocal (S_{21} and S_{12} are equal). S_{21} of the total structure shows a dip at 2.4 GHz and at 4.8 GHz. At the frequency 2.08 GHz the Z_{11} of the line is very small and the phase is 90 degrees so the behavior of the line below 2 GHz is inductive and at 2.08 GHz the circuit resonates, the phase becomes -90° and the line shows capacitive behavior which gives an anti-resonance at 2.27 GHz.

Figure 3-12 (a) Two single-cell EBG structure, (b) left patch, (c) thin power trace, (d) right patch

The circuit also resonates at 4.5 GHz. The structure has low transmission around 4.3 - 5 GHz. There is a resonance in a middle of a second dip at 4.4 GHz and the next one is at 4.7 GHz. The whole structure is resonating around 4 - 5 GHz which is related to the physical resonance of the total structure and excitation of its 20 mode.

Figure 3-13 Reflection coefficient S_{11} of two single-cell EBG structure (Board 4)

Figure 3-14 Transmission coefficient S_{21} of two single-cell EBG structure (Board 4)

Figure 3-15Amplitude of Z_{11} of two single-cell EBG structure (Board 4)

Figure 3-16Phase of Z_{11} of two single-cell EBG structure (Board 4)

Figure 3-17 Amplitude of Z_{21} of two single-cell EBG structure (Board 4)

Using Equation (8) the resonance frequency of the patches for every excitation mode was calculated and these are listed in Table 3-2 .

Table 3-2 Calculations of resonances of the patch

$f_{r.p.}$ [GHz]	k	m
2.4	0	1
4.8	0	2
7.2	0	3
2.41	1	0
4.8	2	0
7.2	3	0
3.4	1	1
5.4	1	2
7.6	1	3
5.4	2	1
6.8	2	2
8.7	2	3
7.6	3	1
8.7	3	2
7.2	3	0

Analytical calculation of patch 01 mode resonance is around 2.4 GHz and 02 mode resonance is around 4.8 GHz which influence the total structure. This result is reflected also in the CST simulation.

As can be seen in Figure 3-13 - Figure 3-17, the structure has a notch at the frequency 2.09 GHz and 4.4 GHz due to the length of the interconnected line. This can be easily calculated from Equation (27) for the difference between peak frequencies.

$$k = \frac{2\pi}{\lambda} = \frac{2\pi}{\lambda_o \sqrt{\epsilon_r \mu_r}} \quad (9)$$

λ_o - free space wavelength, magnetic permeability $\mu_r = 1$

$$k^2 = k_x^2 + k_y^2 + k_z^2, Z_{\text{mode}}=0 \quad (10)$$

$$k_x = \frac{m\pi}{w} \quad (11)$$

$$k_y = \frac{n\pi}{l} \quad (12)$$

$$k_y = \frac{p\pi}{h} = 0 = \beta \quad (13)$$

$$k = \sqrt{k_x^2 + k_y^2} \quad (14)$$

$$k = \frac{1}{\sqrt{\epsilon_r \mu_r}} \sqrt{k_x^2 + k_y^2} = \frac{1}{\sqrt{\epsilon_r \mu_r}} \sqrt{\left(\frac{m\pi}{w}\right)^2 + \left(\frac{n\pi}{l}\right)^2} \quad (15)$$

Where n is refractive index defined with formula (16)

$$n = \sqrt{\epsilon_r \mu_r} \approx \sqrt{\epsilon_r} \quad (16)$$

$$\lambda = \frac{\lambda_o}{n} = \frac{\lambda_o}{\sqrt{\epsilon_r}} \quad (17)$$

$$\lambda_d = \frac{\lambda_o}{\sqrt{\epsilon_{\text{eff}}}} \quad (18)$$

$$e^{-j\beta z} = e^{-j\frac{2\pi}{\lambda_d} z} \quad (19)$$

Here $\beta_z = \Delta\phi$ is a difference in phases. Considering the peak corresponds to a frequency f_i with a wavelength $\lambda_i = \frac{c}{f}$ then the next frequency peak is equal

to $f_{i+1} = f_i + \Delta f$. At the peak frequency $\Delta f_{total} = i2\pi$. Over the length of the line the

$$\Delta f_L = \beta L = \frac{2\pi}{\lambda_{di}} L$$

$$\Delta f_{total} = 2\Delta f_L + 2\Delta f \quad (20)$$

$$\Delta f = (i+1)2\pi = 2(\Delta f_{L_i} + \Delta f) \quad (21)$$

$$2(\Delta f_{i+1+\dots}) = (i+1)2\pi \quad (22)$$

$$\Delta f_{i+1} - \Delta f_L = \pi \quad (23)$$

$$\lambda_d = \frac{\lambda_o}{\sqrt{\epsilon_{eff}}} = \frac{c/f}{\sqrt{\epsilon_{eff}}} = \frac{c}{\sqrt{\epsilon_{eff}}} / f \quad (24)$$

$$\frac{2\pi}{\lambda_d} = \frac{c2\pi f}{\sqrt{\epsilon_{eff}}} \quad (25)$$

$$\Delta f_L = \beta L = \frac{2\pi}{\lambda_{di}} L = \frac{2\pi f L}{c / \sqrt{\epsilon_{eff}}} \quad (26)$$

So:

$$2L = \frac{c}{\Delta f \sqrt{\epsilon_{eff}}} \quad (27)$$

this expression can be used to define the peak frequency. The physical length of the line is 35 mm,

$$\Delta f = \frac{c}{2L \sqrt{\epsilon_{eff}}} \quad (28)$$

EBG structure can be characterized as a network consisting of a cascade connection of several two-port networks as shown on Figure 3-18.

For this reason a 2×2 transmission, or $ABCD$, matrix is used for its analysis [73], [74]. The $ABCD$ matrix of the cascade connection of two or more two-port networks can be easily found by multiplying the $ABCD$ matrices of the individual two-ports. The $ABCD$ matrix is defined for a two-port network in terms of the total voltages and currents:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (29)$$

Figure 3-18 ABCD matrix

V_1 and I_1 are the voltage and the current at port 1 of the network. V_2 and I_2 are the voltage and the current at port 1 of the network flowing *into* port 2

For the cascade connection of two two-port networks shown on Figure 3-18, Equation 30 can be used:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_3 \\ I_3 \end{bmatrix} \quad (30)$$

It can be also related to Z parameters as (31)

$$\begin{aligned} V_1 &= I_1 Z_{11} - I_2 Z_{12}, \\ V_2 &= I_1 Z_{21} - I_2 Z_{22} \end{aligned} \quad (31)$$

For the proposed EBG structure (Board 3 Figure 3-9) the ABCD matrix was calculated and plotted on one graph with CST simulations (Figure 3-19).

Figure 3-19 Reflection S_{11} and transmission S_{21} coefficients of 2 single-cell EBG structure achieved with $ABCD$ matrix calculations and CST simulations

Figure 3-19 shows that the CST simulations and the $ABCD$ matrix have very good agreement except around 5 GHz. At 5 GHz the structure has the longitudinal resonance which was not considered in the $ABCD$ matrix. The $ABCD$ matrix is considering only normal mode and CST considers common mode and radiation from

the structure. To evaluate if there is an influence of the common mode, the power conservation check was performed. The result is shown in Figure 3-20.

Figure 3-20 Power conservation

Indeed at the frequency 5 GHz there is a power loss due to the resonance of the structure. Above 4.6 GHz the power is also lost in dielectric which is a well-known effect.

3.6 Stopband of EBG

To analyze the onset and bandwidth of the stopbands of EBG, its dispersion diagram was calculated using one unit cell consisting of 17.5 mm line and 30x30 mm patch. The dispersion diagram shows the propagation constant as a function of frequency. It can be built by solving the equation:

$$\cos \gamma d = \frac{A + D}{2} \quad (32)$$

Where γ is a propagation constant, A and D are calculated from $ABCD$ matrix. The complex propagation constant is a frequency dependent parameter and is:

$$\gamma = \alpha + j\beta \quad (33)$$

Where α is a attenuation and β is phase constant. It is a measure of the change in the amplitude and phase of a wave between the points of origin or reference, and a point

at a distance z as it travels along the transmission line. A and D can be calculated from $ABCD$ matrix based on Z parameters using standard methodology

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \rightarrow \begin{bmatrix} A & B \\ C & D \end{bmatrix} \quad (34)$$

There are 2 different conditions

Case 1:

if attenuation constant α is 0, phase constant β is not 0 then there is propagation or pass band

$$\alpha = 0, \beta \neq 0, \text{ propagation } \gamma = j\beta, \cos \beta d = \frac{A+D}{2} \rightarrow \text{passband}$$

Case 2:

If attenuation is not 0, phase constant is 0 or π , then there is a stop band

if $\alpha \neq 0, \beta = 0, \pi$ which corresponds to standing wave $\gamma = \alpha, \cos \alpha d = \frac{A+D}{2} \rightarrow$

$$\left| \frac{A+D}{2} \right| \leq 1 \rightarrow \cos \beta d = \frac{A+D}{2}$$

$$\left| \frac{A+D}{2} \right| > 1 \rightarrow \cos \alpha d = \frac{A+D}{2}$$

$\beta d = \cos \frac{-A+D}{2} \rightarrow$ these frequencies correspond to the stopband of EBG, there is

no propagation of electromagnetic wave

Z is a function of frequency so β is also a function of frequency $\beta d = \beta(f)$

γ is the propagation constant

α is the attenuation constant

β is the phase constant

d is the length of the unit cell, for simulated structure $d=65$ mm

Based on this analysis the dispersion diagram has been calculated and plotted in Figure 3-21. It shows the phase constant β plotted with respect to the frequency. From the calculation of the dispersion diagram, a band is between two lines. In Figure 3-21 the first stop band of two single-cell EBG structure is in the frequency range from 0.3 – 1.8 GHz, in a frequency range from 1.8 – 2.7 GHz there is a first pass band. And in the frequency range 2.7 – 4 GHz there is a second stop band. In the Figure 3-22 the stop and pass bands obtained with dispersion diagram on the graph with measured S parameters have been plotted.

Figure 3-21 Dispersion diagram

Figure 3-22 Transmission coefficient S_{21} of two single-cell EBG structure

The stopband match very well with the measured transmission coefficient S_{21} . In other words, the structure behaves as a low pass filter. The passband is 450 MHz and all frequencies above it are attenuated at least 25 dB.

3.7 EBG variations

To evaluate the effect of the size reduction of an individual patch on the resonances in the power plane, several variations of EBG structures with different cell sizes were designed on a EURO-card printed circuit board (100×160 mm) using FR4 substrate. Board 5, shown on Figure 3-23, had equal length, shape and location of interconnecting traces, and different patch size. The dimensions of the patches and trace length for each EBG structure on Board 5 are listed in Table 3-3. All interconnecting traces were 0.25 mm wide and 35 mm long. The transmission coefficient S_{21} has been measured using the VNA in the frequency domain up to 10 GHz and plotted in Figure 3-23. As can be concluded from the graph, in a standard design approach of the power distribution network (Figure 3-23a) the power plane mirrors the ground plane and creates a transmission line sandwich, which behaves as an electromagnetic resonant cavity. The transmission coefficient for this structure (Figure 3-24) is the highest. As can be seen from the graph, the EBG structures b) and c) can better reduce propagation of noise compared to a standard power plane. EBG structured power plane has wider and more stable suppression band than standard power plane. As expected, the size of the patch also influence the resonances. The case b) shows the highest attenuation and the less resonant behavior comparing with the other design solutions.

Table 3-3 The dimensions of EBG structure on Board 5

Set	Patch size, [mm]	Length of connecting trace, [mm]
a)	30x95	-
b)	30x30	35
c)	20x20	35
d)	10x10	35
e)	5x5	35

Figure 3-24 Transmission coefficient S_{21}

To demonstrate the influence of the shape, length and inductance of the interconnecting traces on the resonances in the PDN, another test board, Board 6, shown in Figure 3-25, was prepared. On Board 6 each EBG variation had the same size of the patch $30 \times 30 \text{ mm}^2$, the difference was in the interconnecting trace.

Figure 3-25 Board 6. Variation of interconnecting trace for EBG structured power plane on FR4

Figure 3-26 Transmission coefficient S_{21} of EBG with different interconnecting traces lines on FR4 substrate

The inductance of the lines for the case b) is 453 nH, EBG fragments d) and e) have equal inductance of the interconnecting line which is 325 nH. All interconnecting traces are 0.25 mm wide. On the Board 6-b the interconnecting trace had a shape of meander, on the Board 6-c and Board 6-d the patches were connected with a straight trace located at the corner of the patch and in the center of the patch respectively, as shown in Figure 3-25) The EBG fragments were designed on EURO-card printed circuit boards of 100×160 mm. The thickness of the board was 1.6 mm. The transmission coefficient of these structures was measured and plotted on Figure 3-26.

As expected, the longer meander power trace results in a more resonant behavior of the structure, as shown in Figure 3-26, as there is additional coupling between parts of the meander. Two single-cell EBG structure interconnected with a thin straight power trace shows the lowest transmission, and damps the resonances in the board. The exact position of the power trace is not very important which gives flexibility for the design engineer. Almost 30 dB difference can be achieved employing EBG in PDNs, this fact is demonstrated by the comparison of curves a) and d) of Figure 3-26.

3.8 Common mode current analysis

Common mode radiation is more difficult to control than differential mode radiation, and it usually determines the overall emission performance of a product. The most common form of common mode radiation emanates from cables driven by noise voltages in the reference conductor of a PCB, here the ground plane. The assessment of common mode radiation can be realized by measuring of common mode currents on the cables. The radiation from the cables is directly proportional to the common mode current on that cable. Common mode emission can be modelled as a dipole, or monopole antenna (the cable) driven by a noise voltage (the ground voltage). For a short dipole antenna of length l , the magnitude of electric field strength measured, in the far field, at a distance r from the source is

$$E = \frac{4\pi \times 10^{-7} (f l I_{cm}) \sin \theta}{r} \quad (35)$$

where E is in volts/meter, f is in hertz, I_{cm} is the common-mode current on the cable (antenna) in amperes, l and r are in meters, and θ is the angle from the axis of the

antenna that the observation is made. The maximum field strength will occur perpendicular to the axis of the antenna where $\theta = 90^\circ$.

Using a common mode current clamp common mode currents generated in a cable connected to the Board 5 and Board 6 was compared. The measurements of common mode currents were performed with absorbing clamp EM 101 and PNAL Network Analyzer (NA) Agilent technologies N5230A. The current clamp is an RF current clamp, having inductive and capacitive coupling and allowing the induction of large currents on cables in the frequency range of 0.15 MHz to 1 GHz. The absorbing clamp is both a current probe and an 'antenna impedance' formed by a number of ferrite ring cores arranged in a row that surround the cable of the equipment under the test (EUT). Some of these ring cores are part of the current transformer. The output voltage of this current transformer is taken to the measuring receiver via an internal RF cable also loaded by ferrite rings. With power cables, the measurement result is not affected by the magnitude of the current since the currents of the forward and return leads cancel each other out. The clamp consists of a two-part plastic case that can be opened. Each part includes a set of ferrite ring core halves. The halves are arranged in spring-loaded holding devices to form a channel to surround the cable of the EUT to be inserted. By closing the upper part of the plastic case, the magnetic loop around the cable is completed. Practical eccentric catches provide the necessary contact pressure. The major advantage of the clamp is the highly repeatable and comparable common mode current measurements, compared to common mode measurements using a current probe only.

Figure 3-27 shows the used measurement set up. The measured cable (1 m length) was placed on a non-conducting surface, the test table, so that it was at least 40 cm away from a conductive floor or wall. It was connected to port 2 of the NA and stretched out over the length of the absorbing clamp. Then Board 5-a and Board 5-b were measured, each of them was connected to the cable and terminated with 50 Ω load. The current transformer was facing the equipment under of the test (EUT). The generator in the network analyzer was feeding the inner circuits with a test signal. Another port of the NA was connected to the absorbing clamp. Via the absorbing clamp the cable acts as an antenna tuned at all frequencies. The clamp measures a current on a cable by using inductive and capacitive coupling at the same time.

Figure 3-27 a) Set up for common mode measurements;
b) Electromagnetic absorbing clamp

Figure 3-28 Common mode measurements setup scheme

Inductive coupling is realised by a transformer having a one turn primary circuit which uses the clamp's ferrite tube of 60 cm length as magnetic core. The mechanism of capacitive coupling between the cable under the test and the primary turn (semi cylinder of a metal foil in the groove of the clamp) is as follows: the resistance in the impedance of the primary turn enhances the directional effect and diminishes the influence of the load at the back side of the clamp. A ferrite absorber provided in the clamp surrounds the power cable and acts as resistance for the high frequency power. The incoming current is measured at the absorber input by using a current transformer and an EMI measuring receiver. Since there is no matching between the disturbance source, the cable, and the absorber in this setup, the clamp is slid along the cable to obtain the maximum current.

Figure 3-29 Common mode radiation Board 3, Board 4

Figure 3-29 shows the measured common mode currents of Board 3 and Board 4. All measured amplitudes are written in terms of dBpW, according to the convention [75] that the absorbing clamp is measuring the radiated power. The common mode radiation from the cable connected to the EBG structured power plane (Board 4) is almost 20 dBpW less at the frequency around 0.9 GHz and around 1.6 GHz than in case of a standard power plane (Board 3). This shows the beneficial effect of the EBG structures. Comparing the radiated power of Boards 3 and 4 (Figure 3-29) with measured transmission coefficient S_{21} (Figure 3-10) of these boards, it can be concluded that reduction in radiated power corresponds to PDN noise reduction. At the frequencies 0.9 GHz and 1.6 GHz the standard PDN (Board 3) has a resonance frequency.

3.9 Summary

Reduction of PDN noise by means of EBG was studied by several researchers in the last decade. However, most of these structures are effective only in the limited frequency band. Often the structures are embedded in a PCB as a separate layer, or require extra vias which increase the manufacturing cost. In this work a new type of planar EBG structure was proposed which consists of 2 patches interconnected by a

thin power trace. The resonance reducing effect of EBG structure etched on a power plane while maintaining the ground plane solid was presented. The suppression of the propagation of unwanted noise in power distribution network (PDN) was achieved and analyzed. The EBG structure was analyzed by means of dispersion diagram. The transmission coefficient of prototype boards was measured with a network analyzer. The proposed two single-cell EBG structure behaves as a low pass filter. The passband is 450 MHz and all frequencies above it are attenuated at least 25 dB. The size of the patch also influences the resonances. The exact position of the power trace is not very important which gives flexibility for the design engineer. Performed full wave simulations with CST are in good agreement with measurements. The measurements of common mode radiation show that reduction in radiated power corresponds to a reduction of S_{21} .

4. Wide band segmented power distribution networks

Most of the EBG structures reported in literature are suppressing noise in a limited frequency band. We are more interested in a low-pass filter instead of such a band-pass filter. In this chapter the influence of the structure (size and shape), layout and amount of a series of EBG cells on its filtering behavior is investigated. Simulations in CST microwave studio were performed and it is shown that the one-unit cell EBG structure and the EBG with multiple cells have the same suppression bands. Based on this conclusion, several design strategies of EBG with broader suppression band are proposed.

4.1 One unit cell EBG versus EBG with multiple cells

As it was mentioned in the previous chapter, dispersion diagram analysis provides us with information about the frequency band in which the EBG structure attenuates electromagnetic waves. Conventional EBG with multiple cells are implemented as a separate layer between power and ground plane, but due to space restrictions on the PCB and cost constraints such solution is not optimal. In our approach it was proposed to etch EBG structures on the power plane. In this chapter it was analyzed how the amount of EBG cells can influence the stopband and passband of the structure and if it is possible to achieve good isolation using an EBG with a limited number of cells. For this purpose one-unit cell EBG shown on Figure 4-1 was designed.

Figure 4-1 One-unit cell EBG

The structure was etched on the power plane layer, while the ground plane remained solid. The thickness of the FR4 substrate was 1.6 mm. This one unit cell consists of a 17.5 mm long and 0.25 mm wide power trace interconnected with a 30x30 mm patch followed by another 17.5 mm power trace. The transmission coefficient S_{21} of this structure was calculated in the previous chapter (Figure 3-19) using CST Microwave Studio. Figure 4-2 demonstrates the stop and pass bands of this structure obtained with these calculations plotted on the graph with simulated S parameters. The unit cell was excited with 50 Ω ports as shown in Figure 4-1.

Figure 4-2 Transmission coefficient S_{21} of a one unit-cell EBG

According to the dispersion diagram calculations this one-unit cell EBG structure has a stop band in the frequency range from approximately 0.3 – 1.8 GHz, there is a pass band in the frequency range from 1.8 – 2.7 GHz, and in the frequency range 2.7 – 4.0 GHz there is a second stop band. Indeed, as can be seen from Figure 4-2, the structure has -15 dB attenuation around 1.5 GHz and around 3 GHz, which corresponds to the calculated stop bands.

To investigate if adding some extra cells to the one-unit cell EBG structure can influence the isolation performance of the structure, two, three and four cell EBG structures were designed. Their simulated S_{21} parameters are plotted in Figure 4-3, Figure 4-4, Figure 4-5 respectively.

Figure 4-3 Transmission coefficient S_{21} of two unit-cell EBG

Figure 4-4 Transmission coefficient S_{21} of a three unit-cell EBG

Figure 4-5 Transmission coefficient S_{21} of four unit-cell EBG

Figure 4-6 Transmission coefficient S_{21} of general EBG example, Board 1

The two unit-cell EBG structure had two 30×30 mm patch interconnected with a 35 mm line, the three and four unit-cell EBG structures had one extra line and an extra patch. All these EBG variations were excited with a 50Ω port in the center of the

patch. Figure 4-3 – Figure 4-5 demonstrate that the first stop band in the frequency range from 0.3 – 1.8 GHz corresponds with the low frequency transfer function of one, two, three and four unit- cell EBG. All 4 structures have the pass band in the same frequency range 1.8 – 2.7 GHz, and in the frequency range 2.7 – 4.0 GHz (second pass band) one, two, three and four unit-cell EBG demonstrate low attenuation. For all these structures the first 2 pass bands and the first 2 stop bands are the same. All 4 variations around 2.4 GHz have a dip which corresponds to analytical calculation of patch 01 mode resonance (Chapter 3, Table 3-2). These results, simulated in CST, demonstrate that stop bands and pass bands depend only on the design of the EBG unit cell and is not influenced by the number of cells. The number of cells is responsible for the attenuation level. The analytically calculated stop bands correspond very well with the simulated transmission coefficient S_{21} . By using only one unit-cell it is already possible to achieve 15 dB attenuation. By increasing the number of unit cells it is possible to increase the noise isolation. A three unit-cell EBG structure showed -60 dB. Each of these structures can be called a one-dimensional EBG structure because it was formed by repeating the unit cell along a single direction. These periodically patterned EBG structures are true “band-gap” and act as good band stop filter. But PCB power plane structures are very wide band, and are driven/ignited by a high frequency impulse caused by the power supply decoupling transient, causing resonances in a large frequency band. Although periodic EBG act as band stop filter they have very large resonances, which are even increased for multiple-cell EBG.

Figure 4-7 shows S_{21} of a general EBG example (Board 1) discussed in Chapter 3. It is effective only at frequencies higher than 4 GHz. At higher frequencies it has multiple resonances. To reduce the resonances at higher frequencies, it was proposed to use structures with varying dimensions of the cells, which is discussed in the next section.

4.2 Novel power plane geometry

In a practical PCB design there are several ways of isolating noisy components from the rest of the board. One of them is board zoning or board floor planning described in [11], [76]. This approach implies location of components on the PCB in separate zones according to their functions, as opposed to mixing them. With this arrangement, the high-speed logic has less chance to pollute signal traces. Another strategy of power isolation is to split a power plane into power islands [32], [77]-

[78]. As it was mentioned in Section 3.4, noisy components should be placed on separate islands, isolated from the rest of the board by an inductive and/or (small) resistive bridge. This can be a relatively thin trace with respect to the width of the island, or a ferrite bead or a wire connecting the islands, or have a separate connection to the power supply. This solution is effective in a frequency range from 0.5 through 1 GHz. At higher frequencies crosstalk between the power islands, through the air, is observed. To achieve the low pass filtering behavior of PDN in a wider frequency range and considering the fact that it is possible to achieve the same stop band by using only a limited number of EBG cells instead of a series of periodically patterned EBG cells, we propose to combine these 3 methods (EBG, board zoning and power islands) by creating a series of varying size of power patch structures to replace the power plane. Four experimental boards were designed to demonstrate the effect of the proposed PDN concept on the reduction of noise propagation in the power ground plane structure. Board-7 (Figure 4-7) represents a standard PDN. It was designed on a single EURO-card printed circuit board (100×160 mm). The dielectric of the PCB was FR4 and 1.6 mm thick. Four SMA connectors were connected to represent different port locations. Port 1 and port 2 of the board were connected to the VNA, and the insertion loss was measured. The measurements were performed in a frequency range 10 MHz – 10 GHz. Then port 1 of the VNA was connected to port 3 of the board, and port 2 of the VNA was connected to port 4 of the board. Another experimental Board 8 (Figure 4-8) contains three power patches with equal size of 48.3×85 mm. Four SMA connectors are connected to the board as shown on the Figure 4-8. The transmission coefficient S_{21} was measured between port 2 and port 1 and the results are shown in Figure 4-9. The resonance frequencies of the patches of Figure 4-8 are listed in Table 4-1. The first resonance is around 200 MHz and anti-resonance is around 300 MHz due to the combination of 2 patches. Around 0.85 GHz the peak which corresponds to 01 mode resonance is observed. The transmission coefficient S_{21} of the proposed board reaches -45 dB at 300 MHz and -50 dB at 1 GHz.

The transmission coefficient S_{21} measured between port 2 and port 1 of the Board 8 is lower than for a standard PDN design for frequencies upto 2 GHz.

To evaluate the power isolation between 2 patches port 1 of the VNA was connected to port 3 (Figure 4-8) and VNA port 2 was connected to port 4, then measurements of transmission coefficient S_{34} between ports 3 and 4 of the board 8 (all the other ports were terminated with 50 Ω load) were performed. The results are plotted on Figure 4-10.

Figure 4-7 Standard PDN. a) Board 7 front side, (b) Board 7 back side

Figure 4-8 Board 8 front side

Figure 4-9 Transmission coefficient S_{21} of Board 7 and 8 measured between port 2 and port 1

Table 4-1Resonances of the patch 48.3mm x 85mm

$f_{r.p.}$ [GHz]	k	m
0.8	0	1
1.7	0	2
2.6	0	3
1.5	1	0
2.9	2	0
4.5	3	0
1.7	1	1
2.3	1	2
2.9	1	3
3.1	2	1
3.4	2	2
3.9	2	3
4.6	3	1
4.8	3	2
4.5	3	0

This graph demonstrates that at frequencies below 4 GHz good power isolation can be achieved. Figure 4-10 demonstrates that it is possible to achieve almost 50 dB attenuation around 1 GHz. At higher frequencies the effect of the power islands is negligible. This was already observed in [40]. The low attenuation is mainly caused

Figure 4-10 Transmission coefficient of Board 7 and 8 measured between port 3 and port 4

because the patches forming EBG do resonate themselves and by the (capacitive) crosstalk between them.

4.3 Design of wide band segmented PDN

Common passive EMI filters involve the combination of capacitors and inductors using dedicated components [79]. Another class of filters are embedded flat filters [80], [81]. An example of such a common filters is the stepped impedance filter shown on Figure 4-11. This filter is composed of alternating low and high impedance microstrip transmission lines where the change in impedance is controlled by the line width of the strip. A high degree of attenuation in the stop band can be achieved by obtaining a 'high to low impedance ratio' ($Z_{OH}=Z_{OL}$ or by increasing the order of the filter [82]. At the same time, the filter is just a series connection of different values of inductors with different capacitors to ground forming a C - L network. Such filters are commonly used in microwave circuits, for example in baseband pulse shaping for data transmission. From a lumped element perspective this filter can be considered as an inductor-capacitor set, where we can distinguish a C , then a L , followed by a larger C , again a L and a C .

Figure 4-11 Transfer stepped impedance low pass filter (5th order,) [83]

All capacitors are connected to ground. This can be considered as a band stop filter. The idea of different sizes unit cells has been applied to our wide band low pass filter. Board 9 was designed as a combination of different power patches sizes (Figure 4-12), interconnected via 3 mm wide and 5 mm long power traces which act as inductors (Table 4-2). The power trace is used as inductive decoupling, while the power patch itself can be considered as a capacitor. The objective is to create a low pass filter. Each patch has its own resonance frequency. The unit cells have been

made with different dimensions (also l and w) to get different resonant frequencies. The measured transmission coefficient S_{21} is shown in Figure 4-13.

Figure 4-12 (a) Board 9 front side, (b) Board 9 back side

Figure 4-13 demonstrates that using varying size power patches is very efficient in a broad frequency range, and gives good noise isolation. Figure 4-13 compares the design of Board 9 with the standard PDN (power and ground planes symmetrical and identical in shape and size). For both boards port 1 was $50\ \Omega$ located in the left upper corner of the board (15 mm from the right hand side of the board and 15 mm from the upper edge), port 2 was also $50\ \Omega$ (105 mm from the right hand side and 60 mm from the upper edge) as shown in Figure 4-12.

Table 4-2 Dimensions of the patches

Patch	Dimensions	
	Length, l [mm]	Width, w [mm]
A	45	45
B	40	40
C	35	35
D	30	30

The combination of Board 8 and Board 9 was implemented in the design shown in Figure 4-14. This board was etched on 1.6 mm FR4 substrate. The size of individual patches vary from 5×5 mm to 10×10 mm, 15×15 mm, 20×20 mm, 25×25 mm, 30×30 mm and 35×35 mm. The patches are chosen in a way that each of them attenuate at a different frequency, and the idea is that a combination of the attenuation leads to low pass filtering performance of the structure.

Figure 4-13 Transfer function of Board 9

Figure 4-14 Board 10 Front side

The transmission coefficient S_{34} , measured between port 3 and port 4 while all other ports were terminated with 50Ω , is shown in Figure 4-15. In Figure 4-16 S_{34}

parameters of Board 8 and Board 10 measured between port 3 and port 4 are compared. These two figures demonstrate that Board 10 is mitigating noise in a wider frequency band than Board 8 or the standard power plane of Figure 4-7. The cut-off frequency is lower and sharper, but due to the interconnected patches and the wide (thus low inductance) interconnecting traces between the patches Board 8 resonates causing a worse transfer function between 550 and 1700 MHz.

Figure 4-15 Transfer function of Board 10

Figure 4-16 Transfer function of Board 8 and 10

4.4 Summary

In this chapter it was shown that it is possible to achieve good noise isolation using EBGs with a limited number of cells. Using periodic cells are creating a real band gap or band stop filter, but the disadvantage is the low reduction of noise outside this band. Using a multiple set of differently sized power patches a wide band suppression could be created. Based on this concept four experimental boards were designed. It was shown that PCB boards employing differently sized power patches instead of large power planes on printed circuit boards reduce unwanted resonances in the Power Distribution Network (PDN) and acts as a low pass filter in a wide frequency range.

5. PDN variations on PCB with active components

In this chapter four different power isolation concepts are evaluated. Instead of what has been done by many authors [39],[84],[85] not the passive behavior, but a design with active components was used. Boards with active components were built and measured to investigate the effect of the geometry of the PDN on the common mode noise generated by the board into its environment. The effect of the power plane, power track and EBG structures on the noise reduction in printed circuit boards with active components is investigated. Longitudinal noise voltage measurements of these boards are performed and to evaluate the effect of EBG on CM currents, radiated electromagnetic fields were measured in a reverberation chamber. Measurements with a shield around the noisy electronics on the printed circuit board were also performed. In addition, near field measurements were performed with an EMxpert XY near field scanner.

5.1 Power isolation

As it was shown in previous chapters, the standard power plane parallel to a ground reference plane forms a symmetric transmission line which at high frequencies has a high transfer impedance. It forms a parallel-plate waveguide which can be excited causing a voltage wave to propagate radially away from the excitation point. The line over a ground plane has the lowest transfer and can serve an alternative to solid power planes. It was also shown that power planes are needed locally for decoupling, the optimal solution would be two single-cell EBG structures or EBG with different cell sizes. In this chapter the concept was applied using a real electronic circuit. Four identical digital electronic circuits, designed to generate PDN noise deliberately, were built. Each board was 50 mm wide, 160 mm long and 1.6 mm thick employing FR4 dielectric covered with a 0.035 mm copper layer on both sides. The circuit schematic diagram for all active boards is the same and is shown in Figure 5-1. The dual copper clad boards have a ground plane on the side opposite to the component mounting and four different arrangements of the power distribution. Each board has a noise generator consisting of the 24 pin octal bus driver ACT11244PW fed by a 10 MHz crystal controlled oscillator. The line driver's signal rise time was approximately 0.3 ns/V, resulting in harmonics into the GHz range. All 8 driver inputs are receiving the 10 MHz clock output signal. The driver in turn charges and discharges eight 47 pF Surface Mount (SMT) capacitors

Figure 5-1 Schematic diagram of the active circuit

Figure 5-2 Power distribution network employing (a) Board 11 a power plane, (b) Board 12 a power line, (c) Board 13 two single-cell EBG, (d) Board 14 an EBG with different cell sizes

at this 10 MHz rate. The clock generator and driver were supplied with 5 V DC supply voltage via a 9 V power supply stabilized by the common 7805 linear regulator. The active circuits are listed in Table 5-1.

Table 5-1 Active components on the PCB's

Device	Manufacturer	Description
ACT11244PW	Texas Instruments (TI)	Octal non inverting Buffer
L7805CV ST	Microelectronics (STM)	5V linear regulator
CSX750FCC	Citizen (CTZ)	10.0000 MHz oscillator

The boards were designed with the PDN configurations as listed in Table 5-2. On Board 11, shown in Figure 5-2 a, the conventional design of a power distribution network using a power plane was employed. The clock generator and driver were supplied with power via the power plane. This power plane was parallel to the ground plane and identical to it in shape and size. In [86] it was described that the longitudinal noise voltage developed in the ground conductor is determined by the ratio of the net partial inductance of the ground plane compared to the total loop inductance of the transmission line. This concept is very similar to the transfer impedance concept used in this thesis. And it was recommended to replace power planes with power lines or power tracks. Therefore, to reduce the effect of the symmetrical power plane Board 12, shown on Figure 5-2 b, was built. The clock generator was supplied via the 2.7 mm wide and 100 mm long power track. In [87] and [88] a similar approach was proposed, where a set of transmission lines was connecting the PDN to the power pins of the line driver.

Table 5-2 Overview of boards designed for a study

PDN configuration	Name	Figure
Power plane	Board 11	5-2 a
Power line	Board 12	5-2 b
Two single-cell EBG	Board 13	5-2 c
EBG with different cell sizes	Board 14	5-2 d

Another approach to reduce noise is to use EBG structures. As it has been demonstrated in previous chapters, EBG structures on power planes of PCB boards act as low-pass filters which significantly reduce the resonances, and the common mode currents due to these resonances. To demonstrate this effect, the test board shown in Figure 5-2c, Board 13 was created. The power patches, which are actually two cells of an EBG structure of 50×50 mm, were interconnected by a 60 mm long and 2.7 mm wide power trace. The active components for the power regulator and the noisy line driver were each placed on one of the power patches. The objective is that the decoupling currents are isolated on the power patch and are not propagating over the board. The last design configuration is shown in Figure 5-2 d. This Board 14 contains cells with different size patches (50×50 mm, 20×20 mm, 15×15 mm, 10×10 mm, 5×5 mm, 50×25 mm) interconnected with 2.7 mm wide power traces. This structure forms an EBG, by employing a periodic structure of different patch sizes. The power trace is used as a small inductive decoupling, while each patch itself can be considered as a capacitor. This creates a wide-frequency band stop filter, while each of the cells has a different suppression band, and resonance frequency.

To compare the functional behavior of the electronic circuitry on these four test boards the voltage on the load side of each board was measured, which is the voltage across the capacitor (47 pF) connected to the output of IC1, the 74ACT11244. The voltage was measured on every of the 8 capacitors of Board 11, Board 12, Board 13 and Board 14. Figure 5-3 shows the measured voltage. For all 4 structures it is almost the same, which means that the electronic circuitry on all 4 cases works properly. Note that the large undamped amplitude was deliberately created by loading the IC with only a capacitor, and thus to create maximum load currents while still not overloading the circuit. This creates a large SSN, using 8 parallel outputs, resulting in as much PDN noise current as possible.

Figure 5-3 Measured voltage on the load side on Board 11, Board 12, Board 13, Board 14

5.2 CM noise voltage measurements

To evaluate the effect of the described power isolation concepts on the noise reduction of the PCB, the longitudinal noise voltage of the proposed board configurations was measured. Following the procedure described in [89] and [90] the test board was placed at a distance $d=28$ mm above a brass reference plane with a width 120 mm. This serves to create a common mode impedance of approximately $50\ \Omega$ to reduce reflections which can occur due to mismatch of impedance with the $50\ \Omega$ instruments, and thus influence the measurements. Figure 5-4 and Figure 5-5 shows the measurement set up. The ground plane of the PCB was connected to chassis-type N-type connectors. The ground of these connectors was connected to the brass structure, and the inner conductor of one of these N-type connectors was connected to a Rohde and Schwarz ESS test receiver. The N-type connector on the other side was terminated in a $50\ \Omega$ load. The power supply current flows through the power plane/trace structure. Depending of the topology (Figure 5-2a-d) some CM noise voltage is generated across the PCB ground plane which is measured for this experiment. It would generate the unwanted common mode (antenna) current in actual applications [17]

Figure 5-4 Schematic of test set-up for measuring the noise voltage developed in the ground plane

Figure 5-5 Test set-up for measuring the noise voltage developed in the ground plane of the tested boards

Via this test setup the CM noise voltage is measured, via the brass reference plane. There are three conditions of validity to use this setup [44]:

The transmission line cross section has to be small with respect to the wavelength of the signal used in the measurement setup, and

The transmission lines are terminated in their characteristic impedance.

The third condition is that the current in the brass reference planer should be negligibly small compared to the current in the PCB power plane and PCB ground plane. This is achieved via the 50 Ω terminating impedance of the measuring

receiver, which is larger than the ‘internal’ impedance of the noise voltage source developed in the PCB ground plane [17].

Because the clock oscillator is very stable a small measuring bandwidth for the test receiver could be used. This results in a low noise level and high dynamic range. The measurements were performed in a frequency range 10 MHz-1 GHz and the longitudinal noise voltage developed between the two ends of a PCB ground plane was measured. This implicitly assumes no voltage loss over the brass bracket. The amplitude of the measured noise voltage is shown in Figure 5-6. At 500 MHz, a longitudinal resonance of the structure creates the peak in the measured response. All the boards have the same width (50 mm) and this resonance corresponds to the [0;1] excitation mode or “back and forth reflection”. Figure 5-6 shows that using a power trace instead of a power plane can decrease the noise voltage between 5 and 15 dB. Two single-cell EBG (Board 13) shows a large reduction of the noise voltage up to 500 MHz in comparison to Board 11. At higher frequencies the effect is lost and noise reduction of Board 13 is almost the same as Board 11, due to the crosstalk between the islands. Therefore a board with different cell size was used creating a wide frequency electromagnetic band gap. This board shows the largest effect on noise reduction.

Figure 5-6 Longitudinal noise voltage of boards employing the described power isolation concepts

5.3 Noise voltage measurements with shielded noisy part of the board

Because the transmission line structure used to measure the longitudinal noise voltage is open it can pick up fields from other sources. To exclude the local, differential-mode, switch current fields from contributing to the boards common mode noise voltage, the noisy part of the board was shielded with a metal shield. The measurements of the noise voltage generated over the ground plane have been repeated using the same test set up as described in Section 5.2. The amplitude of the measured noise voltage is shown in Figure 5-8. At 500 MHz the boards show the same resonance as before, which corresponds to the [0;1] excitation mode.

Figure 5-7 Test set-up for measuring the noise voltage developed in the ground plane of the tested boards

Figure 5-8 shows that all 3 solutions are more effective decreasing the noise voltage, compared to the PCB with a power plane. The board power line is very efficient in a frequency band lower than 500 MHz. The board with different cell size EBG with shielded noisy electronics can reduce the noise in a frequency band 10 MHz-1 GHz, and the 2 cell EBG shows good performance till 500 MHz. The resonance at 500 MHz is less pronounced due to the shielding. Comparing Figure 5-6 and Figure 5-8 shielded two single-cell EBG show better results than unshielded two single-cell EBG in the frequency range from 500 MHz till 1 GHz.

Figure 5-8 Longitudinal noise voltage of boards employing described power isolation concepts, with shielded active part

Around 800 MHz the difference is almost 20 dBμV. One remark has to be made on the frequency range. The experiment has been optimized for a basic and useable test setup which gives repeatable results. The validity is however much broader, and by scaling the structures up or down, the effect should be similarly effective at lower respectively higher frequencies.

5.4 Radiated emission measurements using a VIRC

One of the ways of estimating the radiated emission is to conduct radiated emission measurements inside a Reverberation Chamber (RC) [11]. A RC consists of an electromagnetic resonant cavity featuring some kind of mode stirring process to create changing boundary conditions in order to obtain a statistically uniform electromagnetic field. This is conventionally accomplished by introducing a mechanical tuner into a shielded room. By rotating the tuner, the boundary conditions within the chamber are changed. Once the tuner has been moved to a sufficient number of positions the field at any point is statistically uniform [91].

A particular non-conventional reverberation chamber available at the University of Twente is the Vibrating Intrinsic Reverberation Chamber (VIRC), as shown in Figure 5-8 [92]. The VIRC is made of conductive cloth. By vibrating the walls,

inside the VIRC a diffuse, statistically uniform electromagnetic field is created without the use of a mechanical, rotating, mode stirrer. The results regarding the VIRC lead to a better homogeneity and increased field strength compared to a conventional mode stirred chamber [92, 93]. The big advantage is that a measuring antenna does not have to be positioned in a sphere around the tested object, the Equipment Under Test (EUT), to find the maximum emission. The EUT can be positioned at any location in the RC and will create always the same field strength, in a RC. Our boards (Board 11-Board 14) have unknown spectrum and the fields that reach our passive antenna are, statistically, a good representation of what the boards actually emit as noise. Each board was placed inside the VIRC as depicted in Figure 5-9. For our measurements a discone antenna was used [94]. The main advantage of the application of this antenna for VIRC measurements is its compact size and large frequency operation band (0.35 – 3 GHz). The Rohde and Schwarz FSH3 Spectrum Analyzer was connected outside the reverberation chamber. Comparative measurements were done: the boards under the test without shielding (Table 5-2b-d) were each compared against the board with conventional power plane (Figure 5-2a).

Figure 5-9 Position of board inside the VIRC

Figure 5-10 depicts the comparison of the radiation emission measurements of the board with the conventional design of a power distribution network using a power plane (Board 11), and alternative board with a power line in the PDN (Board 12). The track was 2.7 mm wide and 100 mm long. It can be seen that the design of the Board 12 with power line radiates more than the Board 11 with standard power

plane. This is due to fact that this is an open structure, which suggests that the main portion of the radiated emission is differential mode.

Figure 5-10 Comparison of radiated emission of Board 11 (board with power plane) and Board 12 (power line)

Figure 5-11 compares the measured radiated emission of Board 13, with two single-cell EBG, to the Board 11 with the power plane as PDN.

Figure 5-11 Comparison of radiated emission of Board 13 (board with two single-cell EBG) and Board 11 (power plane)

It can be seen from these measured results that the Board 11 radiates more due to the parallel-plate configuration corresponding to resonant frequencies. Around 600 MHz Board 13 with EBG cells has its pass band which increases the radiated emission. These characteristics indicate that a 2 cells-EBG power plane can create low radiation in the measured frequency band. But the main reason for it's effectiveness is the reduced differential mode current in the power-ground plane circuit, because the power supply decoupling current is kept local. Figure 5-12 shows the measured radiated emission of the board with EBG with different cell sizes, Board 14, with respect to the standard PDN.

Figure 5-12 Comparison of radiated emission of Board 14 (board with EBG with different cell sizes) and Board 11 (power plane)

Figure 5-12 measured results demonstrate that Board 11 radiates more due the parallel plate configuration, especially at its resonant frequencies. The radiation of the EBG board (Board 13) is much less than the standard PDN (Board 11). The EBG board with different cell sizes, Board 14, can significantly reduce the radiated emission. Comparing the noise voltage measurement results presented in Section 5.2 and 5.3 and the radiated emission measurement results in Section 5.4 we can observe that the EBGs reduce the noise voltage and the emission levels, but are also limiting the direct emission of the circuitry. This can be concluded from a comparison of Figure 5-10 with 5-11 and 5-12.

5.5 Measurements of emissions of active boards with EMxpert XY near field scanner

The near field emissions of boards with active circuits shown in Figure 5-2 was measured with an EMxpert XY near field scanner. The EMxpert allows to visualize near fields, and the supplier suggests it allows to find the root causes of potential EMC and EMI problems. It helps to find unintended radiators or RF leakage. It consists of a patented flat compact scanner and adapter, a customer-supplied spectrum analyzer and EMxpert software. The scanner is used for EMI analysis of high speed, high power, and/or high density/complexity PCB boards. The boards were placed on the scanner as shown in Figure 5-13. The measurement results at a frequency of 250 MHz are shown in Figure 5-14. During the second measurement the boards were rotated, i.e. the power plane of the board was facing the scanner, as shown in Figure 5-15. The measurements were performed at frequency of 250 MHz.

Figure 5-13 EMxpert XY nearfield scanner

Figure 5-14 Noise generated at 250 MHz by active boards with PDN employing
(a) Board 11 with power plane, (b) Board 12 with power line,
(c) Board 13 with two single-cell EBG,
(d) Board 14 with EBG with different cell sizes

Figure 5-15 EMxpert XY nearfield scanner

Figure 5-16 Noise generated at 250 MHz by active boards with PDN employing
 (a) Board 11 with power plane, (b) Board 12 with power line,
 (c) Board 13 with two single-cell EBG,
 (d) Board 14 with EBG with different cell sizes

As can be seen from the graphs depicted on Figure 5-16, the noise is propagating through the power plane of Board 11. Employing a power line, two single-cell EBG or EBG with different cell sizes helps to keep noise locally and prevent it to propagate through the board. Moreover, the maximum noise level of a PDN with the EBG with different cell sizes, Board 14, is much lower compared to the other boards: 28 dB μ V for Board 14 versus 35 dB μ V for the other boards.

5.6 Summary

The effect of power plane, power track and two single-cell EBG structures and different sized cells EBG on the noise reduction in PCB with active components was investigated. Many researchers evaluated the effect of passive EBG structures. In this chapter not only the passive behavior, but a design with active components was used. In [95] the radiation of far fields of unpopulated EBG structured PCB has been confirmed when radiation is monitored at 3 m distance away from the board. Because such measurements are extremely time consuming radiated emission measurements were performed inside a Reverberation Chamber (RC). The performed measurements prove that all 3 solutions are more effective decreasing the noise voltage with respect to a power plane. The creation of a wide band EBG showed to be effective on the radiated emission of PCB with active components.

6. Modeling the power circuit of a CMOS bus driver in SPICE

The subject of this chapter is to create an equivalent circuit of an active board on a two single-cell EBG (Board 13) with SPICE circuit simulator to eventually enable synthesis of better PCB PDN lay-outs for high-speed, usually digital, designs. The modeling of the 2 single-cell EBG structure, Board 13, and standard power plane, Board 11, in SPICE is done using the so called "bed-spring" analogy [96] where small squares of copper plane are replaced by rectangles with four inductors as edges. This chapter proposes some behavioral models for devices on our active boards in order to build a SPICE model of these boards.

The main motivation is that the electromagnetic field solvers, like Microwave Studio, cannot deal easily with non-linear (active) components. One way to solve the problem is to simulate the EBG structures in an EM tool and then use the results as a building block, for instance via S parameters, in a (time-domain) circuit simulation tool. In this chapter also the passive parts are modeled as a circuit model.

6.1 Modeling the ACT11244 with its capacitive loads

The description of the boards is given in Section 5.1. As can be seen in Figure 5-1, the circuit consists of a 10 MHz clock circuit followed by an octal bus driver loaded with eight capacitive loads. On a low to high transition of the driver, all eight capacitors will be charged through the output impedances of the driver. On the subsequent high to low transition, the capacitors will be discharged. The charge-discharge circuit is shown in Figure 6-1.

Figure 6-1 Capacitive load charge-discharge circuit

Figure 6-2 Model for the behavior of an ACT11244 driving load capacitors

The PDN is loaded only during charge actions. Only the charge operation will draw current from the driver's power supply as shown in Figure 6-2a. During the discharge cycle shown in Figure 6-2b the current will flow only locally in the driver output circuits. In addition to the current drawn by the ACT11244 chip there is the 10 MHz oscillator. It also provides a square wave driving the input capacitances of the ACT11244 input circuits. According to the data sheet of the ACT11244PW [97], the values are typically 4 pF per input. Eight of these are loading the oscillator in parallel, adding up to 32 pF. The ACT11244 is a non-inverting buffer which means that charging of its input capacitances occurs simultaneously with the charging of its output load capacitances (give and take some propagation delay). In order to keep the model as simple as possible, the behavior will be considered as the charging and discharging of 9 capacitors with a total value of $8 \times 47 + 32 = 408$ pF at a rate of 107 times per second with a 5 V amplitude square wave source, 1 ns rise-time with a non-linear output impedance of 1/9 times the value of one ACT11244 output.

6.2 Driver output behaves as a non-linear resistor

As outlined above, only the charging action has implications for the power supply current. The SPICE model hence should mimic 10^6 charge pulses per second, loading the power bus. This can be achieved by using a 5 MHz square wave feeding the non-linear resistor and the capacitors as shown in Figure 6-1. The decoupling capacitors in this figure are hidden in the EBG-PDN structure. The implicit assumption here is that the RF components generated during the rising edge of this 5 MHz (10^6 transitions) generator are identical to those generated during the falling edge. The symmetric structure of the ACT11244 output and the identical non-linear series resistor used for both edges make this very likely. The ACT11244 output impedance can be derived from Figure 6-3 is determined using the source line between 0 and 5 V and 0 and 200 mA.

Figure 6-3 AC11244 output characteristics

As is obvious from Figure 6-3, the output resistance of the ACT11244 is nonlinear. A second order polynomial fit has been determined and divided by 9 to model 9 output-resistors in parallel. This results in Equation 36. Since a total of 9 capacitors are being charged (and later discharged) the combined load resistance has been labeled R_9 .

$$R_9 = 1.66 + 11.1 |I_{charge}| + 67 I_{charge}^2 \quad (36)$$

Notice the absolute value of the charge current, $|I_{charge}|$, used in the linear term in Equation 36. This is necessary to simplify the SPICE model to a square wave voltage source with a frequency of 5 MHz (10^7 transitions per second). This will result in a positive current spike on the rising edge and a negative one on the trailing edge. In reality all current spikes are loading the Direct Current (DC) power line. This simplification is a compromise and is acceptable as the behavior of the PDN is to be studied in terms of a maximum voltage disturbance around each transition. In the real world, all disturbances would be reducing the available power bus voltage. In the SPICE simulation, there will be alternating transitions in the positive and negative direction. It is important, however, that the shape and size of all transitions are identical. Equation 36 is sensitive to the polarity of the charge current. For that reason, the absolute value of this current is used in the linear term.

6.3 PDN local decoupling capacitors

The decoupling capacitors are supposed to form a barrier between the noise generating elements, the oscillator and driver, on the PCBs and the PDN. Their efficiency depends on the parasitic elements: Equivalent Series Resistance (ESR) and inductance (ESL). The value of these parasitic elements depends on the way the capacitor is built and mounted. For the 10 nF SMT capacitors, measurements have been performed using a spectrum analyser with tracking generator to see their behavior over frequency. The analyser generator combination was calibrated to 0 dB while directly interconnected and then the capacitor, mounted on a special test board, was used to short-circuit the tracking generator output, as shown in Figure 6-4. The measured response is shown in Figure 6-5.

Figure 6-4 Measurement of decoupling capacitor parasitics

For the 10 nF decoupling capacitor model used on these active boards, a 55 dB series resonance attenuation is measured at 70 MHz. From these numbers the two parasitic parameters can be derived:

1. The equivalent series resistance (ESR) is approximately $R_{ESR}=45 \text{ m}\Omega$, based on the 55 dB attenuation in this 50//50 Ω measurement system

Figure 6-5 Decoupling capacitor behavior with frequency

2. The equivalent series inductor (ESL) is approximately $L_{ESL}=0.5\text{ nH}$, based on the resonance frequency with the series capacitor of 10 nF at 70 MHz.

6.4 Modeling the active current in SPICE

The 10 MHz clock and ACT11244 driver loaded with capacitors can be modeled in LTSPICE [98] as shown in Figure 6-6. Running the schematic of Figure 6-6 results in the output voltage versus output current graph in Figure 6-7. The current drawn from the PDN will be a series of this type of current spikes with a repetition frequency of 10^7 transitions/s. Figure 6-8 shows the same current in detail for the first low to high transition. This load current source can now be used to excite the various PDN PCB SPICE models developed in the following sections. This loading will be done in the way shown in Figure 6-1.

Figure 6-6 LTSPICE model for non-linear driver with capacitive load

Figure 6-7 ACT11244 with capacitive load output voltage vs. PDN current

Figure 6-8 ACT11244 with capacitive load output voltage vs. current (detail)

6.5 The highest frequency in the power current spectrum

The highest frequency present in these PDN experiments is determined by the fastest rise time in the power transients. Howard Johnson defines, or actually chooses, this maximum as the knee frequency as in Equation 37 [18]. The rise time of the ACT11244 device output current (asymptote at the start of the output transient) is $\tau_r = 110$ ps. To determine this value, the data of the SPICE simulation was exported to MS-EXCEL and the slope at the start of the current spike determined as $4 \cdot 10^9$ A/s. Extrapolated to the maximum current value (440 mA) this gives the mentioned result.

$$F_{knee} = \frac{1}{2\tau_r} = 4.5 \text{ GHz} \quad (37)$$

6.6 Modeling interconnected patches in SPICE

The proposed SPICE model considers both patches and traces above a ground reference plane as loss-less transmission lines. The thin traces are modeled in the traditional way as partial element equivalent circuits (PEEC) shown in Figure 6-9. Note that both the trace and the underlying ground reference plane should receive (partial) inductances [99]. This is essential as the model will be used both for power

island separation analyses as for CM current generation into e.g. connected wiring. The source for these CM currents are the voltages appearing over the ground plane as a result of currents owing in it.

Figure 6-9 Trace over ground partial elements model

6.7 Meshing of power patches and ground plane

Each trace in the model is broken up into L - C sections, as in Figure 6-9, shorter than $\lambda/2\pi$ where λ is the wavelength of the highest excitation frequency. For a patch this is a 2-dimensional process: each patch is subdivided, or meshed, into squares with dimensions smaller than $\lambda/2\pi$. An additional requirement is that the connection points of physical sources and loads should be made available in the model. For example the Board 13 shown in Figure 5-2c, has two power patches of 50×50 mm. The ground plane underneath it has the same width but is 160 mm long. Figure 6-10 shows the nomenclature applied to patches and traces.

Figure 6-10 Labeling of patch and trace dimensions

The edges of each square in Figure 6-11 are replaced by small inductors and the nodes on each corner by small capacitors towards the ground plane to create the SPICE model of a patch. The ground plane is subdivided in the same way. This indicates that the meshing of patches and ground plane and the sectioning of the traces are interrelated as the capacitors originating from the nodes in the patches terminate in the nodes on the ground plane. This implies that the meshes of patches and ground plane have identical dimensions. i.e. all node capacitors are vertical. The SPICE model for a patch is a matrix of capacitors interconnected by inductances as shown in Figure 6-12. Note that, in this drawing, each capacitor is still connected to a triangular ground symbol, provisionally showing the reference plane as an ideal conductor with zero resistance and inductance in order not to complicate the picture too much. The final model will also show the ground plane as a grid of inductances where the capacitances are connected to the nodes in this grid. An impression is shown in Figure 6-12.

Figure 6-11 Subdivision of the Largest Power Island

Figure 6-12 SPICE model for 1 power patch (partial view)

6.8 Mesh sizes

The actual wavelength, needed to calculate the maximum section or mesh dimension, depends on the propagation delay, τ_{PD} , of the transmission line or patch under consideration. The propagation delay is solely dependent on the dielectric permittivity and magnetic permeability of the medium in which the line is placed as shown in Equation 38.

$$\tau_{PD} = \sqrt{\epsilon_0 \epsilon_{eff} \mu_0} \quad (38)$$

Equation 38 contains an effective relative permittivity, ϵ_{eff} . This is because the patch and trace medium is not homogeneous. At the side of the ground plane, there is the

epoxy-glass base material. On the other side, there is air. The assumptions made here are that the magnetic permeability of the epoxy-glass and air is equal to μ_0 , the value for free space, while the dielectric permittivity on the air side is ϵ_0 , the value for free space, and $\epsilon_0\epsilon_r$ on the "epoxy-glass" base material side. ϵ_r is the relative permittivity of this base material. To calculate the effective permittivity in this micro-stripline case, the relative permittivities of both media are needed:

- ϵ_r for the epoxy-glass base material
- 1 for the air

Equations for the effective dielectric permittivity used here can be found in [100]. Other sources are [101], [18] and [102]. The effective dielectric permittivity depends on the geometry of the transmission line. For the patches, which are much wider than the base material thickness, $W_p > d$, such as shown in Figure 6-10, and the effective dielectric permittivity is calculated using Equation 39. For the traces which are 2.7 mm wide, the trace width, D , is still larger than the base material thickness, 1.6 mm. The same equation is used, now using the parameter D instead of W_p , see Equation 40.

$$\epsilon_{\text{effPatch}} = \frac{\epsilon_r + 1}{2} + \frac{\frac{\epsilon_r - 1}{2}}{\sqrt{\frac{12d}{W_p} + 1}} \quad (39)$$

$$\epsilon_{\text{effTrace}} = \frac{\epsilon_r + 1}{2} + \frac{\frac{\epsilon_r - 1}{2}}{\sqrt{\frac{12d}{D} + 1}} \quad (40)$$

For very narrow traces, where $D < d$, a correction is needed as shown in Equation 41 [18].

$$\epsilon_{\text{effNarrow}} = \epsilon_{\text{effTrace}} + \frac{\epsilon_r - 1}{50} \left(1 - \frac{D}{d}\right)^2 \quad (41)$$

The base material dielectric permittivity ϵ_r can be found by measuring the value of the capacitance of the board and then using the parallel plate capacitance expression shown in Equation 42 to extract the value of ϵ_r as performed in Equation 43.

$$C_{\text{pplate}} = \frac{\text{Area}_{\text{cap}} \cdot \epsilon_0 \cdot \epsilon_r}{d} \quad (42)$$

$$\epsilon_r = \frac{C_{\text{pplate}} \cdot d}{\text{Area}_{\text{cap}} \cdot \epsilon_0} \text{ F/m}^2 \quad (43)$$

Figure 6-13 3-D representation of a patch over ground, 2 layer L - C model

Figure 6-14 Patch cross-section dimensions

With $\epsilon_0=8.85 \cdot 10^{-12}$ F/m, the value of the 50×160 mm board measured with LCR meter is $C_{pplate}=200$ pF with $Area_{cap}=8 \cdot 10^{-3}$ m², the dielectric permittivity of the base material is found as $\epsilon_r=4.5$. Equation 35, the effective dielectric permittivity for full power plane or any of the patches, all widths are $> d$, evaluates as $\epsilon_{effPatch}=4.3$. From Equation 38, the propagation delay for the patch area is then $\tau_{PD}=6.9$ ns/m. The shortest wavelength can now be determined from the highest frequency, $F_{knee}=4.5$ GHz, present in the power transients as calculated using Equation 44.

$$\lambda_{minPatch} = \frac{1}{F_{knee} \cdot \tau_{PD}} = 0.032 \text{ m} \quad (44)$$

The maximum edge length of each mesh, S in Figure 6-11, is $S \leq \lambda_{minPatch}/2\pi = 5$ mm. Using 5 mm will provide an integer number (10) of meshes on 50 mm, i.e. in the

SPICE model a connection can be made in the middle of the patch. That is where the trace connects and where the ACT11244 chip and the oscillator get their supply. For the patches of Board 14 the mesh length will have to be divided by two (i.e. $S=2.5$ mm) to obtain a connection point in the middle.

6.9 Values of the mesh capacitors

Given a mesh square of 5×5 mm, the capacitance of each square can now be calculated. Board 11 Figure 5-2a, size 50×160 mm equal to 320 (5×5) mm squares, has a capacitance between the top and bottom copper sheets of 200 pF. The dielectric is an epoxy-glass plastic with thickness 1.6 mm. The capacitance per mesh is then given by Equation 45. In the SPICE model illustrated in Figure 6-13, this will be the capacitor value connecting each four-inductor junction.

$$C_{mesh} = \frac{20 \cdot 10^{-12}}{320} = 625 \cdot 10^{-15} \text{ F} \quad (45)$$

6.10 Values of the mesh inductors

The inductances on the edges of each mesh can be derived using the propagation delay calculated in Equation 34. This propagation delay can be written in terms of the per-unit-length (PUL) capacitance and inductance of the transmission line forming the PDN. That relation is shown in Equation 46, using the calculated value of $\tau_{PD\text{Patch}}=6.9$ ns/m.

$$\tau_{PD} = \sqrt{\epsilon_0 \cdot \epsilon_{eff} \cdot \mu_0} = \sqrt{L_{PUL} \cdot C_{PUL}} = 6.9 \cdot 10^{-9} \text{ s/m} \quad (46)$$

For Board 11, shown in Figure 5-2a, with the full power plane over a ground plane, the transmission line is a two strip Lecher line with a length of 160 mm. It has 200 pF capacitance. A 1 m line hence would have $C_{PUL}=1.25$ nF/m of capacitance. Then, from Equation 46, the PUL inductance of this line can be calculated as shown in Equation 47.

$$L_{PUL} = \frac{\tau_{PD}^2}{C_{PUL}} = 38 \cdot 10^{-9} \text{ H/m} \quad (47)$$

This is the inductance of 1 m of a 50 mm wide strip of PCB material, clad with copper on both sides and short circuited on one of the short sides. The inductance could be measured between the copper foils ends on the – other - short side as shown in Figure 6-6. This will now be translated into edge inductances of the meshes. The 50 mm PCB strip has 10 parallel rows of 5 mm meshes. Considering

the edges of these meshes only, 11 parallel conductors running along the topside of a strip of 1.6 mm thick epoxy-glass, bent around the end of the strip and then back along the bottom side [103]. See Figure 6-16. The inductance of these 11 wires in parallel is the inductance calculated in Equation 47. This means the inductance of one single wire is 11 times that value: $L_{single\ wire} = 418\text{ nH}$. Considering the mesh size of 5 mm, the individual (partial) inductance on each mesh edge is calculated shown in Equation 48.

$$L_{mesh} = \frac{0.005}{2} \cdot 418 \cdot 10^{-9} = 1.1 \cdot 10^{-9}\text{ H} \quad (48)$$

Using the same propagation delay in the perpendicular direction over the width of the copper sheet produces the same inductance for all four mesh edges on either side of the strip i.e. applicable for the power patches as well as the ground plane

Figure 6-15 Measurement of line inductance (dielectric removed for clarity)

Figure 6-16 Power Plane and PDN seen as Reussenleiter

6.11 Traces modeled as surface micro-striplines

The approach for the sectioning of traces is the same. The relevant measures in addition to the dielectric permittivity, $\epsilon_{effTrace}$, of the insulating layer in the micro-stripline configuration are shown in Figure 6-17. The height of the trace over the ground plane, d is shown. Additional equations for the calculation of the surface micro-stripline PUL trace parameters are also found in [104]. As for the patches, first the effective relative dielectric constant is calculated from Equation 40.

With the value of $\epsilon_{effTrace}$, the propagation delay for the surface micro-stripline can be found from Equation 34. In contrast with the approach for the patches, the characteristic impedance, Z_0 , of the micro-stripline is used to determine the capacitances and partial inductances for each section of the line.

Figure 6-17 The dimensions of micro-striplines

As the trace width (2.7 mm) is less than the selected mesh size, the micro-stripline is modeled in SPICE using a single row of mesh inductances in series grounded to the underlying ground plane via capacitances as illustrated in Figure 6-9. The characteristic impedance of a loss-less transmission line can be expressed in the PUL inductance and capacitance of that line as shown in Equation 49.

$$Z_0 = \sqrt{\frac{L_{PUL}}{C_{PUL}}} \quad (49)$$

The characteristic impedance of the surface micro-stripline according to [104] is given by Equation 46 if $W_p < d$. In other cases, Equation 47 should be used.

$$Z_{0(\text{micro})} = \frac{60}{\sqrt{\epsilon_{\text{eff}}}} \cdot \ln\left(\frac{8 \cdot d}{W_p} + \frac{W_p}{4 \cdot d}\right) \quad (50)$$

$$Z_{0(\text{micro})} = \frac{\frac{120 \cdot \pi}{\sqrt{\epsilon_{\text{eff}}}}}{\left[\frac{W_p}{d} + 1.3 + \frac{2}{3} \cdot \ln\left(\frac{W_p}{d} + 1.4\right)\right]} \quad (51)$$

Given equations for the propagation delay, $\tau_{PD(\text{micro})}$ and characteristic impedance, $Z_{0(\text{micro})}$, the PUL capacitance and inductance can now be derived from Equations 46- and 50 as shown in Equations 52 and 53.

$$C_{PUL\text{microstrip}} = \frac{\tau_{PD(\text{micro})}}{Z_{0(\text{micro})}} \quad (52)$$

$$L_{PUL\text{microstrip}} = \tau_{PD(\text{micro})} \cdot Z_{0(\text{micro})} \quad (53)$$

With the dimensions for the traces, $d=2.7$ mm the effective permittivity is found as $\epsilon_{\text{effTrace}}=3.4$. The propagation delay from Equation 46 is $\tau_{PD(\text{micro})}=6.1 \cdot 10^{-9}$ s/m. This implies the propagation delay is a bit smaller and consequently the smallest wavelength longer. The sections for the trace could be chosen larger in that case than the value calculated for the patches. But the traces run over the ground reference plane which is also meshed with the same sides of $S=5$ mm as the patches. For the model the trace is therefore broken up in sections of 5 mm so they will match up with the meshing in the ground reference plane. The characteristic impedance of the traces are found from Equation 50 as $Z_{0(\text{micro})}=53\Omega$. With these parameters, the PUL capacitance and inductance are found as (54).

$$C_{PUL(\text{micro})} = 1.16 \cdot 10^{-10} \text{ F/m} \quad (54)$$

$$L_{PUL(\text{micro})} = 3.26 \cdot 10^{-7} \text{ H/m}$$

The 5 mm trace sections will have $C_{5\text{mm}}=5.8 \cdot 10^{-12}$ F and $L_{5\text{mm}}=1.6 \cdot 10^{-8}$ H respectively.

6.12 SPICE models for the active boards

All prerequisites for the SPICE modeling are available now. Two aspects must be checked:

1. Power Integrity (PI), for the system to work at all
2. The CM noise generation of the chosen segmented power structure

In this section the CM noise generation of Board 13 in Figure 5-2c, with two 50×50 mm power islands are simulated and compared to Board 11 in Figure 5-2a with a

full power plane. Measurements have also been performed on the actual hardware as reported in previous chapter. These will be included in the comparison for validation of the SPICE model.

6.13 Configuring the SPICE models for PI analyses

Power integrity (PI) requires the power supply of each active device to be within the specified tolerances at all times. This implies the analysis must be performed in the time domain. The PI of the ACT11244 bus-driver circuit is analyzed. The specification [105] provides 4.5 to 5.5 V as the recommended operating condition. To monitor it in the SPICE model, the differential mode supply voltage of the bus driver chip must be monitored. For that purpose the return pins of the ACT11244 are connected to the SPICE ground symbol which is the 0 V reference with respect to which all voltages are measured. The available SPICE voltage probe can then be attached to the supply voltage point i.e. the VCC pins of the device, to monitor the voltage over the power pins during operation. In the model the output of the linear voltage regulator, the 7805, is modeled as a plain DC voltage source of 5 V, regardless of the load current. The active hardware is represented by the circuit of Figure 6-6. Parallel to this load are two 10 nF decoupling capacitors including the parasitics derived before. As it was mentioned before, the LTSPICE tool was used to simulate the SPICE model. The resulting SPICE model for full power plane Board 11 is shown in Figure 6-17 while the model for Board 13 with two separate power islands of 50×50 mm connected by a trace is shown in Figure 6-18. The voltage over the load (i.e. on the ACT11244 power pins) is shown in Figure 6-18. The simulation returns identical results for these two PI measurements as resistances in traces and planes are not modeled and no $I \times R$ losses occur. For PI, the boards are identical. It is clear from Figure 6-20 that the decoupling is marginally sufficient. This is acceptable here as the recommended operating conditions are not an absolute limit.

Figure 6-18 SPICE bedspring model for Board 11 (Figure 5-2a) PI noise measurement

Figure 6-19 SPICE bedspring model for Board 13 (Figure 5-2d) PI noise measurement

6.14 Configuring the SPICE models for CM noise analyses

To analyze the CM noise generated by the two boards in the Time Domain (TD) or Frequency Domain (FD), the voltage between the two extremities in the middle of the left and right hand sides on the ground plane in Figure 5-2a and Figure 5-2d is measured. In real life, these measurements are performed using a special brass fixture with an N-type connector on one side and a touching brass stripe on the other as shown in Figure 5-6. The boards are placed across the gap between the ridge and the N-type connector as shown in Figure 6-21 and Figure 6-22.

6.15 LTSPICE CM noise analyses in the time domain

In the LTSPICE model, the midpoint of the ground plane at the left-hand side in Figure 6.3 and 6.4 is connected to the LTSPICE ground symbol (0 V). The voltage at the midpoint of the ground plane at the right hand side is measured. The 5 V DC power source and the non-linear load and decoupling capacitors remain in place. Note that measurements are across the ground plane, i.e. in longitudinal direction. These points are visible in Figure 6-24 and Figure 6-25. The CM noise voltages, simulated over the length of the boards in the time domain are shown in Figure 6-26 and Figure 6-27 respectively.

6.16 LTSPICE CM noise analyses in the frequency domain

Analyses in the FD can be performed with these same models if the spectral noise generated by the active circuitry is modeled adequately, and neglecting the effects due to the non-linearity of the active components. As a simple demonstration, the voltage source, used for the TD model of the ACT11244 circuit, can be replaced with a 5 V white noise source in series with a fixed 10 Ω resistor and the same 408 pF capacitor. The maximum current generated will then still be 450 mA. This way, the high frequencies will be over-estimated but specific resonances can be observed. The SPICE models is shown in Figure 6-28 and Figure 6-29 for Board 11 and 13 respectively. The resulting CM noise voltage spectra over the board's ground planes are shown in Figure 6-30 and Figure 6-31. The analysis is performed up to 1 GHz.

Figure 6-20 DM noise voltage between the ACT11244 power pins, as function of time, for Board 11 and Board 13 (Power Integrity, (PI))

Figure 6-21 Test set-up for measuring the CM noise voltage developed in the ground plane of the tested boards

Figure 6-22 Test set-up for measuring the CM noise voltage developed in the ground plane of Board 11

Figure 6-23 Test set-up for measuring the CM noise voltage developed in the ground plane of Board 13

Figure 6-24 SPICE bedspring model for Board 11 (Figure 5-2a) CM noise measurement in the time domain

Figure 6-25 SPICE bedspring model for Board 13 (Figure 5-2d) CM noise measurement in the time domain

Figure 6-26 CM noise voltage in Board 11 (Figure 5-2a) in the time domain

Figure 6-27 CM noise voltage in Board 13 (Figure 5-2c) in the time domain

Figure 6-28 SPICE bedspring model for Board 11 (Figure 5-2a) CM noise measurement in the frequency-domain

Figure 6-29 SPICE bedspring model for Board 13 (Figure 5-2c) CM noise measurement in the frequency domain

Figure 6-30 CM noise voltage in Board 11 (Figure 5-2a) in the frequency domain

Figure 6-31 CM noise voltage in Board 13 (Figure 5-2c) in the frequency domain

6.17 Frequency domain simulations compared to measurements

All models are abstractions of the real world. Only the essential elements are preserved and the rest is ignored. In the SPICE models of these active boards the following remarks are in place:

1. All mesh inductors are identical in the ground plane, the power plane and the 50×50 mm power patches. This implies that no edge effects are modeled.
2. The measurement points of the ground plane CM noise voltages are the centers of the ground plane at the extreme edges of the board. In the actual measurements there is some uncertainty at the brass reference plane connection ridge and at the N-type connector. At the ridge, the connection could be made somewhere between the board edges, not exactly in the middle. The ridge and N-type center pin extend for about 5 mm over the GRP. Here too an uncertainty exists about the exact connection point.
3. The frequency domain source spectrum at the ACT11244 is modeled as a white noise source with a fixed amplitude over the frequency range. This source has been given a fixed, 10 Ω internal resistance.
4. The copper conductors in both layers of the example PCBs are modeled with ideal inductors only. The simulated results near DC therefore lack any I^2R losses i.e. are too low. A similar remark can be made for the frequencies in the GHz ranges: the pure capacitors used between the copper layers may have to be shunted by resistors modeling the dielectric losses.

6.18 Actual measurement results for comparison

The results of actual measurements on the active Boards 11 and 13 of Figure 5-2 are shown in Figure 6-32. These measurements were reported in Chapter 5. The relevant are the red trace (plane) and the green trace (two single cell EBG structure). Both in measurements and in simulations two single-cell EBG structure show less noisier behavior.

Figure 6-32 Measurements: Boards 11 and 13 compared in the frequency domain

6.19 Summary

The EBG structures can be modeled and simulated in electromagnetic tools such as Microwave Studio from CST. However, non-linear active components are not easily modeled in those EM tools. Several options are available. In this chapter two single-cell EBG board have been converted into SPICE-bedspring models, and their behavior has been simulated. In the time domain, adequate power integrity is demonstrated before common mode analyses can be reasonably made. The CM simulation is performed in the time domain and frequency domain. Two boards, Board 11 and Board 13 shown in Figure 5-2a and 5-2c, were. The PI simulation shows the decoupling used for the ACT11244 bus driver is adequate. The frequency domain CM noise results simulated in LTSPICE are compared to actual frequency domain measurements performed earlier. There is a good match in general behavior of the boards comparing simulations with measurements.

7. Miniaturization of EBG structures using embedded capacitance material

High capacitance materials as PCB substrate to reduce EMI have been investigated. The objective is to investigate the effect of embedded capacitance material on the size reduction of EBG structures etched on a power plane and its filtering performance. Due to the high permittivity of the embedded material and the smaller separation distance between the power and ground conductors, the effective band shifts to much lower frequencies. The effect of EBG on high capacitance material on common mode radiation was evaluated.

7.1 Introduction

As it was already mentioned in Chapter 3, due to velocity of propagation of electromagnetic energy v , capacitance of PCB substrate is used locally to IC and is limited by the effective decoupling radius r :

$$r = vt = \frac{3 \cdot 10^8 \cdot t}{\sqrt{\epsilon_{\text{reff}} \mu_{\text{reff}}}} \text{ m} \quad (3)$$

Where r is effective decoupling radius, t is time required to move charge in nanoseconds, ϵ_{reff} is the effective relative dielectric permittivity and μ_{reff} is the magnetic permeability of the medium through which the wave is propagating. The effective decoupling radius can be reduced by using special material with high permittivity.

Commonly, FR4 is used as a PCB substrate for economical and mechanical reasons. A FR4 substrate consist of a woven fiberglass cloth, filled with epoxy resin: a composite, non-homogeneous, material. The dielectric permittivity of FR4 substrates is often not guaranteed, and only typical values are given by manufacturers. Moreover, it is degrading with frequency [106]. The Restriction of Hazardous Substance (RoHS) directive [107] restricts since 2006 the concentration levels of some chemical substances. In the PCB manufacturing process, the design components that affects RoHS compliance are the laminate, final finish selection, solder mask and legend ink. Due to this restriction producers of PCB substrates limit restricted materials to justified level and at the same time they try to adjust manufacturing process because PCB has to survive a higher temperature assembly

and rework process [108], [109]. There is a strong need in application of new materials in PCB process and accurate characterization of them.

7.2 Classification of measurement techniques

Electromagnetic characteristics of material are dependent on the dielectric properties. Accurate measurements of these properties can provide scientists and engineers with valuable information to properly incorporate the material into its intended application. Complex dielectric permittivity (ϵ), also termed the dielectric constant, describes the interaction of a material with an electric field. The dielectric constant (k) is equivalent to relative dielectric permittivity (ϵ_r) or the absolute dielectric permittivity (ϵ) relative to the permittivity of free space (ϵ_0). The real part of complex relative dielectric permittivity ϵ_r' is a measure of how much energy from an external field is stored in a material; the imaginary part of complex relative dielectric permittivity ϵ_r'' is called the loss factor and is a measure of how dissipative or lossy the material is to an external field [110].

$$k = \frac{\epsilon}{\epsilon_0} = \epsilon_r = \epsilon_r' - j\epsilon_r'' \quad (55)$$

However, the dielectric “constant” is constant neither over frequency nor temperature. The relative lossiness of a material is the ratio of the energy lost to the energy stored and is termed tangent loss. To measure these parameters several national and international standards are used such as:

1. ASTM (American Society for Testing and Materials) Standards;
2. NIST (National Institute of Standards and Technology) Technical notes;
3. IPC (Institute for Interconnecting and Packaging Electronic Circuits);
4. Notes of The National Physical Laboratory (NPL), the UK's National Measurement Institute;
5. Russian national standards;

Usually the choice of techniques depends on such factors as the frequency of interest, the expected value of ϵ_r , the required measurement accuracy, material properties (i.e., homogeneous, isotropic), the material form (i.e., liquid, powder, solid, sheet), sample size restrictions, destructive or non-destructive, contacting or non-contacting and temperature. There is a big variety of measuring methods: capacitance method, coaxial probe, resonant cavity, transmission line and free space methods. Figure 7-1 represents a summary of measuring techniques.

Figure 7-1 Summary of techniques

The coaxial probe method uses an open ended coaxial probe, usually with a network analyzer. This method is mostly used for liquids, or soft semi-solids, although very flat hard solids can be measured as well. The method is applied for measurements in the RF to microwave frequencies, 200MHz to 50GHz.

The transmission line method applies a variety of transmission lines for sample holders with a network analyzer. It can be coaxial, waveguide and free-space. It is useful for a broad frequency range, from the low microwave region to mm-wave.

The resonant cavity method uses a resonant cavity for the sample holder, and a network analyzer to measure the resonant frequency and quality factor Q of the cavity, both empty and with the sample present. From this, the dielectric permittivity can be calculated. This method has the best loss factor resolution. Open resonator is using the same principle but in a different frequency range.

The capacitance method uses a parallel plate capacitor, with the material sandwiched between. This method uses an impedance analyzer. It is typically used at the lower frequencies, below 1 GHz.

The transmission line method for low frequency band requires large size of the material sample. For the coaxial probe technique the sample should be precisely machined. Therefore for the frequency band of our interest, less than 5 GHz, the most suitable measurement techniques are the parallel plate method and the free-space method.

7.3 Measurements of dielectric permittivity of high capacitance material

As it was mentioned before, most EBG are mitigating noise in a limited bandwidth, mainly in the high MHz and GHz range. To improve the filtering performance of EBG without increasing the size of the structure, EBG on high capacitance substrate were manufactured. Thin sheet of 3M™ Embedded Capacitor Material C1012 [111], [112] was used as substrate for EBG design. It is a copper-clad laminate which utilizes an ultra-thin, high permittivity dielectric material between the copper planes. The dielectric permittivity of this substrate was measured using parallel plate capacitor method. The measurement setup is shown on Figure 7-2. Parallel plate capacitor system uses a parallel plate capacitor as a sample holder, with the material under the test sandwiched between. This method requires an impedance analyzer or LCR meter. The material is stimulated by an AC source and the actual voltage across the material is monitored.

Figure 7-2 Measurement setup

The material test parameters are derived by knowing the dimensions of the material and by measuring its capacitance and dissipation factor using Equations

$$\epsilon_r' = \frac{C}{\epsilon_0 \frac{A}{t}} \quad (56)$$

$$\tan \delta = D \quad (57)$$

$$\varepsilon_r'' = \varepsilon_r' \times D \quad (58)$$

Here C is an equivalent parallel capacitance of the Material Under Test (MUT) [F], D is the dissipation factor (measured value), t is an average thickness of the MUT [m], A is the surface area of guarded electrode [m²], ε_0 dielectric permittivity of free space = 8.854×10^{-12} [F/m]. In our case, $d=12.8$ mm, $t=12$ μ m.

After putting a sample into a sample holder, a capacitor is formed. This method uses a wide frequency range from 20 Hz to 1 GHz, has high measurement accuracy and involves very simple sample preparation and setup. Typically $\pm 1\%$ for ε_r' and $5\% \pm 0.005$ for loss tangent.

Figure 7-3 Real part of the dielectric permittivity (ε') of 3M material

Figure 7-3 and Figure 7-4 show the real (ε_r') and imaginary (ε_r'') part of the dielectric permittivity (ε') of 3M material in the frequency range 10 kHz - 1 GHz. It is almost 4 times higher than dielectric permittivity of standard FR4 material. This material is therefore often used to perform a power supply decoupling function.

Figure 7-4 Imaginary part of the dielectric permittivity (ϵ'') of 3M material

7.4 EBG structure on high capacitance material

Four experimental boards, shown in Figure 7-5, were designed to demonstrate the influence of the substrate material, shape, length, inductance of interconnecting line, size and capacitance of patches on resonances in power plane and common mode radiation. Board 5 and 6 were described in Chapter 3, Section 3.7. They were designed on EURO-card printed circuit boards ($100 \times 160 \text{ mm}^2$). The dielectric of the PCB was FR4 with relative dielectric constant of 4.5. Board 15 and 16 were designed on embedded capacitor material with dielectric constant of approximately 22, which is almost 4 times higher than dielectric permittivity of FR4 material. Board 6 and 15 had the same design configuration. The first structure (Board 6-a) represents a conventional power plane which mirrors the ground plane creating a cavity. The geometries of three other structures on Board 6-b-c-d and Board 5- b-c-d were as follows. The size of each individual patch was $30 \times 30 \text{ mm}^2$. Inductance of meander for the case 6-b) and 5-b) is 453 nH, EBG fragments 6-c), 5-c), 6-d), 5-d) have equal inductance of the interconnecting trace which is 325 nH. All interconnecting traces were 0.5 mm wide.

Figure 7-5 Set of EBG structures etched on FR4 substrates a) Board 6, b) Board 5, and on high capacitance material Board 15, and Board 16.

Board 5 and 16 were designed to estimate the influence of the size of individual patch of EBG on radiated emission. These 2 boards also had the same design configuration. Dimensions of patches for each EBG are listed in Table 3-2. All interconnection power traces were 0.5 mm wide and 35 mm long. The transmission coefficient of the boards shown in Figure 7-5 was measured and plotted in Figure 7-6 and Figure 7-7. The graph demonstrate that the EBG reduces resonances in the PDN. Significant noise reduction is achieved by combination of EBG and high capacitance substrate in comparison with Board 6a, the standard power plane. Measurement results of S_{21} of the board with different size of the patches are plotted on Figure 7-7 which demonstrates that EBG etched on high dielectric material show better performance at low frequencies. The EBG with the smallest patch size (5x5mm) etched on high capacitance substrate shows 5 dB better attenuation than EBG on FR4 (30x30).

Figure 7-6 S_{21} of EBG with different power traces on FR4 and high-k, Board 6 and Board 15

Figure 7-7 S_{21} of EBG with different patches on FR4 and high capacitance material and FR4 substrates Board 5 and Board 16

This demonstrates that the combination of EBG structure and embedded capacitance material could be used to suppress PDN noise in high speed electronics.

7.5 Summary

The noise reduction effect of different variations of Electromagnetic Band Gap structures (EBG) using different dielectric materials was analyzed. The high capacitance material can be used as a substrate to miniaturize the EBG structures. Moreover a combination of EBG and high capacitance embedded material substrate leads to better filtering performance of EBG at lower frequencies. The Power Distribution Network (PDN) employing EBG showed behavior of a low pass filter, and reducing unwanted resonances. Almost 60 dB in noise reduction was achieved implementing EBG on high-permittivity substrate compared to conventional power plane design.

8. Conclusions

This thesis presents the investigations how to mitigate noise and reduce EMI by means of structuring the power plane of PCBs as Electromagnetic Band Gap (EBG) Structures. Therefore a general example of Power Distribution Network (PDN) is described. The mechanism of noise generation and propagation in the PDN is introduced. It is discussed that due to the symmetric shape of power and ground planes, the traditional PDN forms an unterminated waveguide which resonates at high frequencies. At these frequencies the PDN has large impedances which leads to voltage fluctuations either generating edge-radiation or creates common currents towards the connected devices. The resonance frequency of a PDN is determined by the mode number, the dielectric constant of the insulator and the physical size of the planes. Various existing methods to reduce this noise are considered. The main drawbacks of these methods and the need for a new approach to reduce PDN noise are addressed.

There is a raising interest in applying EBG structures to reduce simultaneous switching noise. EBGs are siblings of a more general application of various repeating metallic structures in dielectric media that have attractive electrical properties and are known as metamaterials. Therefore, a general introduction to metamaterials and EBG in particular is given. The concept of EBG structures and their use in PDNs was analysed. The main limitation of EBG is its limited bandwidth in noise suppression, the complexity and manufacturing cost. The traditional EBG is a band-pass, or band-stop, filter. Combinations of conductive patches interconnected by thin traces over a wide metallic ground plane create this behavior. Simplifying, these can be modeled as capacitors and inductors creating a multi section filter. The novel application in this thesis is to form an essentially low-pass behavior that can be applied to PDNs. Metallic, usually copper, patches over a ground plane are considered as capacitors and these capacitors are interconnected by relatively thin copper traces that behave as small inductances. With the traditional PCB materials, the patch capacitance per surface area is not sufficient for power supply decoupling and discrete capacitance must be added. Due to the finite velocity of propagation, charge needed to satisfy a sudden local current surge can only be

reached when located within a finite radius from the devices being supplied, called effective decoupling radius. Based on this concept, the new planar EBG structure consisting of power patches interconnected with thin power traces is proposed. The realization and the characterization of an EBG structure consisting of two single cells, or patches, are performed. The transmission coefficient S_{21} of this structure has been measured using a vector network analyzer in the frequency range 10 MHz – 3 GHz. The proposed EBG structure shows the behaviour of a low pass filter reducing unwanted resonances of the PDN. The achieved noise isolation between 2 ports is more than - 20 dB over a large frequency band.

Reducing the high frequency currents on the PDN inherently reduces their conversion into common mode (CM) currents through the PDN transfer-impedance. The measurements of CM current performed with a current clamp showed that these currents on a cable connected to the board with two single-cell EBGs is almost 20 dB less than in the case of a traditional PDN built as a symmetric power plane-ground plane combination.

To verify the influence of cell/patch parameters on noise isolation, several variations of EBG structures with different patch sizes and different shapes and lengths of interconnecting traces were designed. Based on the measurements of transmission coefficient, the conclusion is drawn that the size of the patch defines the resonant frequency of the structure, the longer power trace, meandering between the patches, results in a more resonant behaviour of the structure forming additional coupling between parts of the meander. A two single-cell EBG structure interconnected with a thin straight power trace shows the lowest transmission coefficient. The exact position of the power trace is not very important which gives flexibility for the design engineer. The analysis of the basic EBG cell is performed by means of a transmission (*ABCD*) matrix. To analyze the onset and bandwidth of the stopbands of EBG, its dispersion diagram was calculated using one unit cell. The calculated stopband matches very well with measured transmission coefficient S_{21} .

EBGs have been conventionally developed to create a stop band for one specific frequency by using a series of similar shaped cells. In order to find the influence of the amount of EBG cells on the suppression band, CST simulations of one-, two-, three- and four-unit cell EBG structures were performed. It is proven that one-cell EBG structures and the EBG with multiple cells have the same suppression bands. The stopbands and passbands depend only on the design of the EBG unit cell and is not influenced by the number of cells. It is possible to achieve good noise isolation using an EBG with only a limited number of cells. Based on this conclusion, several

design strategies of EBGs with broader suppression band are suggested. A novel concept for ultra-wide-bandwidth suppression of PDN noise is proposed and implemented. This method consists of applying EBG cells with different stop bands creating noise isolation over a wide frequency range. It is proven that combining several EBG structures with different stopbands with some periodicity will lead to the overall performance of the structure similar to a low pass filter with a stopband equivalent to the superposition of the original individual filters. Every patch has a different dimension and resonant frequency. The noisy modules can be isolated by being placed on individual EBG cells. Several experimental boards with power planes patterned by these EBG structures and solid ground planes, as reference, were manufactured and their transmission coefficient was measured. The measured transmission coefficient S_{21} showed that using varying size power patches is very efficient in a broad frequency range.

To verify the proposed concept in a real design, four boards with active components were manufactured. The effect of the geometry of the PDN on the common mode noise generated by the board into its environment is investigated. The effect of the power plane, power track, two single-cell EBG and EBG with different cell sizes on the noise reduction in printed circuit boards with active components is investigated.

To evaluate the effect of the described power isolation concepts on the noise reduction of the PCB, the longitudinal noise voltage of the boards was measured. Using a power trace instead of a power plane can decrease the noise voltage between 5 and 15 dB. Two single-cell EBG shows a large reduction of the noise voltage up to 500 MHz. At higher frequencies the effect is lost due to the crosstalk between the islands. A board with different cell sizes was used creating a wider band suppression of the noise. This board shows the largest effect on noise reduction. To exclude the local, differential mode switch current fields from contributing to the boards emissions, the noisy part of the board was shielded with a metal shield, and measurements of the noise voltage generated over the ground plane were performed. To evaluate the effect of EBG on radiated emission, electromagnetic fields were measured in a reverberation chamber. The performed measurements prove that all 3 solutions are more effective in decreasing the noise voltage compared to the version with the full power plane. The creation of the multi-patched EBG showed to be effective also on the radiated emission of the PCBs with active components.

Near field noise measurements of the boards were performed with an EMxpert XY nearfield scanner.

An equivalent circuit of an active board on two single-cell EBG and with the full power plane PDN was created with a SPICE circuit simulator, because an electromagnetic field simulator cannot easily deal with non-linear active components. The model was compared with measurements of the longitudinal noise. Measurements and simulations showed good agreement. This indicates that a SPICE model can be a good starting point to evaluate the effects of a chosen design before it is actually built.

To decrease the size of an EBG structure some experiments with a high capacitance substrate were performed. First, the material characterization of the substrate and dielectric permittivity measurement techniques are discussed. The substrate was measured using parallel plate capacitor technique and had a relative dielectric permittivity of 22, which corresponds to manufacturers datasheet. Several EBG patterned PDNs were etched on this substrate and its transmission coefficient was measured and compared with the same EBG on standard epoxy-glass FR4 substrate. The combination of EBG and high capacitance embedded material substrate leads to better filtering performance of EBG at lower frequencies. Almost 60 dB difference in noise reduction was achieved implementing EBG on high-permittivity substrate compared to conventional power plane design. A disadvantage of the thin high-epsilon substrate material is that it cannot be used for additional data traces as the characteristic impedance of such lines would be prohibitively low.

Suggestions for future research, impact on society of the work presented in this thesis and design guidelines are given in the last chapter of the thesis.

9. Design guidelines and recommendation for future work

Based on the filter theory and the fact that EBG behaves like a band-stop filter, it was proven that combining several EBG structures with different stopbands with some periodicity will lead to the overall performance of the total structure similar to low pass filter with a stopband equivalent to the superposition of the original individual filters. Each stage of the filter is formed by an independent EBG unit cell. First of all the PCB designer needs to discover noisy components that need to be placed together to form the *coherent modules* already in the schematic diagram phase. Each of these modules can be isolated by being placed on a separate individual EBG unit cell. This has to be done during the lay-out phase to separate them from other modules to achieve an end result with loosely coupled coherent modules. The analysis of EBG unit cells was discussed in Chapter 3. Each EBG unit cell consists of a rectangular patch and a thin interconnecting trace. Every patch has a different dimension and resonant frequency. Each of these resonant frequencies correspond to low transmission. The power plane is patterned by these EBG structures and the ground plane has to be kept solid because any slits in the ground plane increase EMI. The practical PCB designer will have a number of cells equal to his number of coherent modules. So it is usually not a designable parameter. The size of the patches is determined by the active hardware in the module built on it and it needs to be larger than the effective decoupling radius. The effective decoupling radius can be reduced by using special material with high permittivity. Full-wave simulations can be used to validate the design before fabrication.

Figure 9-1 represents the schematic diagram of design procedure. The equivalent circuit model using SPICE, as proposed in Chapter 6, can be used to verify the design.

Figure 9-1 Schematic of design procedure

Further research can be done in improving the equivalent circuit model of active components. The combination of EBG and new materials including nanotechnology is promising research direction.

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Appendix A: List of acronyms

CM	Common-Mode
GRP	Ground Reference Plane
IC	Integrated Circuit
IRS	International Roadmap on Semiconductors
EBG	Electromagnetic Bandgap
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
PCB	Printed Circuit Board
PDN	Power Distribution Network
PEEC	Partial Element Equivalent Circuit
PI	Power Integrity
PUL	Per Unit Length
RF	Radio Frequency
SI	Signal Integrity
SSN	Simultaneous Switching Noise
VRM	Voltage Regulator Modules

Appendix B: List of the designed boards

Board 1
Board 2
Board 3

Board 4
Board 5
Board 6
Board 7
Board 8
Board 9

Board 10
Board 11
Board 12
Board 13
Board 14
Board 15
Board 16

Appendix C. Some discussions of Chapter 4 and 6.

Figure 4-1 of one unit cell EBG can be interpreted as having the topology of a T filter shown on Figure C-1.

Figure C--1 Topology of 1 unit cell EBG

The circuit of Figure 4-3 is the “PI” filter below:

Figure C--2 Topology of 2 unit cell EBG

These simple lumped element models can be easily LTSPICEd:

a)

Figure C--3 Equivalent circuit model of

- a) 1 unit cell EBG
- b) 2 unit cell EBG
- c) 3 unit cell EBG

These SPICE models can be run and the low frequency pass band is easily recognized in comparison to the figures. Red (solid) is Figure C3-a, blue is Figure C3-b and green is Figure C3-c.

First, second and third order behavior. By chopping up the patches and traces in smaller sections the model can be made to approach the real simulation models.

Addition of decoupling capacitors

As suggested in the LTSPICE simulations of the active boards, the EBG structures discussed here will never be used without additional discrete decoupling capacitors, and at least 20 nF per power island is needed. If these capacitors would be added in the SPICE models above, the schematic diagrams shown below can be created. Notice that a 50 Ω source impedance is not so realistic in that case. The source is 1 Ω and the load to 10 Ω .

Figure C3--a (modified)

Figure C3--b (modified)

Figure C3--c (modified)

The resulting transmission coefficient S_{12} :

The cut-off frequencies are much lower. The higher frequency pass bands are no doubt the result of parasitic capacitances between the patches. These are still present but do not change with respect to the situation without the decoupling capacitors. In theory the decoupling capacitors in the CST simulations can be added in future research.

List of publications

- 1 O.V.Tereshchenko, F.J.K. Buesink, F.B.J. Leferink 'Measurement of Complex Permittivity of Composite Materials using Waveguide Method', *EMC Europe 2011*, York, UK, September 26-30, 2011.
- 2 O.V.Tereshchenko, F.J.K. Buesink, F.B.J. Leferink 'An overview of the techniques for measuring the dielectric properties of materials', *XXX URSI General Assembly and Scientific Symposium of International Union of Radio Science*, Istanbul, Turkey, August 13-20, 2011.
- 3 O.V.Tereshchenko, F.J.K. Buesink, F.B.J. Leferink (2012) 'Reduction of power plane resonances using EBG structures to decrease common mode current', *IEEE 2012 Asia-Pacific International Symposium on Electromagnetic Compatibility*, Singapore, May 21-24, 2012.
- 4 O.V.Tereshchenko, F.J.K. Buesink, F.B.J. Leferink 'EBG structures on high permittivity substrate to reduce noise in power distribution networks', *2012 IEEE International Symposium on EMC*, Pittsburgh, PA, USA, August 5-10, 2012, *Nominated for 'Best Student Paper Award'*.
- 5 O.V.Tereshchenko, F.J.K. Buesink, F.B.J. Leferink 'Miniaturization of EBG structures using embedded capacitance material', *EMC Europe 2012*, Rome, Italy, September 17-21, 2012.
- 6 O.V.Tereshchenko, F.J.K. Buesink, F.B.J. Leferink 'EBG Structures on High-k Substrate as a Common Mode Radiation Suppressor', *URSI Benelux Forum*, Brussels, Belgium, 14 September, 'Best Poster Award'.
- 7 O.V.Tereshchenko, F.J.K. Buesink, F.B.J. Leferink 'Power isolation strategies to reduce PDN Noise', *IEEE 2013 Asia-Pacific International Symposium on EMC*, Melbourne, Australia, May 20-23 2013.
- 8 O.V.Tereshchenko, F.J.K. Buesink, F.B.J. Leferink 'Wide-band segmented power distribution networks', *Proceedings of the 2013 International Symposium on Electromagnetic Compatibility (EMC Europe)*, Brugge, Belgium, September 2-6 2013.
- 9 O.V.Tereshchenko, F.J.K. Buesink, F.B.J. Leferink, 'Radiated emission of various PDN designs', *EMC 2014/Tokyo*, May 13-16, 2014.
- 10 S. Op 't Land, O.V.Tereshchenko, M. Ramdani, F.B.J. Leferink and R. Perdriau 'Printed Circuit Board Permittivity Measurement Using Waveguide and Resonator Rings', *EMC 2014/Tokyo*, May 13-16, 2014.
- 11 O.V. Tereshchenko, F.J.K. Buesink and F.B.J. Leferink, 'Effect of PDN variations of PCB with active components on unwanted emission', *EMC Europe 2014*, Gothenburg, Sweden, September 1-4, 2014.

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Biography

Olga Tereshchenko was born on January 29th in Dnipropetrovsk, Ukraine in 1986. She received her Bachelor degree in Electrical Engineering in 2006. She graduated with the Master in Power management (cum laude) from the National Mining University in Dnepropetrovsk, Ukraine

As part of her study she was participating in exchange program in Brandenburgischen Technischen Universität, Cottbus, Germany starting on November 2006 till February 2007.

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Her research interests are in electromagnetic modeling, EBG structures, electromagnetic integration, system integration and EMI countermeasures in electronics.