Integration of Reliability- & Tolerance Effect Analysis.

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ABSTRACT.

This paper focuses on the development of systems with so called on-line optimized reliability. In case of on-line analysis reliability analysis should have the same importance as functional analysis is having now. Reliability should be integrated in a design. The function of a quality assurance team is only to check this built-in reliability. Not to make a functional correct design also reliable [1]. Therefore the designer (or design team) should be able to perform reliability analysis during the system synthesis.

Although conventional failure rate prediction using, for example MIL-HDBK-217 [2] methods, proof to be very useful there are often considerable numbers of failures due to "unexpected" causes. Analysis of these failures shows that a considerable group of these "unexpected" failures is due to a combination of tolerance effects and part (over-) stress. This paper describes a method to predict these failures. Research was carried out in close cooperation with Philips Industries, the Netherlands to verify the predicted results.

INTRODUCTION.

One of the most characteristic aspects of the development process of a system is the fact that only in a few cases a design is completed without numerous, often tedious, changes. This is a consequence of the nature of the process of designing. And, as the changes are initiated by numerous causes, they will be introduced in the development process somewhere between preliminary system design and system use.

There is, however, a considerable difference in which phase of the development process the design changes are introduced. In general changes are introduced in the first phases of the development cycle. Changes introduced later do occur but should be avoided due to the great effort required to make changes in an almost completed design. This due to the large amount of parameters involved. The problem, however, will often be that there is quite a difference in one single, working, prototype in a laboratory environment and a large series of systems working according to their specifications for a stated period of time under certain environmental conditions.

Generally speaking there are two methods in use to predict the behavior of a series of systems in a user environment:

- Problem prediction using prediction models and techniques.
- Intensive simulation tests of a series of prototypes.

An advantage of the second method is the fact that, generally speaking, many design weaknesses will be detected. This method, however, will be rather time consuming and tedious. It will require quite a lot of effort to modify an (often) almost completed design. A consequence will be that a lot of interaction between different groups of people is required. (Designers, Quality assurance teams, etc.) As a result solutions will be *added to* and will not be *integrated in* a design. This is called *off-line* optimization.

Theoretical predictions are therefore used to improve the efficiency of the design process. A problem of the use of prediction models is the fact that, generally speaking, not all possible problems will be predicted. Therefore simulation tests will be used for control and verification purposes to find problems not predicted by the first method.

An advantage of the first method is the possibility to perform system optimizations during an early design phase. And, if there are "problem prediction models" available expressing unwanted effects in terms of (electrical) design parameters it is possible that bottlenecks are removed by the designers themselves as an integrated part of the design process. This is called *on-line* optimization. This paper will describe possibilities for on-line optimization taking into account tolerance effects, reliability effects and combined tolerance and reliability effects.

TOLERANCE EFFECTS.

As the main emphasis in on-lined circuit optimization is on circuit optimization performed by the designer himself it is important to define parameters closely related to parameters already in use by the designer. To describe the effects of part tolerances on system level there is a wide range of parameters known in literature. The method adopted here is the use of so-called tolerance sensitivity parameters. [3,4,5]

$$TS_x = \frac{\delta Y(x)}{\delta x}$$

Where: TS_x = Tolerance sensitivity (of signal Y) for (part) parameter x.

Y = circuit signal (such as a node voltage),

x = (part) parameter such as a resistor value.

Using these parameters it is possible to describe the effects of circuit (part) parameter tolerances on signals defined on system level such as output signals. The use of automated tolerance analysis tools to provide sensitivity data will be very useful for a designer to optimize a circuit in respect to the influence of tolerance effects. However, these parameters will not be sufficient to prevent the already mentioned "unexpected" failures. Therefore it is necessary to take also reliability effects into account.

RELIABILITY EFFECTS.

A well known method to predict a circuits (or systems) reliability is given in the United States department of defense handbook MIL-HDBK-217. The MIL-HDBK 217 establishes uniform methods for predicting the reliability of electronic parts and systems. An example of the result of such a MIL-HDBK-217 Part Stress Analysis is given in the figure below.

Figure 1: Failure rate prediction using MIL-HDBK-217.

A disadvantage of the use of failure rate figures is the fact that, although they are very useful as *indicators*, they hardly provide a direct relation with often used design parameters such as voltages, currents, part temperatures, etc. In an on-line optimization process a designer will not only be interested in failure rates but also in the mechanism (or mechanisms) *causing* that failure rate. This is illustrated using the following example:

Given two power resistors with an equal rating but constructed using different technologies. In this case a resistor in accordance with MIL-spec. MIL-R-26 (Code RW: Resistor, Fixed, Wirewound, Power type) and a resistor in accordance with MIL-

spec. MIL-R-11804 (Code RD: Resistor, Fixed, Film, Power type). Figure 2 shows for both resistors the failure rate versus the applied power load.

Figure 2: Failure rate / stress (Code RW & RD resistors)

An important conclusion from figure 2 is the fact that, although the numeric value of the failure rate is of the same order of magnitude the failure rate of the code RW resistor appears to be more sensitive to changes in power load than the code. Thus power derating appears to be more effective for code RW resistors than for code RD resistors. A problem is that many devices, especially more complicated devices such as semiconductors, are subject to many different, correlated, stress mechanisms. Therefore it is not possible to present simple failure rate / load figures such as given in the stated example. To achieve a more comprehensive view of requires introduction of a new set of parameters.

LOAD SENSITIVITY ANALYSIS.

Similar with the sensitivity parameters used for tolerance analysis, giving a direct relation between (tolerance in) a design parameter and the tolerance effect, it is possible to define a set of *load sensitivities*. This load sensitivity, will be defined as:

$$LS_x = \frac{\delta \lambda(x)}{\delta x}$$

Where: LS_x = Failure rate sensitivity (of a part) for stress parameter x.

λ = Part failure rate.

x = stress parameter (such as electrical stress)

Simple (power) load sensitivity relations for the two resistors given in the previous example are given in the figure 3. A major problem in presenting Load Sensitivity figures is the fact that simple relations, such as given in the figure above, often do not exist. As many parts are sensitive to various stresses there will exist more than one LS parameter:

Figure 3: Power load sensitivity versus stress.

LSv: Voltage-load sensitivity.
 LSi: Current-load sensitivity.
 LSp: Power-load sensitivity.
 LSt: Thermal-load sensitivity.

It is important to know that these parameters have a strong correlation. Therefore the parameters should always be presented as a *complete set* of parameters and not as a simple figure such as figure 3 above. The conditions under which these parameters were calculated should also be given.

LOAD SENSITIVITY MODELS.

Normally these Load Sensitivity models are derived (mathematical) from the well known MIL-HDBK-217 failure rate models (or other equally detailed reliability analysis handbooks). Sometimes, however, devices appeared to be sensitive to failure mechanisms not covered in the MIL-HDBK-217. For example High-Voltage transistors appeared to be sensitive not only to the applied collector-emitter voltage and the dissipated power but also to the maximum base current. Therefore in some cases additions and corrections on the sensitivity models derived from the MIL Handbook turned out to be necessary.

At the moment Load Sensitivity models have been verified for most single analogue components and for many of these components the mathematical derivation of the MIL-HDBK-217 formulas turned out to be adequate. Only exception were the semiconductor components where a high dQ/dt occurs (Especially power components). At the moment a preliminary model which takes this effect into account is available but not yet completely verified. After verification these models will be published separately. This paper, however, will use the models derived from MIL-HDBK-217.

Although, at the moment, no models are available for integrated circuits a separate research project will be started in september 1988 to fill this gap. As load sensitivity problems are expected especially for power circuits the first task of this project will

consider integrated power circuits such as driver circuits, power amplifiers, etc.

USE OF LOAD SENSITIVITY ANALYSIS.

Load Sensitivity parameters are particularly useful for designers to be used as parameters in the design process in addition to MIL-HDBK-217 part stress analysis results. For example: for parts with a low LSx value derating on parameter x is hardly useful. For parts with a high LSx, however, considerable improvements can be achieved by means of changing parameter x or by taking another part less sensitive to parameter x. This so-called (*electrical*) *parameter centered derating* is quite a safe and useful method in those situations where there are possibilities to change electrical parameters and/or parts. There are also situations (especially in consumer electronics) where the extra costs of derating (Often "stronger" part = more expensive, derating electrical value x = decreasing system efficiency) should be avoided if possible. In those cases it is important, especially when a parts reliability has (in a certain operating point) a strong sensitivity for a certain electrical parameter, that *unexpected variations* in that electrical parameter do not occur. Therefore parts with a large influence on such a parameter should be given special attention. This can be done using the tolerance sensitivity analysis mentioned previously.

COMBINING TOLERANCE- AND RELIABILITY SENSITIVITY.

Therefore a next step will be to combine tolerance data with reliability data. Combining these figures makes it possible to give combined stress-reliability figures for a circuit. In fact this combination of tolerance sensitivity and stress sensitivity allows prediction of a category of failures which would not have been found using straight reliability or straight tolerance effect predictions. And especially this category of failures is one of the major categories of failures appearing in circuits in field situations due to their relative unpredictability. A relative simple method to find failures in this category is the combination of load-sensitivity calculations and tolerance sensitivity calculations which makes it possible to give a direct relation between circuit parameters and part reliability. These figures are called Parameter (Failure rate) Sensitivity figures.

$$PSx = LSy * \frac{\delta(Sy)}{\delta y} * TSx =$$

$$\frac{\delta(\lambda(Sy))}{\delta Sy} * \frac{\delta(S(y))}{\delta y} * \frac{\delta(y(x))}{\delta x}$$

Where: PSx = (Failure rate) sensitivity for circuit parameter x,
 LSy = (Failure rate) sensitivity for (often electrical) stress parameter Sy,
 Sy = relative load of a device for parameter y,
 TSx = (Tolerance) sensitivity for circuit parameter x.

Tolerance sensitivities.

Figure 7 gives the part tolerance sensitivities for "key voltage" V4.

Figure 7: Relative parameter sensitivities (V4).

Part parameter (failure rate) sensitivities.

Combination with the previously given Load Sensitivity Parameter sets shows that a combination of a stable V24 and a load sensitive leads (for capacitor C10) to a small Parameter (Failure rate) Sensitivity for all other part parameters (Figure 8).

Figure 8: Parameter (Failure Rate) Sensitivity of C10.

Important conclusion from figure 9 is the large Parameter (Failure rate) Sensitivity of transistor T3 for its internal parameters and for the parameters in the transistors base network. Especially the effects of changes in Hfe(Q3) and L3 are very important. Therefore special attention should be paid to the tolerance of these parameters in this sample circuit during series production.

Parameter Sensitivity figures FR(Q3)

Figure 9: Parameter (Failure Rate) Sensitivity of Q3

VERIFICATION.

Verification of circuits failing during simulation tests and in fall-off tests shows that indeed a strong relation exists between the stated part tolerances and the reliability of the High-Voltage transistor. Using the improved HV-transistor Load Sensitivity model it is possible to explain about 50% of the former unexpected failures.

CONCLUSIONS.

Sensitivity analysis methods are useful in addition to (MIL-HDBK-217) failure rate predictions. MIL-HDBK-217 provided a good starting point for LSP models. Extensions are found (and being verified) for power semiconductors. After verification these models will be incorporated in this method. As a result of this project it is now possible to perform a complete Parameter (Failure rate) Sensitivity calculation for many analogue circuits using singular devices. In many cases a stand alone Load Sensitivity analysis only turns out to be quite useful.

Three different switched mode power supplies were used as test case to find answers on the following questions:

- Find reliability figures of the circuit under test using (as far and as much as possible) conventional techniques.

The power supplies were analyzed and no particular reliability problems were found. High stresses causing reliability problems did not occur.

- Find consequences of combined reliability & tolerance effect analysis on the circuit under test.

The circuits turned out to be particular sensitive to some minor internal (part value) changes. Combining reliability and tolerance effect figures it was possible to explain about 50 % of

the former "unexpected" failures regarding parameter sensitivities such as the influence of variations in the value of L_3 and $H_{fe}(Q_3)$ given in the example. Also more detailed reliability and tolerance models were found, especially for the key-components of this circuit such as the HV transistor.

In the near future models will be developed for integrated circuits (Start: september 1988). Also the used method will be implemented as a part of the CARAD software. (Start: august 1988)

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Aarnout Brombacher was born in Rotterdam, the Netherlands on September 20th, 1961. He obtained his MSc. in engineering science at Twente University of Technology in 1985. Aarnout Brombacher has experience in industrial reliability analysis projects and the development of reliability analysis software. He is now working as a researcher at Twente University on the subject of reliability engineering and reliability automation, especially on the Computer Aided Reliability Analysis and Design program CARAD.

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Jan van't Loo was born on Sumatra, Indonesia on October 10th, 1933. He completed a study in Mechanical Engineering at the Haarlem Technical Highschool in the Netherlands. Jan van't Loo has company experience in various areas such as analysis of automated semiconductor production and (especially the quality and reliability aspects of) the development of consumer electronics such as television sets and videorecorders. He is now working as senior project leader for "Development Quality Assurance" within the Philips VIDEQ (Video Equipment) lab.