Developing an Integrated Design Strategy for Chip Layout Optimization

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Abstract
This paper presents an integrated design strategy for chip layout optimization. The strategy couples both electric and thermal aspects during the conceptual design phase to improve chip performances; thermal management being one of the major topics. The layout of the chip circuitry is optimized according to the proposed design rules. This offers chip layout designers an intuitive way to optimize the layout for multiple performance indicators, such as temperature, RF power output or amplifier gain. In a case study, the strategy proposed a chip redesign, boosting overall chip performance without compromising the current cooling infrastructure. The developed integrated design strategy presents a new and time-efficient approach to chip layout optimization and electronics cooling in general.

Keywords:
Thermal management, Electronics cooling, Chip layout optimization, Integrated design strategy, Layout design

1 INTRODUCTION

Thermal management has become one of the major challenges for electronic product design. Electronic component dimensions, for instance chip and resistor sizes, decrease continuously, whereas the demand for more power and functionality increases. The net result is a significant gain in component power (heat) density that needs to be controlled. As an example, the increasing power density of Intel microprocessors [1] is shown in Figure 1.

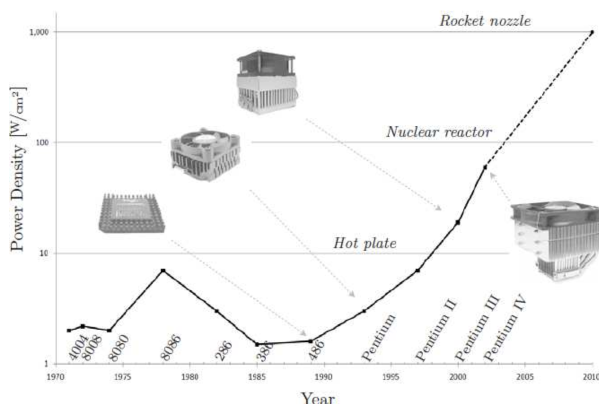

Figure 1: Increasing power density and scaling of heat sink devices for Intel microprocessors [1].

The main strategies to thermally manage the increasing power densities are focusing on the cooling equipment itself (increasing heat sink sizes, increasing air flow performance, etc.) or a change in cooling technology (from air cooling to fluid cooling or two-phase principles). Some of these cooling technologies are also shown in Figure 1. There are many examples of research primarily focusing on increasing cooling capacity [2-5].

A similar trend where this modular approach can also be observed is in publications on the design of LED modules. Researchers take the power specifications of the LED module as an input for their design process and design various cooling solutions to support the given LEDs [6-7].

Another trend in electronics design has been to focus on component layout management. By positioning and spreading high power components, cooling of the entire product can be better managed. Cheng et al. [8] use a sequential meta-modeling approach of analysis techniques to optimize board layout. Other approaches, amongst many others, are based on simulated annealing [9] or statistical parametric optimization [10]. Similar to the previous examples, these techniques also take the initial felon for granted and try to work around them following a modular approach.

As Figure 1 also indicates, future power densities will rise to absorbent levels, also referred to as the economic meltdown of Moore's law [11]. This calls for a more integral approach for the design of not only the cooling system, but the electronic components as well. This study focuses on the optimization of the dissipating electronic element itself.

1.1 Traditional electronics design process

Pahl and Beitz [12] presented in their model of the design process that during the conceptual design phase, a concept should be developed that fulfills the primary functions of the product. Whereas during the embodiment and detail design phase this concept is given its detailed description. The latter phase is illustrated more elaborately in Figure 2.

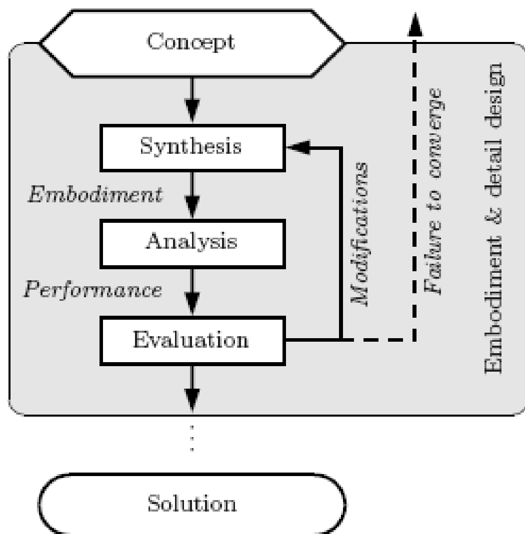

Figure 2: Embodiment and detail design phase.

According to Figure 2, through a synthesis process the concept is developed into a distinct embodiment, which incorporates specific product form and dimensions. This detailed description is required for the analysis process, which predicts product performance. Finally, in an evaluation process these performances are compared to the initial specifications. To optimize product performance, the embodiment may be modified by returning to the synthesis process, after which the altered version is analyzed and evaluated again. Depending on the number of iterations, an optimal embodiment (the solution) of a (single) certain concept is reached.

Traditionally the conceptual design process for the electronic components encompasses mainly knowledge from the electrical domain combined with production knowhow. To manufacture an electronic product, usually various electronics components are combined and assembled on a Printed Circuit Board (PCB) structure. Once an embodiment is formed in the detailing phase, analyses can be performed. Generally this is also the time that thermal analyses are performed.

1.2 Cut and run engineering

Industry generally prefers to stick to tried and tested concepts, as this gives a short time-to-market at minimal development cost. Pugh [13] refers to this as “cut and run”, as engineering is started before the conceptual design phase is thoroughly examined. This applies also to the electronics industry, where today’s product is dispensable in 2 to 3 years time. Hence, they concentrate on the embodiment and detail design phase for their product development. The iterative loop shown in Figure 2 is sometimes also referred to as a trial-and-error approach.

When requirements are updated, proven concepts might not be able to fulfill these specifications and the design process will fail to converge to an acceptable solution. Subsequently, to reach an acceptable solution, one has to return to the conceptual design phase to develop new concepts. This is indicated by the dashed line in Figure 2. Needless to say, this is more time consuming and costly; hence, the industry tries to avoid this.

1.3 Thermal design critical

As thermal management aspects, until recently, scarcely impeded an acceptable product design, thermal analyses were addressed toward the end of the design process or not at all. Cooling was considered a support function, as it supports the primary functions. Consequently, cooling should not impede primary functions, as this leads to an unrealizable concept design. When thermal limits became increasingly critical, issues were initially addressed only in the embodiment and detail design phase. As the concepts themselves did not evolve, product changes were relatively small; hence, the ever-growing heat sinks.

Many reviews indicate that thermal control has already become a critical factor in the design of electronic equipment. For instance for mobile phones, thermal management has been a critical issue since the 1990s, especially in the case of lengthy call durations. With respect to battery usage, the loss of reliability due to increased internal temperatures was significant. According to Yeh [14] in 1995 more than fifty percent of all electronics failures were caused by undesirable temperature control.

1.4 Integrated design approach

Continuing to focus on thermal issues as a support function eventually will lead to conflicting requirements. The persistent growth of thermal management systems, such as heat sinks, contradicts the development of – in particular small and compact – electronic products. Especially for high power electronic products this means product dimensions and the positioning of components are no longer determined by primary functions; instead the embodiment will be affected by thermal criteria, a support function, as well. Moreover, as mentioned, product design may even fail to converge, due to thermal constraints.

To solve these issues, a more substantial thermal engineering effort, earlier in the design phase, is required to further integrate primary and support functions. The design of electronic products in a monodisciplinary manner, for instance by focusing on electrical aspects only, should be avoided. Instead, a multidisciplinary and integrative approach must be utilized to achieve an optimal system configuration.

Domain decomposition

A first step toward such a multidisciplinary and fully integrated design process is to decompose the system requirements according to the domains involved. In 2000, Papalambros and Wilde [15] presented a method for system decomposition: Multidisciplinary Design Optimization (MDO).

In the case of the electronic component, the decomposition is illustrated in Figure 3, where E, M and T refer to the electric, mechanical and thermal domain, respectively.

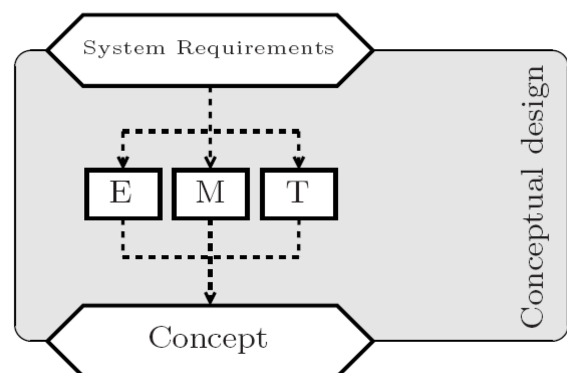

Figure 3: Domain decomposition in conceptual design.

The combined and collective knowledge of these domains has an influence on the conceptual design phase. However, as they are still considered separate and do not

share a mutual engineering "language", even small changes in one domain can have profound effects in other domains. In the case of the design of electronic components, this is a first and important step.

Full domain integration

Ideally, the knowledge of the engineering disciplines involved is directly related to each other and a mutual language has been developed. Evidently, both cases require in-depth and coherent knowledge of the engineering fields involved. This full integration of knowledge disciplines is illustrated in Figure 4.

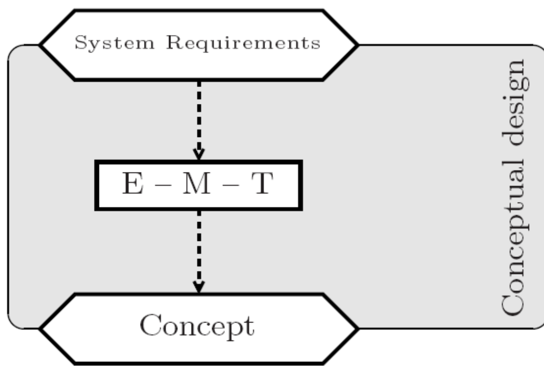

Figure 4: Domain integration in conceptual design.

At present, the latter conceptual design phase is still an abstract, hypothetical case for electronics manufacturing. However, with sufficient joint research, development and collaboration, one day we may arrive at this point. For now, the goal of this research is to start to disseminate the appropriate knowledge with regard to the thermal domain for electronic component design.

1.5 Outline

The outline of the paper is as follows. The next section describes the basic building block for an electronic component: the transistor. It also highlights the applicable design parameters and their major influences. Section 3 presents the proposed integrated design process for chip design and in Section 4 the implemented design process for layout design is described. Also, the optimization strategy for the integrated process is presented here. Section 5 describes the application of the integrated design process and optimization strategy to a case study example. Finally, conclusions and future recommendations are drawn.

2 TRANSISTOR BUILD-UP FOR LAYOUT DESIGN

2.1 Transistor background

Chips perform their electronic functions by a number of interconnected transistors. Each single transistor acts as a switch that can be turned on or off. For microprocessor applications each transistor is used to control a binary (digital) signal: a one (1) or a zero (0). One of the latest Intel chips actually combines more than one billion transistors for their computing power.

The typical layout of a transistor is shown in Figure 5. The transistor is formed by a highly conductive channel deposited on a semi-insulating substrate. The terminals (source and drain) are connected to the substrate with an ohmic metal contact. The gate is also connected to the substrate but has a metal-semiconductor junction in between. This potential barrier acts as a diode and is used to open and close the gate quickly. The length of the gate (denoted L in Figure 5) is defined as the distance between the source and drain. The gate width refers to the extension of the transistor is z-direction. Typically the width is larger than the length.

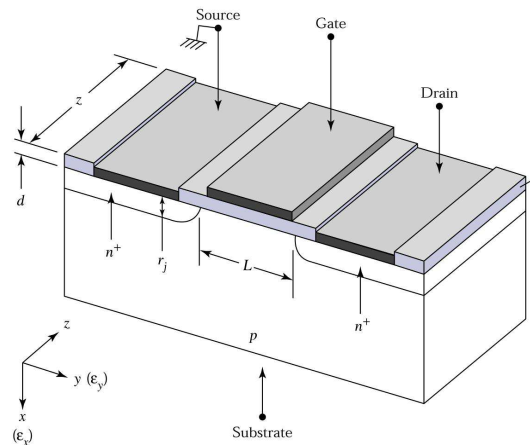

Figure 5: Basic single-gate transistor layout [16].

2.2 Transistor for power amplification

Next to digital applications, transistor technology is also used in analog or microwave applications. Here, the transistor is used as an amplifier that can be switched on and off. When the transistor is switched on, the incoming signal is amplified. To boost amplification, multiple gates can be positioned in parallel. In this case, all of the gates of the transistor combined are capable of controlling the transistor state. If the gates are opened by an applied voltage, electrons can flow from the source to the drain terminal. If no voltage is applied, the gates are closed and the electrons are blocked. The flow of electrons is affected by the size and shape of the transistor. Hence, the amplification characteristics of the transistor are also determined by its geometry.

On a typical High Power Amplifier (HPA) chip the transistors are arranged in amplifier stages. The HPA chip may consist of a single or multiple amplifier stages. Each amplifier stage consists of a single or multiple transistors and within each transistor multiple gates can be positioned in parallel. Parallel positioning of the gates forming a multiple-gate transistor is shown in Figure 6.

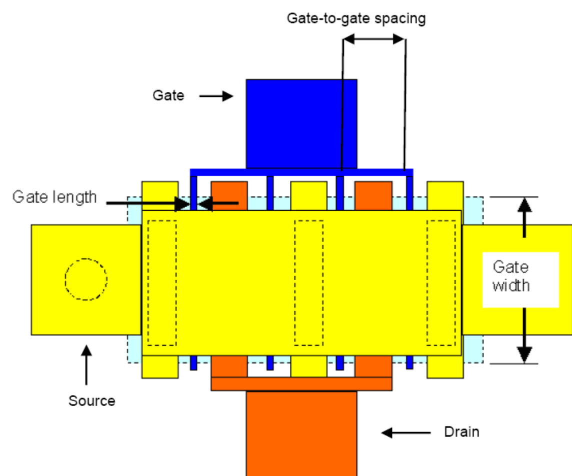

Figure 6: Transistor layout with a multiple-gate structure [16].

Figure 6 shows the gate length and gate width similar to the single-gate transistor of Figure 5. Next to these parameters, now also the total number of gates and the

Parameter	Primary design effect
Gate length	The gate length affects the operating frequency. Higher operating frequencies (small wavelength) reduce the maximum gate length.
Gate width	The gate width determines the amplification performance. It also affects the operating frequency. Higher operating frequencies limit the maximum gate width. Small wavelengths may oscillate, reducing the transistor efficiency.
Number of parallel gates	The total gate width can be extended (without harmful oscillations) by having multiple parallel gates. The number of parallel gates is limited by the phase difference of the transistor's input and output signal, due to the relative distance between center and outer gates. As a secondary effect, more gates also result in a wider device and higher cost (see gate-to-gate spacing).
Gate-to-gate spacing	The spacing and total number of gates determine the total size of the transistor. The total size is limited by the commercial available substrate wafers. To a large extent the usage of wafer space determines the cost of the device.
Substrate thickness	The substrate thickness is limited by commercially available substrate wafers. The thickness and material properties have an impact on the thermal performance.
Solder thickness	The thickness of the solder layer that holds the chip also has an impact on the thermal performance.

Table 1: Geometrical design parameters and their primary effect.

gate-to-gate spacing are important to determine the transistor performance.

The transistor is deposited on a semiconductor substrate and this semiconductor device (chip) is in turn soldered into or onto an electronic package. Hence, other geometrical design parameters for this case study are the substrate and solder thicknesses. Table 1 lists all geometrical parameters. To get a better understanding of the design process, their influence on the chip performance is also given.

2.3 Electric and thermal criteria

Next to the geometrical design parameters, other design parameters are those of the electric and thermal domains. As was mentioned in Table 1, the gate width determines to amplifier performance. Since the width is limited, to boost performance gates are positioned in parallel. Also, the operating frequency of the Radio Frequent (RF) input signal is an important parameter. Usually the frequency is demanded by the application. Other electric criteria are the pulse length and the chip's duty cycle. During the time of the pulse (pulse length) the RF signal is amplified by the chip. Due to the chip's limited efficiency during this time thermal dissipation, heating up the device, also takes place. The duty cycle refers to the percentage of time that the transistor is actually amplifying versus the total operation time. A low duty cycle means a short heat-dissipation time and longer cooling-only time; whereas at a 100% duty cycle the transistors are always dissipating heat.

From a thermal perspective, two additional design parameters are important: (1) the dissipated power and (2) the operating temperature. The power of the input and output signals, the chip DC power and the chip efficiency determine the total amount of power that is dissipated as heat by the transistors. This heat needs to be disposed of through the substrate and solder layers to the external environment.

Chip temperature has an influence on the conducting properties of the base material; hence, it influences the electric efficiency of the chip. This coupling or loop-back effect is usually ignored due to its complexity and to speed up the design process. The chip's operating temperature and material properties determine to a large extend the Mean Time To Failure (MTTF). Usually the application demands a certain MTTF, which limits the maximum operating temperature.

The electric and thermal criteria are summarized in Table 2. For this paper, only the electric criteria that have an impact on the thermal characteristics are presented. Other aspects, as for instance the influence of interstage matching on signal reflections and oscillations, fall outside the scope of this study.

2.4 High Power Amplifier (HPA) chip design

As mentioned in Section 2.2, on a typical HPA chip the transistors are arranged in amplifier stages. Figure 7 shows the chip layout of a 16W X-Band HPA chip. X-Band refers to the frequency range of the RF signal. As indicated in the figure, this chip has two amplifier stages. Also shown are the matching circuits, typical for analog chip design. They split the input signals and combine the amplified signals, like a piping system. Also, they control the signals' impedance. Its layout is dependent on the electric parameters.

Due to the limited conducting properties, power is also dissipated in the matching circuits. However this can be ignored compared to the heat dissipation in the amplifier stages, where the transistors are positioned in parallel.

Parameter	Unit	Design criteria
Operating frequency	[Hz]	Frequency of the RF signal.
Pulse length	[ms]	Time of amplification of the RF signal.
Duty cycle	[-]	Percentage of time that the amplifier is amplifying.
Dissipated power	[W]	Amount of power (heat) that is dissipated by the transistors.
Operating temperature	[°C]	Maximum temperature at the gates of the transistors.

Table 2: Electric and thermal design criteria.

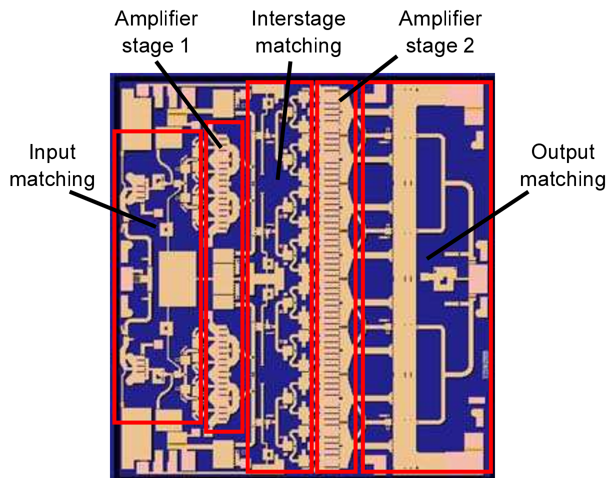

Figure 7: Layout of the TGA2517 – X-Band 16W Power Amplifier [17].

The total number of stages, transistors and gates determine the output power and the amplification gain. Hence, the design can be tailored to meet the required performance of the HPA chip.

3 CHIP DESIGN PROCESS

3.1 Current chip design process

Currently, the design of electronic components is mainly determined by electronic properties. Since until recently the chip temperature did not pose a serious threat, thermal criteria were not a part of the initial design requirements. The design of electronic components was verified thermally by checking the maximum temperature value of hotspots (the gate temperatures) on the surface during operation. The MTTF based on the maximum operating temperature of the components was used to estimate the component lifetime. When the temperature was rising too high, better cooling devices were applied, as was shown in Figure 1. Hence, thermal criteria were applied as a form of go/no go option at the very end of the design phase. Schematically, this is shown in Figure 8.

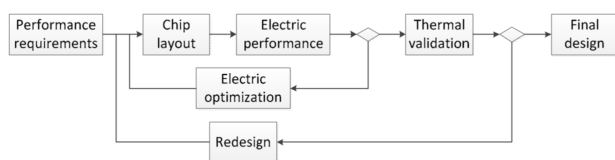

Figure 8: Traditional chip design process.

As shown in Figure 8, an initial chip layout is proposed as an input to determine the electric performance. The electric optimization loop represents the current strategy electronic engineers apply in their search for the optimal chip design based on the initial requirements. This includes, amongst others, finding optimal parameter values for the first four geometrical parameters of Table 1.

Once a chip layout is (electrically) validated and optimized, thermal engineers validate the chip layout. Based on the initial requirements and the final chip layout, the power dissipations at the transistor junction (gate) are determined. Finally, if sufficient cooling capacity can be achieved into the electronic product such that the junction temperatures remain below the demanded MTTF temperature, the chip design is validated. Otherwise, a redesign of the whole layout is imminent.

In practice, the redesign loop is hardly ever practiced. Since thermal analyses are done at the very end, returning would be very time consuming and expensive. As chip design progresses, thermal engineers have to become more and more creative to handle the thermal design. However, they still have no say in the original chip layout, since this is outside of their knowledge domain. Hence, there is still ample space for optimization.

3.2 Proposed integrated design process

This paper proposes an integrated design process that focuses on both electronic and thermal criteria simultaneously. In this new approach, thermal criteria have more influence during the conceptual design phase of the electronic component, compared to the current design process discussed in the previous section.

For instance, with a different chip layout, local thermal hotspots on the chip surface that limit the demanded criteria might be avoided. As a consequence, the maximum chip temperature values can be lower for equal or better electric performances. Hence, overall better performances can be achieved. The process of this strategy is shown in Figure 9.

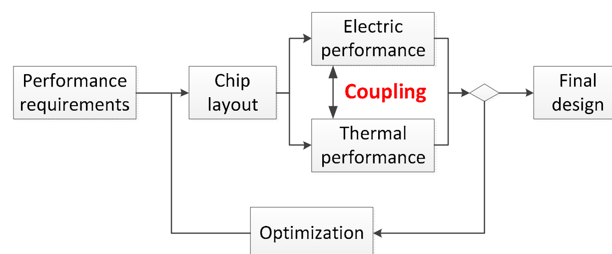

Figure 9: Proposed integrated chip design process.

As illustrated in Figure 9, an initial chip layout is proposed as input to determine both the electric and thermal performances. To determine either performance values, knowledge of the other domain is required. The amount of heat dissipation is determined by electric criteria; whereas electric performances are temperature dependent. Hence, there is a strong coupling between the parameters.

In recent years some work has been done in this field. For instance, Codecasa et al. [18] and Vellvehi et al. [19] both describe a method for electro-thermal analysis. The former uses a network (or lumped) approach that mimics the physical properties of the original phenomenon, whereas the latter uses a two-step approach where electrical and thermal models are solved separately exchanging performance parameters periodically. Multi-physical-domain analyses are usually done is this way, for instance for integrated power devices [20] or bipolar transistors [21]. The latter also present a strategy to evaluate the temperature fields. This information could be used in the design process.

Currently, as illustrated, the direct relation between specific, low-level electric parameters and local structure temperatures is not well understood. For this study, the coupling is realized in a global descriptive way. The dissipated thermal power is coupled to the overall chip electric properties, such as gain, input power and power added efficiency and the total gate width. In terms of handling design knowledge this falls under the category of domain decomposition as described in Figure 3.

Ultimately, as the underlying fundamental principles are better understood a stronger coupling between the local electric parameters and local thermal influences can be modeled. Hence, full domain integration as described in Figure 4 can be accomplished.

4 CHIP LAYOUT OPTIMIZATION STRATEGY

4.1 Identifying the total design space

To find a uniform chip layout optimization strategy, one of the transistors in one of the amplifier stages is modeled and analyzed in a finite element analysis software tool.

With this finite element model the total design space is identified. The design parameters are the geometrical layout properties of the chip, as listed in Table 1; the model's input criteria are the parameters of Table 2.

Since some of the parameters are dependent, to start two independent parameters are chosen. The first independent design parameter is the number of gates. It was varied from one to a maximum value. The second independent parameter is the amplification gain, represented by the total dissipated power. This also determines the total gate width. The transistor technology (e.g. GaN, GaAs, etc.) determines substrate thicknesses and the available chip surface. The following iterative process scheme was used:

1. Adjust the total number of gates (add 1 each time).
2. Adjust single gate sizes (length and width) to the overall chip power requirements.
3. Determine the gate-to-gate spacing.
4. Model and mesh the current layout.
5. Set thermal power dissipation.
6. Determine local gate temperatures with a finite element analysis.
7. Store the input geometry with the generated performance values separately.
8. Return to Step 5, until maximum power is reached.
9. Return to Step 1, unless the maximum number of gates is reached.

For the numerical analysis Comsol Multiphysics was used. Comsol has a good interface with Matlab, which allowed us to automate the iterative process scheme. After the scheme was automated robustly, a high performance computer fully characterized the entire design space. This took several days, for one type of transistor technology.

One of the calculated layouts is presented in Figure 10. It shows a possible configuration for the HPA chip. Four gates are modeled – identified by the finer mesh – at the calculated gate-to-gate spacing (112.5µm). In this case, the gate width and length are 250µm and 1µm, respectively.

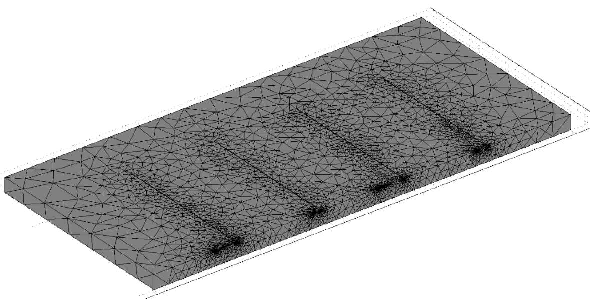

Figure 10: 3D mesh of GaN/SiC HPA chip.

Before identifying the total design space, the transistor finite element model was compared to an in-house benchmark reference dataset. The simulated temperature values at the gate fingers showed a maximum difference of 0.1°C. For a thermal analysis this is an acceptable value.

Data representation

The calculated data from the iterative process can be represented in many ways. Most parameters show an expected trend when the dissipated power is set to a constant value. For instance, for increasing gate width the maximum temperature will increase to a certain threshold value. This is explained by the fact that thermal saturation takes place in the gate finger. Another example is that for increasing gate-to-gate spacing the maximum temperature drops continuously, as can be expected since the power density also becomes lower.

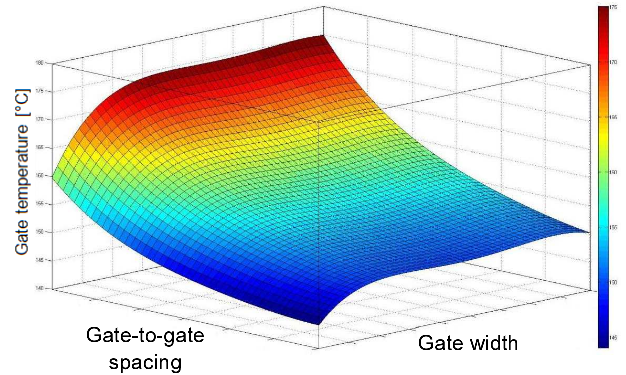

Figure 11: Maximum gate temperature as a function of gate-to-gate spacing and gate width.

Figure 11 illustrates both described effects. For increasing gate width values, gate temperatures increase reaching a threshold. The threshold is caused by the thermal saturation of the gate width. When saturation is reached, changing the gate width does not affect the gate temperature anymore. However, by changing the gate-to-gate spacing still a temperature drop can be realized. In this specific example, a temperature reduction of approximately 25°C is still possible.

4.2 Building an optimization strategy

Further in-depth analysis of the total design space has led to the development of a transistor layout optimization strategy. The goal of the optimization steps is to get as much performance out of the transistor as possible without overheating. This strategy is illustrated in Figure 12.

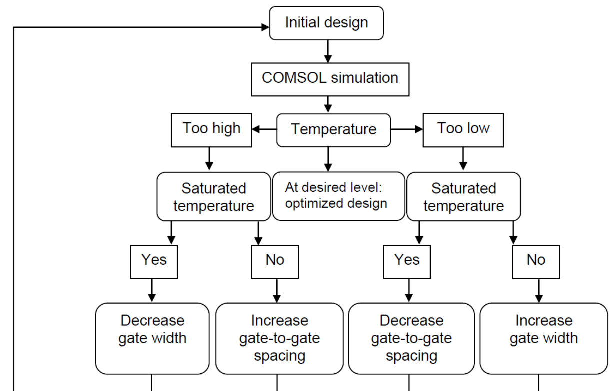

Figure 12: Chip layout optimization strategy.

The optimization scheme centers around the chip temperature. If the temperature is too high and gate saturation is reached, the gate width must be decreased. When saturation is not yet reach the gate-to-gate spacing must be increased. A similar strategy but vice versa must be applied when the chip temperature is too low. Finally, at the desired (maximum MTTF) temperature optimal performance is achieved.

To make this optimization strategy manageable, in our implementation for both the gate width and the gate-to-gate spacing the smallest discretized step was 1µm. Using finer step sizes did not yield higher order effects, but the computational load increased tremendously.

5 CASE STUDY

To demonstrate the procedure and advantages of the proposed integrated design strategy, it has been applied to an industrial case study. The goal was to redesign a HPA chip, based on a GaN/SiC technology platform, used for naval radar systems.

In the design a two-stage chip design was used to reach the required RF power output. The second stage of the chip consisted of several 16-gate transistors. Analysis of this chip design shows a maximum gate temperature of 223.2°C. Figure 13 shows the initial layout of the second stage with the temperature distribution.

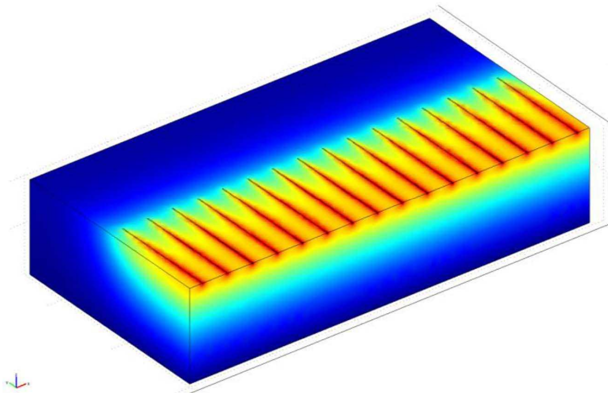

Figure 13: Initial transistor layout (16 gates) overlaid with thermal analysis.

Following the chip layout optimization strategy of Figure 12, it was discovered that the maximum gate temperature could be reduced to 186.1°C, almost 40 degrees lower than the initial design. In the final design, the number of gates was reduced to 8. At the same time, the gate-to-gate spacing and gate-width was optimized to compensate for the lower number of gates. The final design is shown in Figure 14.

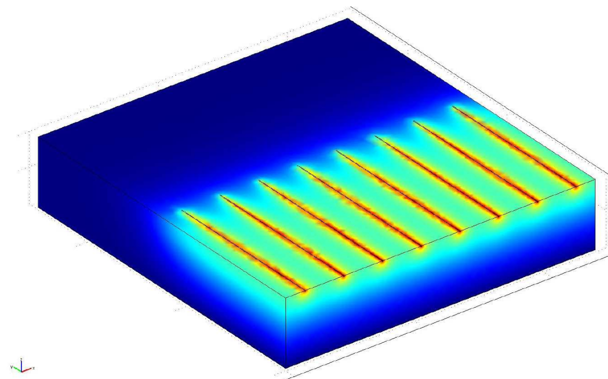

Figure 14: Final transistor layout (8 gates) overlaid with thermal analysis.

With the transistor layout of Figure 14, the required RF power can still be realized. However the gate temperature is much lower (approximately 40°C).

This layout performs much better thermally for equal global electric performance. Hence, in total a more overall optimized design is realized. Also, these analyses can now be performed during the very early stages of the conceptual design phase.

For this case study, this meant that radar performance could be boosted without changing the current cooling infrastructure. Obviously, this is a very desirable outcome, not only for this case study.

6 SUMMARY

By integrating electric and thermal criteria directly into the conceptual design phase of electronic components, better chip performances can be realized. A model of the transistor gate structure is presented, highlighting important parameters. The parameters are split up into geometrical design parameters, and electric and thermal input criteria. Finite element analyses were used to identify the entire design space. By analyzing this data, a new design strategy is formulated for chip layout optimization.

As a result of this study, chip performance can be improved with lower local hotspot temperatures. The local maximum temperature was lower due to a better geometrical layout of the chip circuitry. The proposed strategy was successfully applied to a case study: a redesign could be proposed that fulfilled the RF output requirement while reaching a lower chip temperature.

In the end, this study tries to give chip layout designers an intuitive and pragmatic way to optimize the layout for a multitude of performance indicators, such as temperature, RF power output or amplifier gain.

6.1 Future perspective

Further research is required to tackle further chip layout optimization. For instance, the number of amplifier stages is still chosen as an expert's educated choice. By further expanding the total design space, new strategies are expected to be found to solve these design issues as well.

More fundamental research might reveal the direct interactions between electric and thermal effect locally in the gate finger regions. If this knowledge can be captured in an integrated multi-physics model, the integrated chip design process can be further optimized.

7 ACKNOWLEDGMENTS

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