Ferroelectric Thin-Film Capacitors and Piezoelectric Switches for Mobile Communication Applications

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(*Invited Paper*)

***Abstract*—Thin-film ferroelectric capacitors have been integrated with resistors and active functions such as ESD protection into small, miniaturized modules, which enable a board space saving of up to 80%. With the optimum materials and processes, integrated capacitors with capacitance densities of up to 100 nF/mm² for stacked capacitors combined with breakdown voltages of 90 V have been achieved. The integration of these high-density capacitors with extremely high breakdown voltage is a major accomplishment in the world of passive components and has not yet been reported for any other passive integration technology. Furthermore, thin-film tunable capacitors based on barium strontium titanate with high tuning range and high quality factor at 1 GHz have been demonstrated. Finally, piezoelectric thin films for piezoelectric switches with high switching speed have been realized.**

I. Introduction

Ferroelectric and piezoelectric thin films are gaining more importance for the integration of high-performance functions in miniaturized modules. Dielectric, ferroelectric, and piezoelectric thin films are excellently suited to realize system in package (SiP) devices, which are multifunctional modules, where individual functions are implemented in their optimum technology with respect to performance, size, and cost. SiP especially plays a role for devices based on nontraditional materials and processes, which are not available in standard CMOS technologies (more than Moore) and is thus a complementary technology to the system-on-chip, which follows the CMOS roadmap as predicted by Moore's law. Small-sized SiP making use of ferroelectric thin films will be discussed.

II. Integrated, Discrete Modules with High-Performance Integrated Passives

A. Devices and Processes

Integration of passive functions with active functions into miniaturized modules is a prerequisite for next-generation base-band, audio, and power circuits of mobile and portable electronic systems. We have opened the way for integrated passive functions such as capacitors and resistors with active functions like electrostatic discharge (ESD) protection diodes into one integrated module [1], [2]. This integration of ferroelectric capacitors with resistors and ESD protection diodes in a small chip-scale package enables a board space saving of up to 80% (see Fig. 1).

The devices are realized on highly doped silicon substrates. With optimum design and processing, Zener diodes for ESD protection of 8, 12, and 16 kV are integrated. The ESD protection is essential in mobile and portable circuits to protect downstream ICs from electrostatic discharge. On top of the Si substrate, thin-film metal-insulator-metal (MIM) capacitors are integrated together with thin-film resistors. MIM capacitors offer high design flexibility. Floating coupling capacitors and shunt capacitors can be integrated next to resistors and ESD protection diodes (see Fig. 2).

The thin film MIM capacitors, which are integrated with active functions, are based on lead titanate zirconate. The films are processed on top of Ti/Pt electrodes by spin-on technology. The ferroelectric thin films have a typical thickness of 270 to 400 nm. On top of the ferroelectric thin films, thin-film metal layers are deposited and lithographically patterned. They enable the processing of resistors of 50 Ω up to several hundred kilo-ohms. A special feature of the integration process is that not only ferroelectric MIM capacitors have been integrated with resistors and ESD protection diodes.

In an extension of the process technology, stacking of the ferroelectric capacitors on top of each other also has been realized. The stacking and connecting in parallel enables, on the one hand, a strong increase of the capacitance density of the MIMIM thin-film integrated capacitors. On the other hand, it offers a 3-D integration and an extremely high integration density. An example of stacked ferroelectric MIMIM capacitors on top of Si substrates with integrated active functions is shown in Figs. 3 and 4. The combination of 3 transmission electron microscopy (TEM) dark field images (in red, green, and blue) highlights the columnar growth of the ferroelectric thin films with (lateral) column widths in the range 100 to 300 nm.

Thin-film capacitors realized in the first generation devices have a typical dielectric thickness of 270 to 400 nm,

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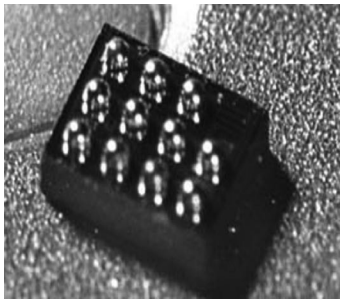

Fig. 1. High-density metal-insulator-metal (MIM) capacitors integrated with resistors and ESD protection diodes in small chip-scale package.

Fig. 2. High-density MIM capacitors designed to ground (right schematic) and in/out (left schematic) integrated with resistors and ESD protection diodes.

relative permittivities of 850 to 1050, tanδ of ~1.5%, and capacitance densities of 23 to 30 nF/mm^2. These first-generation thin-film capacitors integrated with resistors and ESD protection diodes offer high-performance products, comprising, for example, low pass filters with ESD protection diodes (see Fig. 5).

By modification of the process and stacking of 2 capacitors on top of each other, integrated thin-film capacitors have been achieved that show relative permittivities of up to 1600 and capacitance densities of 80 to 100 nF/mm^2.

Stacking of thin-film capacitors has been demonstrated by other groups for $Ba_{1-x}Sr_xTiO_3$ thin films [3] as well as for lanthanum-doped $PbZr_xTi_{1-x}O_3$ films. Stacked PLZT capacitors, applying extremely thin PLZT (12/30/70) films with 50 nm thickness to achieve high capacitances of up to 500 nF, have been reported in [4].

B. Quality and Reliability of Integrated Discrete Modules with Ferroelectric Capacitors

The capacitors developed in our process show an extremely high capacitance density and extremely high breakdown voltages. For the thin-film capacitors with capacitance densities of 20 nF/mm^2 and thickness of 400 nm, a relative permittivity of 950 and a breakdown voltage of 140 V, corresponding with a breakdown field of 3.5 MV/cm, is obtained. Breakdown voltages were obtained from measurements of the current as a function of voltage with increasing voltage rate with 5 V/s. Breakdown voltage is determined from the point where the current strongly increases by orders of magnitude while increasing the voltage with 5 V/s.

Literature models predict a decrease of the breakdown field (E_{bd}) as a function of the dielectric constant k ($E_{bd} \sim k^{-0.5}$) [5], [6], which makes it challenging to combine high-capacitance densities with a high-breakdown

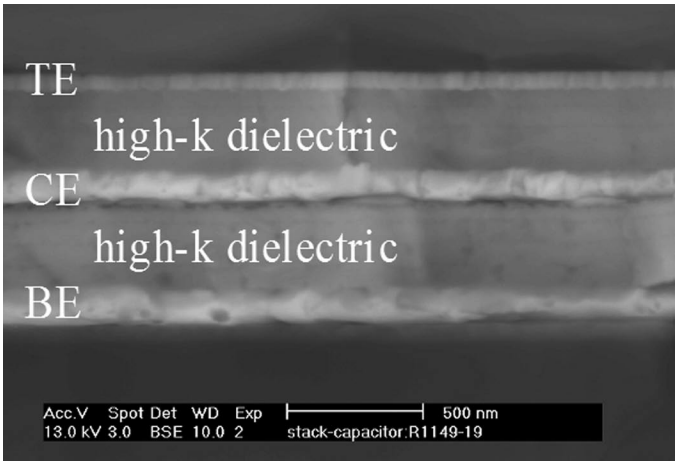

Fig. 3. SEM micrograph of a stacked ferroelectric capacitor: The cross section shows 2 layers with high relative permittivity sandwiched between the bottom electrode (BE) and the top electrode (TE) and a shared center electrode (CE).

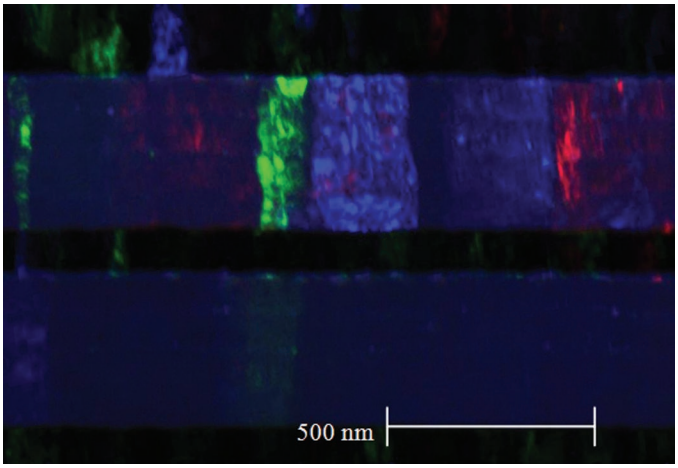

Fig. 4. Combination of 3 TEM dark field images of a stacked ferroelectric capacitor with high relative permittivity. The high-k layers are sandwiched between the bottom electrode (BE, Ti/Pt), the top electrode (TE, resistor metal), and a shared center electrode (CE, Pt).

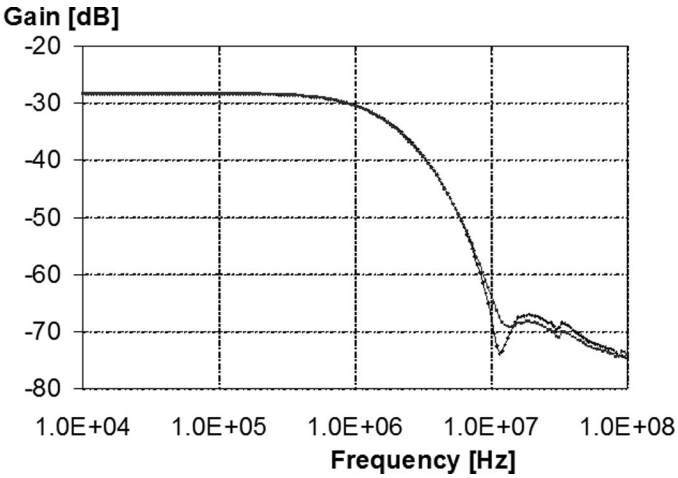

Fig. 5. Frequency response of 2 RC low-pass filters with high density MIM capacitors integrated in Si substrate next to ESD protection diodes.

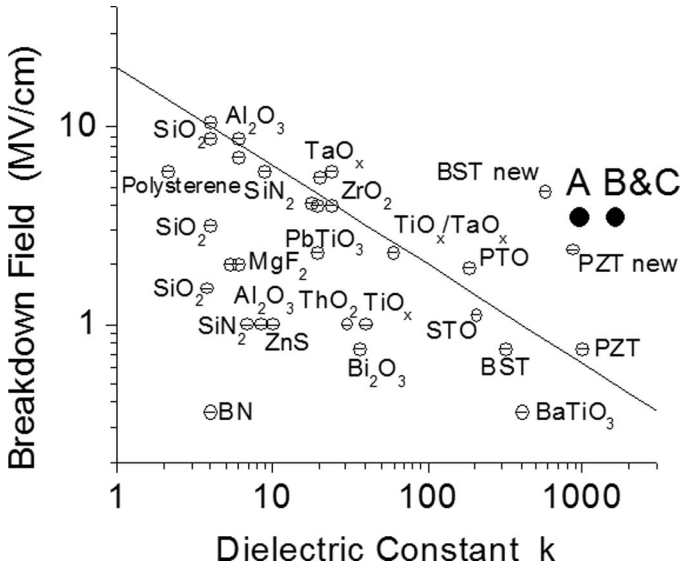

Fig. 6. The breakdown field (E_{bd}) as a function of the dielectric constant (k). The breakdown field decreases as the dielectric constant increases. The line is a fit through the data of the best samples from literature, obtained from [5]. Two more recent data points are added from [6] and [7] indicated by "new." The results from our work are indicated by the black circles (●). The details of A, B, and C can be found in Table I.

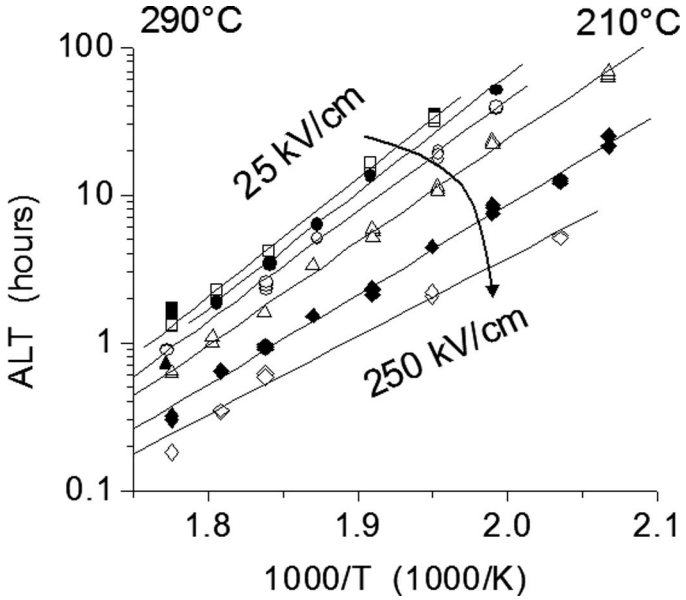

Fig. 7. Accelerated lifetime results for the high-k capacitors of type A (20 nF/mm^2). Measurements are performed between 290 and 210°C and from 25 to 250 kV/cm. The data are fitted by an Arrhenius law, $t \sim \exp(E_{\mathrm{act}}/kT)$.

voltage (U_{bd}). However, these models are mainly based on paraelectric materials. First-generation devices with a capacitance density of 20 nF/mm^2 and a U_{bd} of 140 V are currently mass-produced at NXP Semiconductors. The E_{bd} of these capacitors, 3.5 MV/cm, is considerably larger than what is estimated in [5] and [6], (~0.6 MV/cm for k = 950, see Fig. 6).

The model from [5] is a phenomenological model, based on the best data from literature. In [6], the interpretation of the results is based on a calculation of the breakdown strength by a thermochemical model. Our results demonstrate that ferroelectric materials are able to outperform the estimations from [5] and [6]. The high breakdown field of 3.5 MV/cm of our ferroelectric thin film capacitors is in the order of breakdown fields reported for TiO_2 thin films, but at much higher relative permittivities of up to 1600 in contrast to approximately 80 to 100 for TiO_2. This enables the integration of very large capacitors with high breakdown voltages above 50 V in Si technology. The high breakdown voltage is requested for numerous consumer applications. Currently, due to the limitations of the capacitance density in Si-processing, large capacitors with high breakdown voltage are typically mounted as discrete SMD components on the printed circuit board, consuming more area than the integrated solution with high-density capacitors.

To offer even higher capacitance densities than 20 nF/mm^2, stacked capacitors with 360 nm and 270 nm thickness and relative permittivities of 1600 are realized, which show capacitance densities of 80 nF/mm^2 and 100 nF/mm^2. For these integrated capacitors, breakdown voltages of 120 and 90 V were achieved, which correspond to a breakdown field of 3.3 MV/cm.

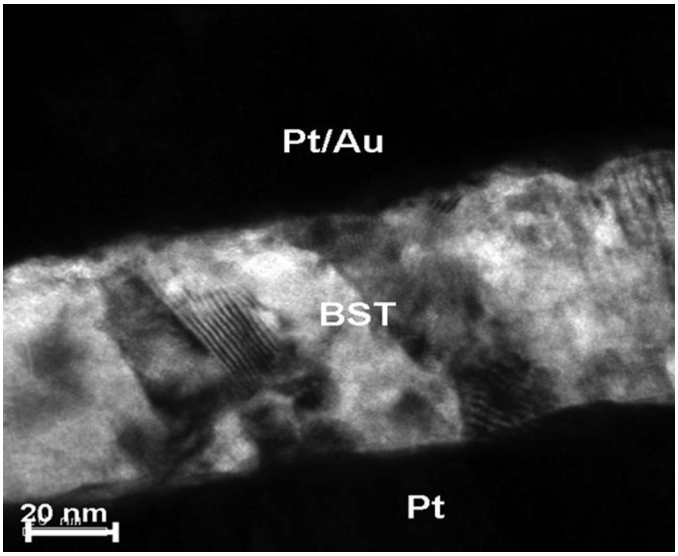

Fig. 8. TEM image of a $Ba_{1-x}Sr_xTiO_3$ thin film grown on top of a Pt bottom electrode.

The extremely high-capacitance density of 100 nF/mm^2 for the integrated thin-film capacitor and the high breakdown voltage of 90 V is a revolution in the world of integration of passive components and has not yet been reported for any other passive integration technology.

The devices are developed for numerous applications, which require typical operation voltages of 3 to 5 V and lifetimes of 10 years at 85°C. For this reason, we intensively investigated the lifetime of our capacitors under dc bias. Accelerated lifetime tests (ALT) have been applied to determine the lifetime of the various capacitors. The end of life of the capacitors was defined as the time where the leakage current has been increased by one order of magnitude, which is a much more conservative lifetime

TABLE I. EXTRAPOLATED LIFETIME FOR INTEGRATED FERROELECTRIC CAPACITORS.

Type	C/A in nF/mm^2	d in nm	Capacitor	Effective dielectric constant (k)	ALT at 5 V and 85°C in years
A	20	400	single	950	1500
B	80	360	stacked	1600	70
C	105	270	stacked	1600	13

[1]ALT = accelerated lifetime test.

definition than the lifetimes obtained by time-dependent breakdown measurements. The field dependence of the lifetime for 20 nF/mm^2 (area is 0.5 mm^2) capacitors at elevated temperatures of 210 to 290°C has been studied. On an Arrhenius plot, lifetime versus 1/T, an exponential behavior $t \sim \exp(E_{act}/kT)$ with a field-dependent activation energy, E_{act}, of 1.6 to 1.1 eV for 75 to 250 kV/cm has been determined (see Fig. 7).

Extrapolation of the lifetime to 85°C results in more than 10 years' lifetime for capacitors with 20 nF/mm^2 and for voltages as high as 10 V (250 kV/cm) (see Table I).

Besides the lifetime data for 20 nF/mm^2 capacitors, we also studied the lifetime of 80 and 100 nF/mm^2 capacitors (area is 0.3 mm^2). The lifetime at 85°C and 5 V for stacked capacitors with 80 nF/mm^2, processed from 370 nm thick dielectrics with relative permittivities of 1600, has been extrapolated down from high temperature data. For 80 nF/mm^2 stacked capacitors, lifetimes of 70 years at 5 V and 85°C have been determined. For stacked capacitors with a 270 nm thick dielectric layer with a relative permittivity of 1600 and 100 nF/mm^2, a lifetime of 13 years at 85°C and 5 V has been extrapolated. These data show that the integrated capacitors developed here with capacitance densities of 20 to 100 nF/mm^2 offer at operating voltages of 5 V and operating temperatures of up to 85°C a lifetime of more than 10 years.

III. INTEGRATED TUNABLE CAPACITORS FOR MATCHING NETWORKS AND TUNABLE FILTERS

Tunable capacitors based, e.g., on paraelectric thin films with perovskite or pyrochlore lattice are becoming more relevant for miniaturized adaptive impedance matching networks, tunable filters, voltage controlled oscillators, or phase shifters [8]–[10]. $Ba_{1-x}Sr_xTiO_3$ (BST) thin films with $x = 0$ to 1 [11], [12], as well as $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ [14], are investigated. For $Ba_{1-x}Sr_xTiO_3$ thin films with $x = 0.5$, which are deposited by sputtering with a typical thickness of 100 to 150 nm on sapphire substrates—and depending on the sputter conditions—relative permittivities of 300 to 900 at 0 V bias and maximum tuning ranges of 90% are reported above 3 MV/cm [11]. For these tunable capacitors, quality factors of 40 to 160 at 1 MHz up to several gigahertz are reported.

Besides $Ba_{1-x}Sr_xTiO_3$, $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ thin films crystallizing in the pyrochlore phase are investigated for tunable capacitors [14]. Thin films with thickness of 300 to 330 nm are deposited by sputtering on glass substrates with a Ti/Pt electrode. Au-topped electrodes are applied on the dielectric thin film. Relative permittivities of 185, tunability of 44% at 1 MV/cm, and quality factors above 100 up to 5 GHz for capacitors with 64 μm^2 capacitance area are reported.

We have investigated $Ba_{1-x}Sr_xTiO_3$ thin films with $x = 0$ to 0.5, which are deposited on Si-substrates with Ti/Pt or Pt or Pt/Au/Pt metallic electrode layers. The barium strontium titanate thin films are grown by spin-on processing at temperatures of 680 to 740°C. As highly conductive top electrodes, Au or Pt/Au electrodes are applied. All the layers are lithographically patterned using dry etching processes. The $Ba_{1-x}Sr_xTiO_3$ thin films have a polycrystalline structure with a grain size varying from 20 to 40 nm. For BST films grown on Ti/Pt bottom electrodes, a thin TiO_2 dead interface layer at the Pt electrode was found with an EDAX (EDAX Inc., Mahwah, NJ) line profile analysis throughout the complete stack. Homogeneous dense films with a sharp Pt–BST interface could be processed on Pt electrodes without Ti adhesion layer (see Fig. 8). EDAX analysis (see Fig. 9) confirmed that no TiO_2 interface layer between the BST film and the Pt electrode is formed.

With these thin films, having a typical thickness of 80 to 130 nm, relative permittivities of 400 measured at 1 MHz (using an HP4194a impedance analyzer; Hewlett Packard, Palo Alto, CA) to 5 GHz (using an R3767CG vector network analyzer; Advantest Corporation, Tokyo, Japan) and corresponding to capacitance densities of 30 nF/mm^2 and tuning ranges of 75% at 1 MHz have been achieved. These high quality thin films grown on Si show at CMOS compatible operating voltages of 3 V already tunabilities of 35% (see Fig. 10) at 1 MHz. So with these thin films, tunabilities of 35% could be achieved at low voltages of 3V. This voltage is much lower than the maximum electrical field strength of the BST capacitors and enables therefore long lifetimes conditions for the capacitors.

At 1 GHz, the thin-film capacitors with BST thin film grown on top of a Pt-bottom electrode and a Pt/Au-top electrode show quality factors above 30.

IV. GALVANIC PIEZOELECTRIC SWITCHES

RF microelectromechanical system (MEMS) switches are attractive devices for mobile communication applications because they show lower insertion losses, higher iso-

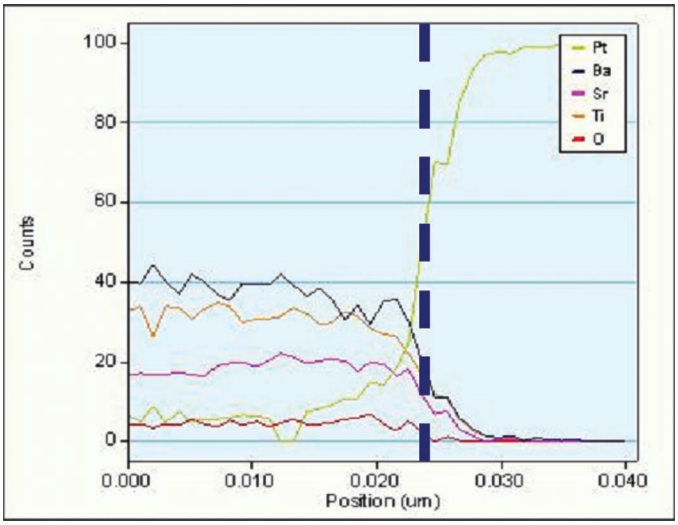

Fig. 9. EDAX analysis of the interface of the $Ba_{1-x}Sr_xTiO_3$ thin film grown on top of a Pt bottom electrode.

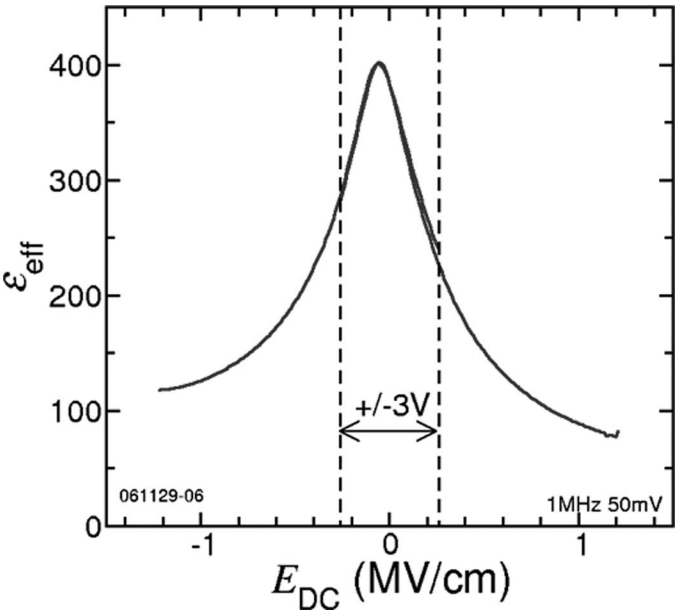

Fig. 10. Effective relative permittivity as a function of dc field for a $Ba_{1-x}Sr_xTiO_3$ thin film grown on top of a Pt bottom electrode on Si.

lations, and better linearity compared with currently used semiconducting RF switches like p-i-n diodes, pseudomorphic high electron mobility transistors (pHEMTs), or CMOS transistors. RF MEMS switches also have low power consumption, making them very suitable for mobile devices. Galvanic RF MEMS switches have been investigated by several groups, because they are broadband and have a higher RF isolation than capacitive MEMS switches.

We are investigating galvanic MEMS switches, based on piezoelectric actuators, which offer several advantages over electrostatic or thermal actuation. Piezoelectric actuators operate at lower voltage and possess a larger open gap and thus higher isolation in the open state. Piezoelectric galvanic switches are not yet state of the art. To

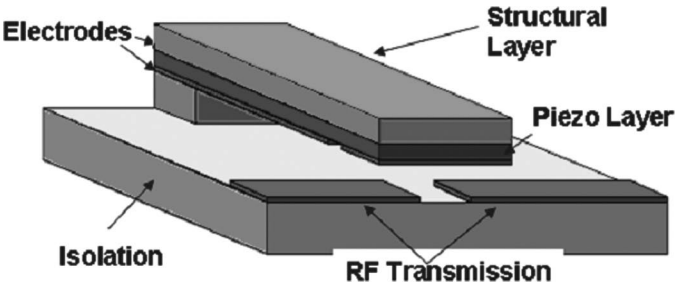

Fig. 11. Schematic picture of a galvanic piezoelectric microelectromechanical system switch. The structural layer is also used as the top electrode.

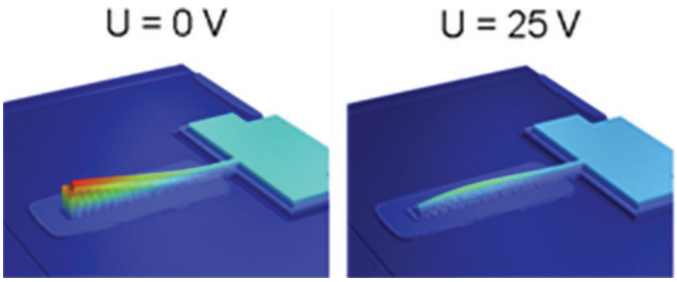

Fig. 12. White light interferometer measurement of the height profile of a galvanic piezoelectric microelectromechanical system switch.

benefit from their advantages, more research is needed with respect to actuator processing and optimum design [15]–[17].

An artist's view of the piezoelectric MEMS switch investigated in this work is shown in Fig. 11. The piezoelectric actuator is built up from a Ti/Pt bottom electrode. The piezoelectric layer is deposited using sol-gel processing. To realize galvanic MEMS switches, a low-temperature-processed 450 to 650°C lead titanate zirconate has been developed. In this design, the top electrode is also used as the structural layer to create a bending moment when applying a voltage across the piezoelectric layer.

The low-temperature-processed piezoelectric thin film materials used here yield a material coupling coefficient of $k^t_{33} = 0.40 \pm 0.03$. It is slightly lower than the material coupling coefficient, which we achieved with our high temperature, processed lead titanate zirconate. For randomly oriented PZT material, coupling coefficients of $k^t_{33} = 0.43 \pm 0.03$ were measured. For strongly (001)-oriented films, material coupling coefficients of $k^t_{33} = 0.57 \pm 0.03$ were obtained.

The low-temperature-processed PZT that is applied in these piezoelectric switches shows high breakdown fields of 1.5 MV/cm, low leakage currents of 10^{-10} A/mm^2 at room temperature, and 0.25 MV/cm. Based on accelerated lifetime measurements (see above section on high-k integrated devices) extrapolated lifetimes at 85°C and 0.25 MV/cm of more than 25 years have been determined. These data demonstrate that the piezoelectric thin-film materials applied here for piezoelectric switches show excellent piezoelectric properties as well as excellent dielectric reliability.

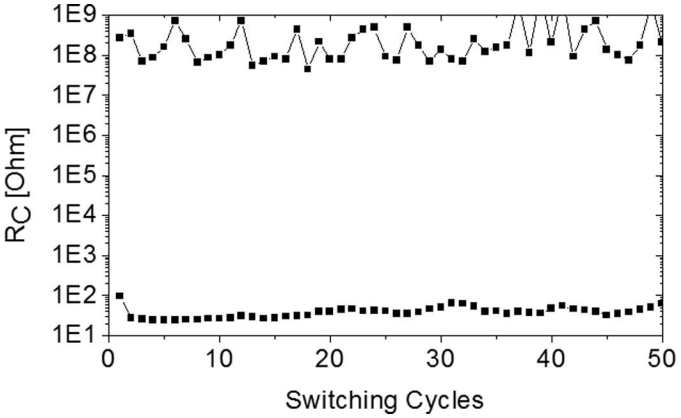

Fig. 13. Contact resistance in the closed and in the open state for 50 switching cycles.

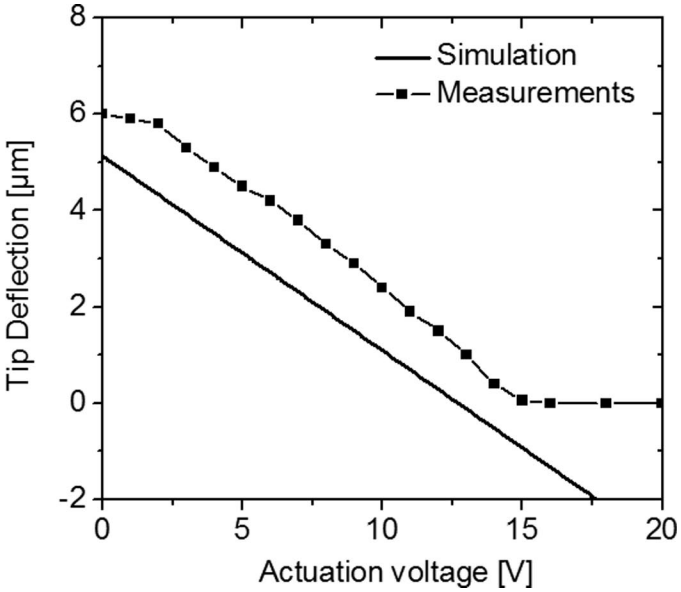

Fig. 14. Tip deflection of the piezoelectric switch for different operating voltages. Interferometric measurements (squares) and simulation results (solid line) are shown. At zero deflection contact is made. Note that no contact is included in the simulations.

In Fig. 12, a 3-D height distribution of a processed switch is shown. The picture is taken by means of a white light interferometer. Because of a gradient in the residual stress of the layers, the tip of the cantilever is pointing upward by several microns. On the left, the operating voltage is switched off and the contacts are open. When applying 25 V across the PZT (right plot), the switch closes and an electric contact is made. These piezoelectric thin film switches have also been tested with respect to their mechanical reliability and showed more than 10^6 switching cycles without mechanical degradation.

In Fig. 13, the open and closed contact resistances are shown for 50 switching cycles. The actuation voltage is 30 V and the voltage across the galvanic contacts is 0.5 V. As can be seen, the contact resistance varies. More detailed investigations are carried out on the contract resistance as a function of processing and design.

In Fig. 14, the measured tip deflection is compared with simulation results with good agreement. Because the residual stress gradient of this switch is smaller than the one in Fig. 12, the opening gap is smaller and hence the contact is already closed at 15 V. The simulations are based on the 1-D Euler-Bernoulli bean equation for an inhomogeneous layer stack. To fit the measured data, a piezoelectric constant of d_{31} $E = -4$ C/m^2 was used with E being the Young's modulus of the PZT layer. Further investigations are ongoing.

Making use of stroboscopic measurements, the mechanical opening and closing switching times have been determined for our thin-film piezoelectric switches on several devices. The opening gap of several switches is closed in less than 10 µs and fully opened within 30 µs. The electric contact is broken in less than 20 µs. Piezoelectric switches can be opened and closed very fast.

V. Conclusion

Ferroelectric thin-film devices based on lead titanate zirconate were investigated for integrated capacitors. They enable a new platform of integration of passive with active functions with integrated capacitors, resistors, and ESD protection diodes in small chip-scale package modules. These modules offer a board space saving of up to 80% and play an important role in present and future generation mobile communication systems. Capacitors with capacitance densities of 20 to 100 nF/mm^2 and breakdown voltages of 90 to 150 V have been realized. For capacitance densities of more than 80 nF/mm^2, stacked capacitors were used. These high-performance capacitors have been integrated with high-performance resistors and ESD protection diodes. These ferroelectric thin-film capacitors with high capacitance density of up to 100 nF/mm^2 and high breakdown voltages of more than 90 V are a major accomplishment in the world of passive components and are not reported by any other passive integration technology. These capacitors offer lifetimes of more than 10 years at 5 V operating voltage and 85°C. This new class of high-k integrated discrete devices is running in mass production at NXP Semiconductors.

Dielectric layers based on $Ba_{1-x}Sr_xTiO_3$, which are processed on Pt electrodes on Si, enable tunable capacitors with relative permittivities of 400, more than 35% tuning at only 3 V and high quality factors above 30 at 1 GHz. These devices are attractive for adaptive impedance-matching networks and tunable filters.

Piezoelectric thin films with high piezoelectric coupling coefficients and high breakdown voltages as well as excellent lifetimes are investigated for galvanic switches. Thin-film switches with first-contact resistance measurements and high switching speeds of 5 to 20 µs have been demonstrated. Measured tip deflections are compared with analytical simulation results and show good agreement.

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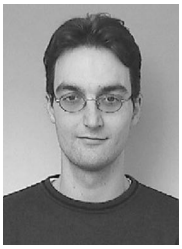

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