# Introduction of Ramp-Type Technology in HTS Quasiparticle Injection Devices

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**Abstract—Injection of quasiparticles with an energy larger than the superconducting gap into a superconducting strip results in breaking of Cooper-pairs and hence the suppression of the superconducting properties. Experiments using planar injection devices made of HTS materials with various barrier materials showed current gains varying from 2 up to 15 at 77K. By changing the junction size and therefore the superconducting volume the current gain could be increased. A further reduction of the junction volume is very difficult using the planar device geometry. However, by applying the ramp-type technology it is possible to reduce the junction volume by at least one order of magnitude and a further increase in current gain is expected. Another advantage of this technology is the formation of in-situ barriers and electrodes and hence a better control of the junction characteristics should be possible, also the compatibility with the processes involved making RSFQ devices can be interesting for later applications. We have fabricated ramp-type injection devices, using various types of barriers. Characterization of these devices has been performed and the results of these experiments will be presented and discussed.**

## I. INTRODUCTION

Quasiparticle injection devices are one set of devices from a family that use various mechanisms for suppressing the superconducting properties in a small volume of high temperature superconductor (HTS) [1]. In the case of current injection devices, high energy electrons are injected through a barrier into a small superconducting volume. Depending on the type of barrier used the injected electrons can be spin-polarized [2] or just normal electrons. In the first case a current gain of up to 35 at 77 K has been reported [3] however this type of device will be rather slow due to magnetic suppression of the superconducting properties. If non-magnetic barriers, such as $PrBa_2Cu_3O_7$ (PBCO) or $SrTiO_3$ (STO) are used, a suppression of the superconducting properties can also be achieved. Depending on the barrier material current gains ranging from 2 to even 15 at 77 K have been achieved [4]. From simple theory it can be shown, that a reduction of the active volume can result in an even larger increase in current gain, however when one wants to achieve this in the commonly used planar device geometry practical problems are encountered. Therefore the use of a ramp to define the active area of the device leads to a more complex production process. Another reason to introduce the ramp-type technology is the process compatibility with possible applications areas, such as RSFQ, that use the same technology.

In this paper we report the first steps implementing the ramp-type technology, problems encountered and solutions that were brought up.

## II. THEORY

Taking the so called Rothwarf Thaylor equations [5] as a first approximation for the dynamics of the non-equilibrium state that is formed upon injecting quasiparticles, after linearisation one can write

$$\frac{d}{dt}n_{qp} = \frac{J_{inj}}{ed} - \frac{\Delta n_{qp}}{\tau_{eff}} \tag{1}$$

where $n_{qp}$ is the number of quasiparticles in the injection volume, d is the thickness of the track and $\tau_{eff}$ is the effective time constant which results from combining all the different recombination processes that play a role in the process. If we then look at the steady state solution we get

$$\Delta n_{qp} = \frac{J_{inj}}{ed}\tau_{eff} \tag{2}$$

An estimate for the change in the number of quasiparticles needed to completely suppress the critical current in the superconducting volume can be derived from the formula given by Owen & Scalapino [6], giving the gap suppression as function of the change in quasiparticle density

$$\Delta(x) = \Delta_0(1-2x) \tag{3}$$

with

$$x = \Delta n_{qp} / 4N(0)\Delta_0 \text{ for } x << 1 \tag{4}$$

where $N(0) = 10^{22}cm^{-3}eV^{-1}$ is the single spin particle density at the Fermi level and $\Delta_0 \approx 20meV$ is the zero temperature energy gap for DBCO [1]. Assuming that for $J_c \to 0$ we have $\Delta \to 0$ we get $x = \frac{1}{2}$ and defining the current gain $K_C$ as:

$$K_C = I_c / I_{inj} = J_c wd / J_{inj} wL \tag{5}$$

where w is the width of the track, d is the thickness and L is the length of the track respectively, we get the following estimation for the current gain:

$$K_C = \frac{J_c}{64L}\tau_{eff} \tag{6}$$

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However in this estimation the effect of the energy of the electrons due to voltage over the injection barrier is not taken into account. When this injection voltage is added we can write for (6):

$$K_C = \left( \alpha \frac{V_{inj}}{\Delta} + 1 \right) \frac{J_c}{64L} \tau_{eff} \qquad (7)$$

where $\Delta$ is the energy gap, $V_{inj}$ is the injection voltage over the barrier and $\alpha$ is an efficiency factor.

From our measurements on planar devices we consider that this injection voltage can be very important to achieve high gains. The best working planar devices were made using a STO barrier having an injection resistance of a few hundred k$\Omega$ till a few M$\Omega$ resulting in injection voltages of a several volts [4]. These high injection voltages directly show that it will be very difficult to obtain any voltage gain and hence power gain, because the output voltages of these devices will be rather small due to the low ohmic characteristic of the device channel.

As can be seen from (6) the expected current gain is inversely proportional to the length of the track. In order to increase the current one would like to have the track length as short as possible and keeping the other characteristics of the devices the same. Reduction of the track length of the device is in our case not really possible below 5 μm due to our pattern process and also getting contact to the injection electrode will become difficult if one further reduces the injection area. However when the so called ramp-type technology is implemented it should be possible to reduce this track length to a few hundred nm. Thus a possible increase in current gain of even two orders of magnitude could be possible if the other characteristics of the devices can be kept the same.

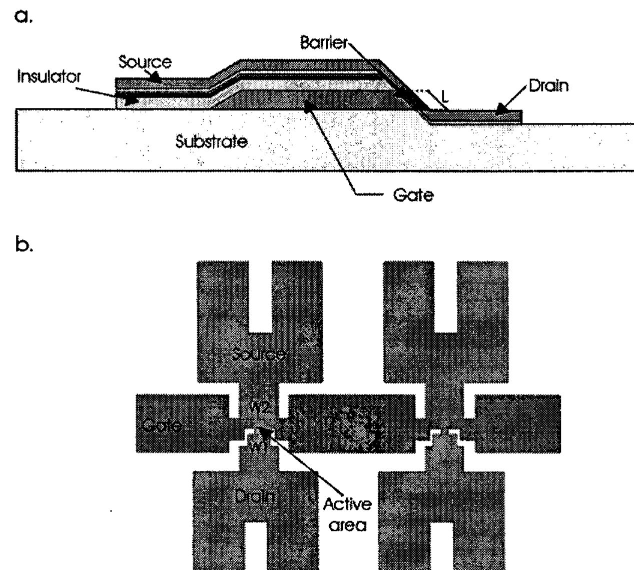


Fig. 1. Schematic of the ramp-type injection design. Where a) depicts a side view of the device showing all the separate layers and b) gives a top view of two neighboring devices, clearly showing the common gate electrode.

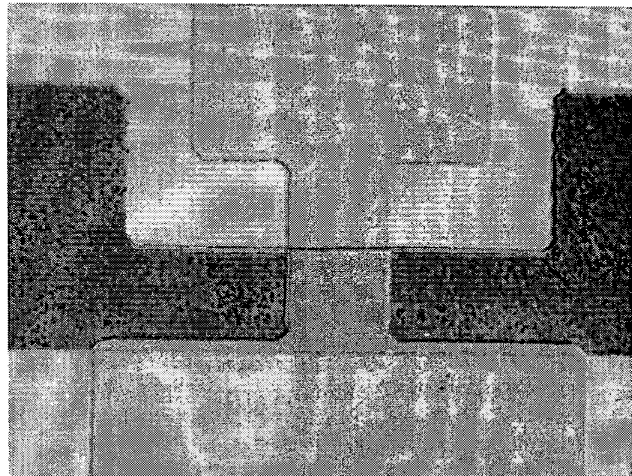

Fig. 2. Photograph of an actual ramp-type injection device were one can clearly see the gate electrode (dark one) and both the source (bottom) and drain (top). Also both ramps are clearly visible, were the injection area is on the smaller ramp.

## III. DEVICE FABRICATION

The films used were all made by off-axis RF-magnetron sputtering and the devices are patterned using standard optical photolithography. The etching was done using a Kaufmann 3 cm ion-gun.

Both the planar as well as the ramp-type injection devices consist of three terminals, for which the ramp-type devices gives rise to the introduction of a second ramp in order to be able to contact the injection electrode, hereafter called gate electrode. The top electrode is for convenience divided into a source- and a drain-side as is also the common description in semi-conductor technology. A schematic of the ramp-type injection devices is shown in Fig. 1. As can be seen in this figure we have chosen a common gate electrode for all the devices to limit the number of contact pads needed and to simplify the mask design. During etching of the second ramp, where the injection area will be created, we partly etch into the substrate to ensure a well defined injection area. By etching far enough into the substrate we can regulate that the top of the drain electrode is lower than the bottom of the gate electrode and hence we really define our active region, as is shown in Fig. 1a.

For the insulating layer between the SD-channel and the gate electrode we used a double layer of STO and PBCO. The STO is used because of the good insulating properties and the PBCO was used to increase the total thickness of the insulating layer without creating problems with the oxygenation of the gate electrode afterwards.

As barrier material both STO and PBCO were used. The best results are expected with the use of STO as barrier material because from experiments with the planar devices it was shown that high resistances and hence high injection

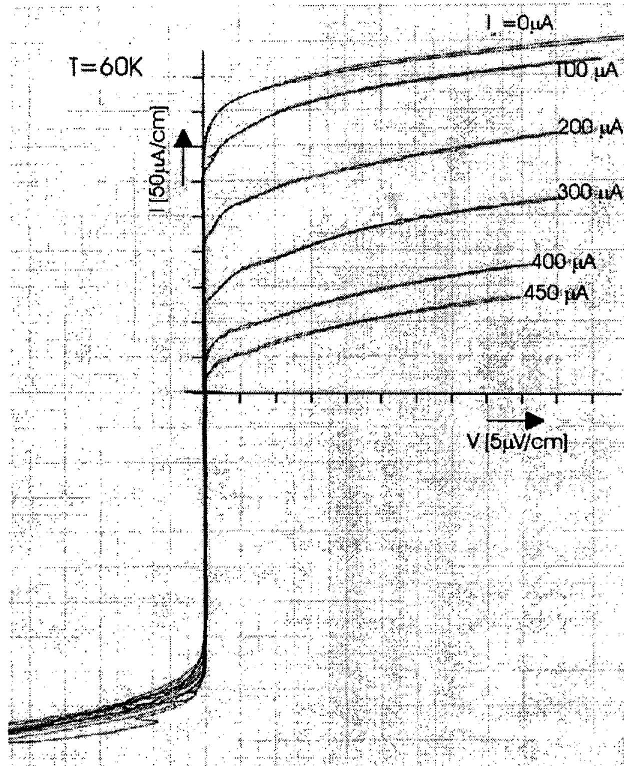


Fig. 3. IVCs of a ramp-type device with a STO barrier for different injection currents at 60K The nominal thickness of the barrier was 15 nm having a injection resistance of 850 Ω.

voltages resulted in the largest gain, subscribing the necessity of modulation of the current gain relationship as suggested in (7). The use of STO gave some limiting factor for the thickness of the STO insulator layer to ensure good separation between gate-electrode and source-electrode.

## IV. EXPERIMENTAL

The characterization of the devices was done using a standard four-point measurement setup to measure the Current-voltage characteristics (IVC) with a standard He flow-cryostat to control the temperature. The IVCs where measured over the SD-channel and the injection current, $I_G$, was flowing from the gate-electrode to the current branch of the drain-electrode. So far no real current gain has been observed, however the fabrication process and the film quality has been improved so that we now see pure current summation as shown in Fig. 3. This indicates that the injection ramp is the real limiting area and homogeneous injection through the barrier occurs and because of the rather small injection resistance this results in the observed current summation effect.

## V. DISCUSSION

As mentioned before the implementation of ramps in the design results in a more complex structure and hence a better control of the film growth and subsequent patterning steps is needed. We would like to address the various critical points in the design separately.

### *A. Overlap area*

One of the first points that have to be addressed is the size of the overlap area, one wants to minimize this area to minimize the changes of shorts and to minimize the capacitance that can be a limiting factor for later applications. However there are various factors that are limiting the minimal size of this area. Firstly the underlying gate electrode should have such dimensions that the critical current of this track is much higher than the possible injection currents that are needed to suppress the current in the source-drain channel (SD-channel). Thus the minimal width of the gate electrode should be larger than the maximal injection area. Secondly, the widths of the ramps and hence the widths of the tracks crossing the gate electrode are also limiting the overlap area. All this factors result in an overlap area ranging in size from 250 $\mu m^2$ up to 400 $\mu m^2$, which asks for very smooth and especially outgrowth free layers to prevent shorts in the insulation between the gate electrode and the SD-channel.

### *B. Relation between ramp sizes*

To ensure that the critical current in the SD-channel is defined by the injection-ramp, the width (W1 in Fig. 1) of this ramp should be smaller than the width of the other ramp (W2 in Fig. 1). We choose for the second ramp to be a factor 5 larger than the injection ramp for that device. This larger width of the ramp results is a big increase of the overlap area as mentioned before, and thus requires an even better control of the surface morphology of the insulating layer. The difference in ramp width is clearly visible in Fig. 2.

Another problem that arises is the intrinsic roughness of the ramp due to terraces that are formed during etching of the ramp. From earlier study [7] it was shown that with careful processing of the ramps a lower limit for the barrier thickness of 8 nm is needed to prevent the formation of pinholes in the barrier. This intrinsic roughness however will always give rise to a rather significant spread in effective barrier thickness over the ramp and hence can lead to the formation of preferred current channels giving a non-uniform injection of the current.

## VI. CONCLUSION

We demonstrated that it is possible to convert the planar injection design into a ramp-type design, however the more complex design gave rise to some process difficulties. So far we have been able to solve most of the problems by redesigning the device structure and careful control of the film growth. The creation of a good injection barrier on the ramp is still one of the mayor problems. We expect to

improve the quality of the injection barrier resulting in real suppression of the critical current in stead of the thus far observed pure current summation effect.

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