Stress-Induced Leakage Current in p^+ Poly MOS Capacitors with Poly-Si and Poly-Si_{0.7}Ge_{0.3} Gate Material

V. E. Houtsma, J. Holleman, C. Salm, F. P. Widdershoven, and P. H. Woerlee

Abstract—The gate bias polarity dependence of stress-induced leakage current (SILC) of PMOS capacitors with a p^+ polycrystalline silicon (poly-Si) and polycrystalline Silicon-Germanium (poly-Si_{0.7}Ge_{0.3}) gate on 5.6-nm thick gate oxides has been investigated. It is shown that the SILC characteristics are highly asymmetric with gate bias polarity. This asymmetric behavior is explained by the occurrence of a different injection mechanism for negative bias, compared to positive bias where Fowler–Nordheim (FN) tunneling is the main conduction mechanism. For gate injection, a larger oxide field is required to obtain the same tunneling current, which leads to reduced SILC at low fields. Moreover, at negative gate bias, the higher valence band position of poly-SiGe compared to poly-Si reduces the barrier height for tunneling to traps and hence leads to increased SILC. At positive gate bias, reduced SILC is observed for poly-SiGe gates compared to poly-Si gates. This is most likely due to a lower concentration of Boron in the dielectric in the case of poly-SiGe compared to poly-Si. This makes Boron-doped poly-SiGe a very interesting gate material for nonvolatile memory devices.

Index Terms—Fowler–Nordheim tunneling, oxide reliability, PMOS, poly-SiGe, SILC, valence band tunneling.

I. INTRODUCTION

STRESS-INDUCED LEAKAGE CURRENT (SILC) limits the scaling of the gate oxide thickness for nonvolatile memories. Until now, SILC was studied mainly for n^+ -doped polycrystalline silicon gate material [1], [2]. Recently a larger tunnel barrier height and different conduction mechanism for gate injection have been proposed for Boron-doped p^+ -gates [3], [4]. SILC in p -type gate devices has not been studied in detail yet.

In this paper the DC-SILC characteristics of PMOS capacitors with p^+ -gate material and 5.6-nm oxide thickness are studied. P^+ -gates with polycrystalline silicon (poly-Si) and polycrystalline Silicon-Germanium (poly-Si_{0.7}Ge_{0.3}) [3], [5] were used to study the influence of the gate workfunction on gate current and SILC currents. Asymmetric SILC (gate bias

polarity) and reduced SILC for poly-Si_{0.7}Ge_{0.3} gate devices were observed.

II. EXPERIMENTAL

PMOS capacitors were fabricated on 10 Ω -cm n -type silicon substrates. A high-quality gate oxide with 5.6 nm thickness (ellipsometric) was grown in diluted dry oxygen. Undoped poly-Si and poly-Si_{0.7}Ge_{0.3} layers (200 nm thick) were deposited using a LPCVD system [6]. Gate doping was done by a 20 keV, $2.5 \cdot 10^{15} \text{ cm}^{-2}$ BF_2^+ implant followed by an anneal at 850 °C for 30 min. Electrical stress has been applied on $A = 4.0 \cdot 10^{-4} \text{ cm}^2$ MOS capacitors using constant current stress conditions of $J_{\text{stress}} = \pm 0.1 \text{ mA/cm}^2$. DC-SILC was measured in a similar way (see [1]). The oxide electric field was determined by integration of the quasi-static capacitance–voltage (C – V) curves using (1)

$$E_{\text{ox}}(V_g) = \frac{1}{\epsilon_{\text{ox}}} \int_{V_{fb}}^{V_g} C(V'_g) dV'_g. \quad (1)$$

III. RESULTS AND DISCUSSION

Quasi-static C – V curves for capacitors with p^+ poly-Si and p^+ poly-SiGe gate show a shift of the flatband voltage from $V_{fb} = 0.82 \text{ V}$ (poly-Si) to $V_{fb} = 0.60 \text{ V}$ (poly-SiGe) [7], which agrees well with previous data [3], [5]. It is caused by a shift in valence band position [5].

Fig. 1 shows the J – E_{ox} characteristics of unstressed poly-Si and poly-SiGe capacitors for substrate-($+V_g$) and gate-injection ($-V_g$) conditions. The onset of conduction for $-V_g$ occurs at significantly higher oxide field ($\approx 1.5\times$) than for $+V_g$ condition. Note the difference between poly-Si and poly-SiGe for $-V_g$. For $+V_g$, the J – E_{ox} curve can be fitted with the standard Fowler–Nordheim (FN) expression with a barrier height of $\phi_B = 3.2 \text{ eV}$. For $-V_g$, a fit with an FN expression cannot be obtained unless unphysical fit parameters are used.

To evaluate the conduction mechanism for gate injection, the gate, diode, and substrate currents were measured by means of carrier separation technique applied to gate-controlled diodes with p^+ -diode and n -substrate grounded [7]. For the $-V_g$ condition, both the substrate and diode currents are larger than the gate current [7]. The larger substrate current compared to the gate current ($I_{\text{sub}} > 2 \times I_{\text{gate}}$) indicates that an avalanche process is taking place. This is not expected when hole tunneling from the substrate to the gate dominates the gate

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V. E. Houtsma, J. Holleman, and C. Salm are with MESA Research Institute, University of Twente, 7500 AE Enschede, The Netherlands.

F. J. Widdershoven is with Philips Research Laboratories, 5656 AA Eindhoven, The Netherlands.

P. H. Woerlee is with MESA Research Institute, University of Twente, 7500 AE Enschede, The Netherlands and also with Philips Research Laboratories, 5656 AA Eindhoven, The Netherlands.

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Fig. 1. J - E_{ox} measurements of unstressed p^+ poly-Si and poly-Si_{0.7}Ge_{0.3} gate MOS capacitors on 5.6-nm thick gate oxides.

current. It appears that the gate current at $-V_g$ is caused by electron injection from the gate. There are two possible mechanisms for electron injection from the gate. Firstly, tunneling of minority carriers i.e., electrons in the conduction band (MCT) from the gate could occur at high negative gate bias when active gate doping is low. The band bending (gate depletion) at the gate-SiO₂ interface for $-V_g$ increases the electron surface concentration.

For high active gate doping at the gate-SiO₂ interface, as in our sample, this mechanism is less probable since gate depletion is reduced. Moreover, temperature dependent measurements on the J - E_{ox} characteristics reveal no n_i^2 temperature dependence, thus ruling out MCT. A second possibility is valence band tunneling (VBT) [3], [4]. Gate currents are either influenced by the workfunction for valence band tunneling or by the bandgap of the gate material for the MCT mechanism. It appears that the carrier injection mechanism in p^+ -poly gate devices is different for gate and substrate injection conditions. The $+V_g$ mechanism is similar to that for n^+ -poly gate devices, i.e., FN electron tunneling from the substrate conduction band. For gate injection, a significantly larger oxide field is required to obtain the same tunneling current as for substrate injection conditions. This will influence the SILC characteristics— results will be shown below.

In Fig. 2, the J - E_{ox} characteristics of p^+ poly-Si gate devices are shown after various stress intervals. For $-V_g$ injection, SILC becomes apparent at much higher E_{ox} . Furthermore, the field dependence is different from that at $+V_g$, i.e., non-FN-like. At comparable oxide field, the SILC is orders of magnitude smaller for $-V_g$ stress than for $+V_g$ stress. Hence, there is a strong asymmetry of the SILC currents with stress polarity. This is different from n^+ -poly gate devices [1], [2], [7], where SILC is almost symmetric with gate polarity. For $+V_g$, the SILC current after stress can be described well by an FN expression with an effective barrier height of $\phi_B = 0.9$ eV. This is similar to values obtained for n^+ -poly devices [1]. For gate injection, the SILC characteristics cannot be described by the FN expression with fixed barrier height. An (unphysical) FN fit of the SILC current results in a barrier height around $\phi_B = 2$ eV, indicating a much stronger field dependence and different tunneling mechanism.

Fig. 2. J - E_{ox} curves of p^+ poly-Si gates before and after stress. Injection of stress takes place from the substrate for $+V_g$ and from the gate for $-V_g$ under constant current stress conditions of $J_{stress} = \pm 0.1$ mA/cm².

Fig. 3. J - E_{ox} curves of p^+ poly-Si_{0.7}Ge_{0.3} gates before and after stress. Injection of stress takes place from the substrate for $+V_g$ and from the gate for $-V_g$ under constant current stress conditions of $J_{stress} = \pm 0.1$ mA/cm².

It has been observed that SILC is proportional to the neutral trap density created during stress [1], [2], and models based on inelastic trap-assisted-tunneling (TAT) are used to describe SILC [9]. The observed bias asymmetry in SILC could possibly be related to a larger tunneling barrier height for TAT or a different position of the traps for the $-V_g$ stress conditions. In Fig. 3, the J - E_{ox} characteristics of the poly-SiGe devices are shown. For $+V_g$ conditions, the SILC current is strongly reduced compared to the p^+ poly-Si reference devices. For $-V_g$ conditions, the SILC current is significantly larger at the same oxide field than for the p -type poly-Si device. The reduced SILC of the poly-SiGe devices for $+V_g$ stress could be the result of a reduced Boron incorporation in the gate oxide. A larger solid solubility and smaller diffusivity of Boron in poly-SiGe lead to a reduced incorporation of Boron in the dielectric [3], [6]. Hence, a lower neutral trap density and reduced SILC for poly-SiGe gates is expected [1], [2], [10]. This is supported by the increased charge-to-breakdown of furnace-annealed poly-SiGe devices [3], [7]. The increased SILC observed for the $-V_g$ condition for poly-SiGe compared to p^+ poly-Si devices could be caused by a

shift in the valence band position. The valence band shift of poly-SiGe reduces the barrier height for tunneling to traps and hence leads to an increase of SILC.

IV. CONCLUSIONS

In summary, both the position of the valence band of the gate material and Boron penetration into the gate oxide strongly influence the SILC characteristics. The reduced SILC observed in p^+ -poly devices for $-V_g$ polarity could be attractive for nonvolatile memory devices. Boron-doped poly-SiGe may be a very interesting gate material due to a low SILC at $+V_g$ and better gate oxide quality.

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