Single-charge transport in ambipolar silicon nanoscale field-effect transistors

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We report single-charge transport in ambipolar nanoscale MOSFETs, electrostatically defined in near-intrinsic silicon. We use the ambipolarity to demonstrate the confinement of either a few electrons or a few holes in exactly the same crystalline environment underneath a gate electrode. We find similar electron and hole quantum dot properties while the mobilities differ quantitatively like in microscale devices. The understanding and control of individual electrons and holes are essential for spin-based quantum information processing. © 2015 AIP Publishing LLC.

Inspired by the idea of using spin qubits in coupled quantum dots (QDs) for quantum computation, several semiconductor platforms have been explored to electrostatically define quantum dots, e.g., GaAs/AlGaAs heterostructures, Si-Ge nanowires and nanocrystals, Si/Ge heterostructures, and silicon. Silicon is particularly a very promising candidate for a scalable quantum computer. First, it is at the heart of today’s integrated-circuit technology, and second because its weak spin-orbit coupling and hyperfine interaction promise long spin lifetimes. Electron-spin coherence times of microseconds in natural silicon (which contains ~5% 28Si), and even up to seconds in isotopically purified 28Si have been reported. Holes have a much stronger spin-orbit coupling, enabling efficient electric-dipole spin resonance to manipulate the spin, as shown for electrons in GaAs and InAs, and for holes in InSb. Electrical control instead of magnetic control is particularly appealing for this purpose, because local, on-chip oscillating electric fields are much easier to generate than magnetic ones.

From a fundamental point of view, it is also worthwhile to investigate holes in silicon. In contrast to the 6-fold valley degeneracy of the conduction band, theory predicts a heavy-hole (m_l = 3/2) and light-hole (m_l = 1/2) sub-band, as well as a split-off sub-band in the valence band, which all have not been explored in this type of structures. First, single-hole QDs have been studied, e.g., in Si nanowire QDs, where the ground-state spin configuration and spin filling of the first four holes were determined. Recently, isolation of holes in gate-defined QDs in intrinsic silicon have been realized. Electrons and holes are mainly investigated in separate devices. Ambipolar devices, however, can be operated both in the electron and in the hole regime, as reported in materials such as graphene, carbon nanotubes, bottom-up grown Si nanowires, AlGaAs/GaAs heterostructures, Ge QDs, silicon-on-insulator (SOI), and black phosphorus. Because the 10 nm CMOS technology node is supposed to be fully operational by 2016 without suffering from the statistical nature of quantum mechanics, it is especially important to have a detailed understanding and control of confined charge carriers in silicon.

In this Letter, we first investigate electron and hole transport in nanoscale, ambipolar metal-oxide-semiconductor field-effect transistor (MOSFET) structures with a single gate in intrinsic silicon and then demonstrate confinement of either electrons or holes underneath an additional nanoscale bottom gate, being both suitable for qubits. The strength of our ambipolar device is the isolation of either charge carrier in a single device in exactly the same crystalline environment, i.e., defects, impurities, trapped charges, and Si/SiO₂ interface. We find the electron and hole QD to have the same source, drain, and gate capacitances as well as charging energies. However, the electron and hole mobilities estimated especially important to have a detailed understanding and control of confined charge carriers in silicon.
from transconductance plots differ by a factor of ~3, like in microscale devices. Unipolar electron and hole devices require fabrication of different devices and do not allow direct discrimination between device-specific physics and the different behavior of electrons and holes.

A schematic of our MOSFET device is shown in Fig. 1. A near-intrinsic Si(100) wafer (ρ > 10,000 Ω cm, corresponding to a n-type background doping of N ≈ 4 × 10^{11}/cm^3) is used as substrate. Source and drain regions are implanted with phosphorus (n++) and boron (p++) dopants, serving as electron and hole reservoirs, respectively, and ohmically contacted with sputtered Al (1% Si) electrodes. Gates are fabricated on top of a 10 nm thermally grown silicon dioxide using electron-beam lithography, electron beam evaporation, and lift-off. A common lead gate overlaps both implanted regions on the source and the drain side, see Fig. 1(a). The lead gate is made of a metal stack (10 nm Al/ 60 nm Pd) for practical fabrication reasons. Depending on the applied lead gate voltage V_L, either electrons or holes accumulate at the Si/SiO_2 interface, forming a two-dimensional electron or hole gas (2DEG/2DHG), respectively, as illustrated in Figs. 1(a) and 1(b). Measurements on similar MOSFET devices with a channel of 5 μm × 50 μm (width × length) give mobilities of μ_e ≈ 950 cm^2/Vs for electrons and μ_h ≈ 360 cm^2/Vs for holes at 4.2 K. All transport measurements in this work are performed at 4.2 K.

Typical ambipolar turn-on curves for devices with only a lead gate are shown in Fig. 2(a) (smallest part of the gate is about 200 nm long and 100 nm wide). The gate dependent source-drain current I_{SD} is measured at a source-drain voltage V_{SD} = 50 mV for 12 devices from one nano-fabrication batch. The green (red) dashed line is the average threshold voltage in the electron regime V_{th}^e = 1.4 ± 0.2 V (hole regime V_{th}^h = -2.10 ± 0.05 V) with the corresponding standard deviation indicated by the shaded area. Here, we define the threshold voltage V_{th} as the voltage where the source-drain current I_{SD} exceeds 0.1 nA. We distinguish three regimes of operation: (1) In the middle region where no current is measured, the Fermi level is in the band gap of silicon. (2) At the threshold voltage V_{th}^e, the Fermi level hits the conduction band (CB), and electron transport occurs for gate voltages V_L > V_{th}^e. (3) For gate voltages below the threshold voltage in the p-region, V_L < V_{th}^h, hole transport occurs since the Fermi level is pulled below the top of the valence band (VB). We find that the transconductance is about three times larger for electrons than for holes, consistent with the nearly three times higher electron mobility measured in microscale MOSFET devices.

For electrons, we measure threshold voltages between 1.2 V and 1.7 V, and for holes between −2.0 V and −2.2 V. The electron thresholds are closer to zero than the hole thresholds and vary more between devices. The exact reason for this threshold asymmetry around zero is not completely understood. The n-type background doping (N ≈ 4 × 10^{11}/cm^3) of the near-intrinsic silicon wafer is one possible explanation. At low temperature, the Fermi level shifts towards the CB edge even for shallow doping,34 resulting in a lower threshold voltage for electrons. But also the work function of the gate, consisting of a metal stack, as well as spurious oxide charges affect the threshold voltage. The asymmetry is most likely a combination of these effects of which we cannot determine quantitatively the individual contributions. A detailed analysis is beyond the scope of this work.

Before studying the functionality of an additional bottom gate (see inset to Fig. 2(b)), we first investigate its effect on the turn-on characteristics for 11 devices from one nano-fabrication batch. Electrical insulation of the bottom gate from the lead gate is achieved by partially oxidizing the Al bottom gate in open air for 5 min at ~150°C. All bottom gate devices are fabricated on the same Si wafer as the lead gate devices but in a different nano-fabrication batch. The turn-on curves are plotted in Fig. 2(b). Here, the same voltage is applied to the bottom gate V_B and the lead gate simultaneously: V = V_L = V_B. We find V_{th}^e = 1.3 ± 0.2 V and V_{th}^h = -2.1 ± 0.1 V, very similar to the devices with only a lead gate. The results in Fig. 2 demonstrate two things: (i) the ambipolar operation of our devices, as we can switch from electron to hole transport by changing the applied gate voltage and (ii) that adding a bottom gate does not influence the threshold voltages significantly.

Now we study the ability of the bottom gate to locally control the charge density in both the electron and the hole regime (Fig. 3(a)). First, we ramp V_L and V_B simultaneously to ± 3.5 V, well above the threshold voltage so that charge carriers can move freely from source to drain (indicated by triangles). We then sweep only the bottom gate voltage to 0 V, while keeping V_L at +3.5 V (−3.5 V) as indicated by green and red arrows in Fig. 3(a) for electrons and holes.
respectively. This creates a potential barrier underneath the bottom gate (indicated by circles) as evidenced by a decrease in the current. Below $|V_B| < 1.3 \text{ V}$, the potential barrier is high enough to block the source-drain current entirely and thus pinch off the channel.

The data are taken at $V_{SD} = 1 \text{ mV}$. In contrast to the measurements in Fig. 2 with larger $V_{SD}$, the electron turn-on here exhibits resonances just above the threshold voltage (black line). Resonances in the pinch-off curves are observed in both regimes. Reference 30 gives two explanations for resonances: (i) Resonances only present in the electron regime are attributed to negative charges trapped near the Si/SiO$_2$ interface, creating tunnel barriers only for electrons and not for holes, and (ii) resonances occurring for both charge carriers can be explained as single-charge tunneling events via a semiconducting island, resulting in Coulomb resonances.35,36

The presence of resonances only in the electron turn-on curve may be caused by negative charge traps (likely introduced during the electron-beam lithography process) or by a non-uniform density of states (DOS) in the reservoirs. Negative charge traps near the Si/SiO$_2$ interface can cause small local potential variations and create tunnel barriers for electrons. The small source-drain bias makes the measurement around the threshold voltage sensitive to these small variations. In this regime, the current is dominated by tunneling of electrons via Coulomb islands. A non-uniform DOS in the reservoirs results from the small lateral dimensions of the lead gate. Here, the reservoirs behave as a quasi-one-dimensional system,37 consisting of one-dimensional subbands which are more densely spaced for holes than for electrons. Thermal broadening of the states can thus explain the smooth turn-on characteristic in the hole regime and the observed

FIG. 3. Local control of charge density and dot formation: (a) Current $I_{SD}$ versus gate voltages $V_{gate}$ for a bottom gate device at $V_{SD} = 1 \text{ mV}$. For the turn-on curve (black line), $V_L$ and $V_B$ are increased simultaneously. Pinch-off curves are measured at fixed $V_L$ while $V_B$ is swept to zero; red (green) line for holes (electrons). Potential profiles are sketched for highly transparent (triangle) and opaque barrier (circles) for both charge carriers. Sweep directions are indicated by arrows. (b) and (c) Single-charge tunneling in the non-linear regime. Bias spectroscopies are taken at $V_L = -3700 \text{ mV}$ and $V_L = 3650 \text{ mV}$, respectively. (d) Schematic cross section and band structure illustrating the QD formed underneath the bottom gate. Dot occupancy numbers are indicated in the diamonds in (b) and (c). Data taken at 4.2 K.
resonances in the electron regime. Note that for both explanations resonances do not appear for larger $V_{SD}$, as observed in Fig. 2. However, a device dependent distribution of negative charge traps could also explain the larger spread in threshold voltage in the electron regime because more charge traps create additional Coulomb islands so that the higher probability of blocked current increases the threshold voltage.

The resonances in the pinch-off curves can be explained by quantum confinement, which affects both types of charge carriers and also clarifies the similar pinch-off voltages at $|V_{0\beta}^{e}| \approx |V_{0\beta}^{h}| \approx 1.3$ V. This is consistent with the picture of quantum dot formation underneath the bottom gate, as illustrated in Fig. 3(d), where the gate oxide on either side of the Al gate results in tunnel barriers to source and drain.\textsuperscript{38,39}

To further investigate these resonances, we perform energy spectroscopy. The numerical differential conductance $dI/dV$ is plotted versus $V_{B}$ and $V_{SD}$ in Figs. 3(b) and 3(c). Clear Coulomb diamonds can be identified in both the electron and the hole regime. Within each diamond, the QD is in Coulomb blockade and the charge occupancy is constant (indicated by $P, P + 1$ and $N, N + 1$). Adding one charge carrier increases the tunnel coupling significantly and blurs the diamond edges. In the electron regime, the higher occupancy numbers are difficult to distinguish, whereas more hole Coulomb diamonds can be identified because the tunnel coupling changes less over a few charge transitions. Outside the Coulomb diamond the QD electrochemical potential is in the bias window and single-charge tunneling takes place through the QD. The two slopes of the diamond edges of the first charge transition are the same for electrons and holes: $\alpha = C_{B}/C_{S} = 0.28$ and $\beta = -C_{B}(C - C_{S}) = -0.57$, where $C$ is the total QD capacitance and $C_{B}$ ($C_{S}$) is the capacitance from the bottom gate (source) to the dot.\textsuperscript{35} Additionally, the transitions $P + 1 \rightarrow P$ and $N \rightarrow N + 1$ exhibit lines of increased conductance parallel to the diamond edges caused by resonant tunneling processes.\textsuperscript{40}

For this type of device, charging energies ($E_C$) have been reported of typically 5–12 meV for electron\textsuperscript{41} as well as hole\textsuperscript{21,22} quantum dots. Here, $E_C$ of the first observable diamond is $\sim 20$ meV in both regimes. The large $E_C$ and the sharp opening of the last diamond in both regimes may be interpreted as depletion of the last charge carrier. However, charge sensing\textsuperscript{42,43} or a highly tunable QD structure\textsuperscript{41} is necessary to exclude other explanations. The same $E_C$ and QD capacitances for both charge carriers are a strong indication that we load the same QD with either electrons or holes.

Ever since it has been shown that electrons can be confined in gate-defined silicon quantum dots,\textsuperscript{9} these structures have been studied intensively\textsuperscript{12} because of the promising properties of silicon for quantum computation.\textsuperscript{13} A breakthrough was achieved recently by Veldhorst et al.\textsuperscript{39} who created a two-qubit logic gate in silicon using spin qubits. While the latter experiment uses electrons confined underneath a single gate electrode, we have demonstrated here the capability to isolate either electrons or holes underneath a single gate electrode. This ambipolarity provides the opportunity for the understanding and direct comparison of both electron and hole spin qubits in silicon quantum dots and thus pushing the search for the most suitable qubit for future quantum information processing.

After completing these measurements, we became aware of experiments on similar device structures elsewhere.\textsuperscript{44}

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