Designing analog circuits in CMOS

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The evolution in CMOS technology dictated by Moore's Law is clearly beneficial for designers of digital circuits, but it presents difficult challenges, such as lowered nominal supply voltages, for their peers in the analog world who want to keep pace with this rapid progression. This article discusses a number of significant items for analog designs in modern and future CMOS processes and possible ways to maintain performance.

Today's ICs are mixed-signal systems consisting of a large digital core, including a CPU or digital signal processor and memory, surrounded by all kinds of analog interface electronics like I/O, digital-to-analog and analog-to-digital converters, RF front ends and more. From an integration point of view, all these functions are ideally merged into a single die. In that case, the analog electronics are realized on the same die as the digital core and consequently must cope with the digital-dictated CMOS evolution.

From a high-circuit or system level, plain physics dictates that the power consumption of analog blocks is proportional to the level of signal integrity (for example, the signal-to-noise and distortion ratio) and to the signal frequencies. In other words, increased performance for analog circuits comes at the cost of higher power consumption. A proportionality constant between the actual and minimum power consumption takes into account things like implementation overhead, margins in operating conditions and device spread (see A.J. Annema, "Analog Circuit Performance and Process Scaling," IEEE tr. CAS II, June 1999, 711-725).

The relative impact of the implementation overhead, however, tends to significantly increase with lowering supply voltages. Hence, for a given power budget, the performance drops while migrating to newer technologies, just because of the lower supply voltage. This is probably the most dominant effect that complicates analog designs at low supply voltages.

Apart from issues at a higher-circuit or system level, the bare-transistor properties also change with CMOS technology evolution. At constant voltage, headroom dc properties, such as transconductance per current and harmonic content per current, are hardly changed over technologies. If, however, the quiescent V_{ds} and the signal swing are proportionally decreased with the nominal supply voltage, the harmonic-distortion components of transistors increase drastically with newer process generations. At the circuit level, this can be compensated for by using regulated cascades. However, they are harder to fit within decreasing supply voltages. Such ac parameters as junction capacitances and gain-bandwidth products improve with technology evolution, allowing better HF and RF performance.

Besides its impact on conventional properties of circuits and devices, the current CMOS evolution introduces several new problems in analog design. One of the new phenomena is gate leakage (see R. van Langevelde et al., "Gate current: Modelling, DL extraction and impact on RF performance," IEDM 2001 Technical Digest, 289-292). Gate current mainly depends on gate source bias and gate size. Effects of gate leakage include input bias currents, gate leakage mismatch and shot noise (see A. Scholten et al., "Compact modeling of drain and gate current noise for RF CMOS," IEDM 2002, Technical Digest).

Input bias currents due to gate leakage are very similar to the well-known base currents in bipolar technologies and hence the solutions known for bipolar circuits can be applied to analog CMOS circuits with leaky gates. The big difference between bipolar and CMOS design is that in CMOS the width and length can be selected—and in analog designs are optimized—while in bipolar designs only the emitter area (equivalent to MOSFET width) can be set and the base width (equivalent to MOSFET length) is fixed. The impact being that in ultradeep-submicron processes, long CMOS transistors that are frequently required in conventional analog circuit

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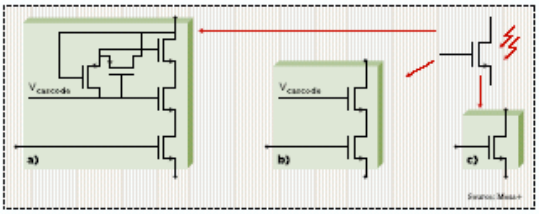

Ways to implement high-voltage-tolerant transistors in standard CMOS: a) a composite MOSFET that implements a retractable cascode b) a composite MOSFET employing a single (thick-oxide) cascode c) a single thick-oxide transistor.

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mats (cf. GDSII) need to be created to transfer information from one tool to another. Ease of use is a must. For example, library translations should not be visible to a designer. Collaboration between technology and EDA toolhouses is needed to provide seamless, reliable and tested design environments. To make significant strides in embedding, more effort is still needed to develop practical substrate-noise-modeling tools.

Cross-technology modeling like 3-D package modeling combined with RF IC simulations must be supported, which is extremely important for chip modules or stacking. Removing overhead from digital-domain designs, for example, requires better support for optimizing the hardware/software partitioning. In some areas, such as antenna design, the tools are in good shape, but new, more powerful and flexible simulation algorithms should be developed.

To achieve the best performance in handheld devices, any overhead in the system must be eliminated. Therefore, adaptive solutions are required. For example, in baseband platforms, dynamic voltage and frequency scaling, digital technologies to tackle leakage current, digital architectures applying asynchronous structures and usage of reconfigurable circuits should be applied. All possible means for preventing unnecessary switching in digital circuits and overhead in latencies need to be applied.

For top performance in handheld devices, any overhead in the system must be eliminated.

Flexibility will be key in the ability to implement all those numerous product categories in the future, since they cannot be based on one or two platforms. As a part of this strategy, enormous ASICs may not be the most probable choice, because they can be too expensive and more difficult to test. In addition to flexibility, power consumption, cost and time-to-market are important drivers. Whatever techniques are applied, the total cost of the product must be reasonable.

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designs may have a lower-than-unity current gain.

To quickly estimate the impact of gate leakage in an application, an evaluation of the type of input impedance of the transistor is valuable. The input impedance consists of the conventional input capacitance and the parallel "tunnel resistance" due to gate leakage. These two have opposite area dependencies, resulting in an area-independent fgate:

$$f_{gate}(V_{GS}, V_{DS}) = \frac{1}{2\pi C_{ox} r_{tunnel}}$$

$$\approx 1.5 \cdot 10^{15} \cdot V_{ox}^2 e^{\alpha \cdot t_{ox}} \quad t_{ox} \text{ in [nm]}$$

For signal frequencies higher than fgate, the input impedance is capacitive and the MOSFET behaves as a conventional MOSFET. Otherwise, it is resistive and the gate leakage is dominant. In 90-nanometer CMOS, typical values of this fgate are around 1 MHz. Due to gate leakage, MOS capacitances cannot be applied for certain low-frequency applications like phase-locked-loop filters and hold circuits. Taking into account the nonlinear behavior of the gate leakage, the droop rate of a "stored" voltage on a MOS capacitor, in [V/s], equals about the value of fgate (in [Hz]); then allowing, for example, a 1-millivolt drop on a sampled-and-held value, the usable hold time is in the low-nanosecond range at reasonable voltage levels in 90-nm technologies.

Another new effect of gate leakage is gate leakage mismatch, an effect that will exceed conventional matching tolerances, thereby requiring active cancellation techniques. Matching usually limits the achievable level of performance on analog circuits, like offsets in amplifiers and the accuracy in A/D converters, and the usual way to get a sufficient level of matching between MOS transistors is to simply spend area.

Gate leakage spread now comes as an extra spread source and places an upper bound on area that can be spent to decrease mismatch. We found that, excluding defectlike outliers, spread on gate leakage is proportional to the gate

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current level with a proportionality constant of roughly 0.03 divided by the square root of the area where area is the transistor's gate area.

Zooming in on conventional spread (see J. Dubois et al., "Impact of source/drain implants on threshold voltage matching in deep-submicron CMOS technologies," ESSDERC 2002) and on gate spread reveals that with spending more area the conventional spread contribution decreases but that at the same time the gate spread contribution increases. As a result, the maximum usable transistor area is limited by gate leakage spread. For 180-nm and 120-nm CMOS technologies this maximum area is very large and hence the reachable levels of matching are very good. However, for the 90-nm and 65-nm (estimated) generation this yields a maximum usable area of respectively 104 micron^2 and 103 micron^2; then gate leakage mismatch is a significant effect that limits the reachable matching figures. For these and newer CMOS generations, active mismatch cancellation techniques or matching insensitive designs will be required.

One strategy analog designers can adopt to deal with the use of lower supply voltages is to operate critical parts of the circuitry at higher supply voltages, by exploiting combinations of thin- and thick-oxide transistors.

Operating analog circuits outside nominal supply rails can solve the low-supply drawback of newer technologies. However, care should be taken with respect to lifetime issues: hot-carrier degradation due to high lateral electrical fields and gate oxide degradation due to high oxide voltages. Both effects can be minimized by a suitable limitation of terminal-pair voltages.

For circuits operating at "high" supply voltages, a number of robust high-voltage-tolerant transistors can be used (see the figure for three examples derived from high-voltage I/O circuits) and see A. J. Annema et al., "5.5-V tolerant I/O in a 2.5-V 0.25-μm CMOS technology," IEEE JSSC, 2001, 528-538. These HV transistors enable direct reuse of most older designs, running at supply voltages corresponding to the original design.

The easiest way is to use the (nowadays available) thick-oxide transistor, which is comparable with the two-generations-ago standard transistor. However, to benefit from technology scaling, the use of smaller devices, as in Figs. 1a or 1b, can be preferable to the use of thick-oxide transistors, as in Fig. 1c.

Transistors for which matching, 1/f noise or output impedance is critical may be realized with the compound structures in Figs. 1a and 1b. The disadvantage of these structures is that a suitable cascode voltage must be provided, which already must be present during powering up. This can be realized using internal cascode-voltage generators, at the cost of circuit complexity. If only a small part of a system is critical, one may choose to generate high voltage on-chip using charge pumps, but they are typically inefficient.

The three topologies were designed to handle the same maximum drain-source voltages. Under assumption of equal drain current, Vgs-Vt, and the same length for the lower devices, Fig. 1a is always preferred above Fig. 1b. Compared with Fig. 1c, 1a has higher Rout, lower 1/f noise, better matching—but lower fT—higher circuit complexity and higher gate current.

The decrease in 1/f noise is under the assumption that the type of gate oxide material is unchanged. So for application in, for example, a current source, the circuit of Fig. 1a is preferred, while for high-speed voltage amplification applications Fig. 1c is preferred. It must be noted that if the required voltage drop over the output terminals of Fig. 1a can be reduced by the rest of the circuit, then the upper cascode(s) can be removed, and 1c has hardly any speed advantage.

Unlike their digital counterparts, analog circuits can benefit from technology scaling if the supply voltages are not scaled down.

In conclusion, analog circuits can benefit from technology scaling if the supply voltages are not scaled down, unlike in their digital counterparts. High-voltage techniques are thus needed; Fig. 1 shows some ways to create high-voltage-tolerant composite transistors.