Extracting Energy Band Offsets on Long-Channel Thin Silicon-on-Insulator MOSFETs

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Abstract—Structural quantum confinement in long-channel thin silicon-on-insulator MOSFETs has been quantified using the temperature dependence of the subthreshold current. The results were compared with the shifts in the threshold voltage. Data were obtained from simulations after initial verification with experimental data. This study demonstrates that, with the temperature dependence of the subthreshold current, shifts in the valence and conduction band edge can be extracted distinctively from changes in mobility and density of states (DOS), making this method more accurate in assessing the impact of structural quantum confinement than the commonly used threshold voltage method. Furthermore, we show that, with additional C - V data, a possible change in mobility and DOS can be disentangled.

Index Terms—Conduction band, quantum confinement, subthreshold current, temperature dependence, ultrathin semiconductor body (UTB) devices, valence band.

I. INTRODUCTION

MULTIPLE-GATE devices such as FinFETs, double-gate (DG) and gate-all-around structures are commonly recognized as promising candidates for the next-generation CMOS technology [1]–[3]. These devices offer enhanced electrostatic control through the combination of multiple gates and an ultrathin semiconductor body (UTB). However, as the thickness of the UTB enters the deca-nanometer range, the impact of quantum mechanical effects on the device characteristics can no longer be neglected. In fact, structural carrier confinement [4] results in the separation of the energy levels within the conduction and valence bands, as schematically shown in Fig. 1 (a) and (b). The silicon body thickness t_{Si} is the key parameter determining the strength of the structural carrier confinement.

With the ultimate scaling of t_{Si} , fundamental semiconductor properties such as band gap E_g , effective density of states (DOS), and mobility μ are reported to deviate from their respective bulk values [5]–[7]. Hence, these quantities become *device* properties, rather than *material* properties. Furthermore, the threshold voltage of UTB devices with lowly doped body can be set by the gate work function [8]. In order to fully understand and tailor the band alignment, DOS, and mobility, accurate extraction and determination of their scaling behavior with, e.g., t_{Si} are required.

Manuscript received February 18, 2009; revised May 27, 2009. Current version published August 21, 2009. This work was supported by NXP Semiconductors, Eindhoven, The Netherlands. The review of this paper was arranged by Editor H. Jaouen.

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Digital Object Identifier 10.1109/TED.2009.2026201

Fig. 1. (a) Schematic cross section of a symmetric (long-channel) DG device with the corresponding cut along the (b) x - and (c) y -direction. (Dotted line) Energy subband minima originating from quantum confinement in the thin body. χ_s is the electron affinity, ϕ_m is the gate work function, and t_{oxf} and t_{oxb} are the front and back oxide thicknesses, respectively.

The effect of quantum confinement on the electrical UTB device characteristics is generally quantified using the shift in threshold voltage V_{TH} as metric [6], [9]–[12]. Hence, changes in the band alignment are expected to contribute to a shift in V_{TH} since, in case of band gap widening, a higher gate bias is required to obtain the same inversion charge density. However, whereas the *theoretical* V_{TH} is well defined [13], several definitions of the *experimental* V_{TH} exist [14], [15], e.g., V_{GS} corresponding to a fixed current level or the linearly extrapolated intersection of I_{DS} with the V_{GS} axis, starting from the maximum transconductance. In this paper, we adhere to the latter.

Regardless of which definition is used, the threshold voltage inherently denotes the transition from weak to strong inversion. Therefore, it is likely that, in addition to the band gap and the DOS, properties such as gate oxide thickness, mobility, and series resistance will also be incorporated in the threshold voltage. After all, those parameters determine the current in the strong inversion regime.

Recently, we reported another approach to electrically assess the impact of structural quantum confinement [16], demonstrating that the temperature dependence of the subthreshold current can be exploited to observe changes in the band alignment, mobility, and DOS.

In this paper, we extend the work presented in [16] and [17] by comparing the extracted band offsets obtained from the temperature dependence of the subthreshold current, denoted as $I_{\text{DS}}(T)$, with the conventional ΔV_{TH} method. Furthermore,

with additional simulations, we will show that, by exploiting the temperature dependence of the subthreshold gate *capacitance*, a t_{Si} -dependent change in DOS and mobility can be quantified.

This paper is organized as follows: First, the $I_{DS}(T)$ method will be outlined, followed by the initial verification of the simulations with previously obtained experimental data. The next section presents the comparative analysis carried out with simulations, followed by a discussion on the sensitivity of both the $I_{DS}(T)$ and ΔV_{TH} methods to change in several device and material properties.

As a general result, this study clearly points out that changes in band edge, mobility, and DOS can be extracted more accurately from temperature-dependent subthreshold current measurements, compared to shifts in the threshold voltage. Furthermore, additional *CV* analysis indicates that it is possible to disentangle a change in mobility and DOS.

II. BAND OFFSET EXTRACTION FROM $I_{DS}(T)$

The subthreshold current contains important information on several “intrinsic” device parameters, which can be accessed through its temperature dependence. The subthreshold current essentially originates from diffusion, as commonly given by

$$I_{DS} = \frac{\mu k_b T}{qL} Q_i(V_{GS}) \left[1 - \exp\left(-\frac{qV_{DS}}{k_b T}\right) \right] \quad (1)$$

in which μ is the low-field carrier mobility, k_b Boltzmann’s constant, T the absolute temperature, q the elementary charge, L the channel length, and V_{DS} the drain–source voltage; Q_i is the inversion charge density per unit area at the source side of the channel and is given by [8]

$$\begin{aligned} Q_i &= q t_{\text{Si}} N_C \exp\left(\frac{E_F - E_C}{k_b T}\right) \\ &= q t_{\text{Si}} N_C \exp\left(\frac{\chi_s - \phi_m}{k_b T}\right) \exp\left(\frac{qV_{GS}}{k_b T}\right) \end{aligned} \quad (2)$$

with N_C the DOS in the bulk conduction band, E_F the Fermi level at the source side of the channel, and E_C the conduction band edge. In this paper, Boltzmann’s approximation is assumed to hold, as well as the principle of “volume inversion” [18], which is justified by the low injection condition in the subthreshold regime. χ_s is the electron affinity, ϕ_m is the gate work function, and V_{GS} is the gate bias [see also Fig. 1(c)]. Equations (1) and (2) apply to fully symmetric devices, as well as DG UTB devices with strongly asymmetric front- and back-gate oxide thicknesses (i.e., $t_{\text{oxf}} \ll t_{\text{oxb}}$), provided that both gates are equally biased, as discussed in Appendix A.

In fact, the second part of (2) suggests that, for a given gate and drain bias, the difference in gate work function and conduction band edge can be extracted from the slope of the drain current versus the inverse temperature. Note that V_{GS} appears as an additive term in the exponent of (2). Hence, the applied V_{GS} must be subtracted when extracting the band offset from the slope of I_{DS} versus $1/T$. Furthermore, the low gate bias in the subthreshold ensures that the impact of *electrical*

carrier confinement, i.e., gate-induced quantization within the inversion layer, is negligible.

Similarly, for a p-type MOSFET, the difference in *valence* band edge and gate work function can be extracted. In general, any shift in band edge, i.e., the top of the source/channel barrier, as shown in Fig. 1(b), relative to the gate work function can be extracted using the exponential temperature dependence. In addition to quantization-induced band offsets, shifts in band alignment due to, e.g., strain or work function differences can be extracted. This work will focus on extracting band edge shifts stemming from structural carrier confinement in the ultrathin body.

To include the effect of carrier confinement, (2) should be replaced by the 2-D charge density, which is given by [19]

$$\begin{aligned} Q_{i,2D} &= q \cdot \frac{k_b T}{\pi \hbar^2} \sum_{k,n} m_{d,k}^* \exp\left(\frac{E_F - E_{k,n} - E_C}{k_b T}\right) \\ &= q \cdot \frac{k_b T}{\pi \hbar^2} \sum_{k,n} m_{d,k}^* \exp\left(\frac{\chi_s + E_{k,n} - \phi_m}{k_b T}\right) \\ &\quad \times \exp\left(\frac{qV_{GS}}{k_b T}\right) \end{aligned} \quad (3)$$

with

$$E_{k,n} = \frac{\hbar^2}{2m_{z,k}^*} \left(\frac{n\pi}{t_{\text{Si}}}\right)^2 \quad (4)$$

where $m_{d,k}^*$ and $m_{z,k}^*$ are the DOS and quantization effective masses belonging to valley k , respectively, and $E_{k,n}$ is the minimum of subband n relative to the bulk band edge.

The strength of structural confinement in thin silicon layers is governed by t_{Si} , as indicated by (3) and (4). The edges of both the conduction and valence bands are shifted with respect to the bulk band edges, due to the offset of (mainly) the first subband. In fact, the extracted band offsets presented in the course of this paper represent “effective,” or apparent, band offsets, i.e., the shift in band edge “averaged” in energy over the entire channel. In case of the silicon *conduction* band, the offset is predominantly determined by the first subband of the *unprimed* valley, which has the largest (longitudinal) mass along the quantization direction. The calculation of the theoretical effective valence band shift is less straightforward, due to its anisotropic nature. However, a fully numerical analysis of the theoretical band offset is beyond the scope of this work. Simple parabolic bands have been assumed to illustrate the variation of the first subband minimum with t_{Si} . In the following, the extracted band offsets are denoted as ΔE_x .

The t_{Si} dependence enters the DOS through the position of the subbands: The energy separation between the subbands increases with decreasing t_{Si} , thereby reducing the number of available energy states. As pointed out in [16], the t_{Si} dependence can be exploited to extract the shift in energy band alignment, mobility, and DOS, using the temperature dependence of the subthreshold current.

In short, we observe, for a fixed V_{DS} and V_{GS} , the ratio of the subthreshold current (η_{rat}) in two UTB devices with different t_{Si} , as given by

$$\eta_{\text{rat}} \equiv \frac{I_{\text{ref}}}{I_{\text{thin}}} = \frac{\mu_{\text{ref}} \cdot g(t_{\text{Si,ref}})}{\mu_{\text{thin}} \cdot g(t_{\text{Si,thin}})} \cdot \exp\left(\frac{\Delta E_x}{k_b T}\right) \quad (5)$$

and thus

$$\ln(\eta_{\text{rat}}) = \ln\left[\frac{\mu_{\text{ref}} \cdot g(t_{\text{Si,ref}})}{\mu_{\text{thin}} \cdot g(t_{\text{Si,thin}})}\right] + \left(\frac{\Delta E_x}{k_b T}\right). \quad (6)$$

The subscripts “ref” and “thin” refer to the quantities corresponding to a reference device having a relatively thick body and a device with a thinner body and corresponding supposedly enlarged band gap, respectively; $g(t_{\text{Si}})$ represents the DOS. The difference in the energy band edge of the thinnest layer and the reference device, i.e., ΔE_x in (5), is equal to $E_{x,\text{thin}} - E_{x,\text{ref}}$, with subscript “x” denoting the valence or conduction band edge for p- or n-type devices, respectively. If the body thickness of the reference device is sufficiently thick, i.e., with negligible impact of quantum confinement, then the resulting values of ΔE_x are referenced to the bulk silicon band edge. This choice is just a matter of convenience, as (5) is clearly valid for any combination of t_{Si} ’s, provided that the volume inversion condition holds.

Separating $\Delta\mu$ and ΔDOS With $CV(T)$

As mentioned before, structural quantum confinement alters not only the band gap but also the DOS and mobility, thus making those quantities explicitly t_{Si} dependent [20]. Since the DOS and the mobility jointly enter the prefactor of (5), quantifying their individual contribution to the total change in offset of η_{rat} is not straightforward. However, in order to disentangle changes in mobility and DOS, the IV measurements can be supplemented with subthreshold *capacitance* characteristics, which do not depend on the mobility. Furthermore, noting that in subthreshold $Q_i = k_b T/q \cdot C_G$ (see also Appendix B), the ratio of capacitances θ_{rat} is obtained similarly to (5), i.e.,

$$\theta_{\text{rat}} \equiv \frac{C_{G,\text{ref}}}{C_{G,\text{thin}}} = \frac{g(t_{\text{Si,ref}})}{g(t_{\text{Si,thin}})} \cdot \exp\left(\frac{\Delta E_x}{k_b T}\right) \quad (7)$$

with $C_{G,\text{ref}}$ and $C_{G,\text{thin}}$ being the subthreshold gate capacitance of the reference and the thin-body device, respectively. When plotting $\ln(\theta_{\text{rat}})$ versus the inverse temperature, the offset is exclusively determined by the DOS. In summary, combining the subthreshold current and capacitance measurements allows for a separate investigation of a possible t_{Si} -dependent change in mobility and DOS, in addition to an extraction of shifts in energy band alignment. In addition to the relative change in mobility, its absolute value can be obtained from the combination of the subthreshold capacitance and current on a single device, as given by (cf. Appendix B)

$$\mu = \frac{I_{DS}}{C_G} \cdot \frac{L}{u_{\text{th}}^2} \frac{1}{1 - \exp\left(\frac{-V_{DS}}{u_{\text{th}}}\right)} \quad (8)$$

with u_{th} being the thermal voltage ($k_b T/q$). From a practical point of view, the influence of the parasitics (e.g., the gate-source/drain (S/D) overlap capacitance) can be reduced

Fig. 2. (Symbol) Experimental and (solid line) simulation data on DG SOI devices with $t_{\text{oxb}} \gg t_{\text{oxf}}$. (Dashed line) Simulation data on fully symmetric devices are also shown, along with (dash-dotted line) analytical values calculated with (1). $T = 300$ K, and $L = 25$ μm .

by performing the measurement differentially, i.e., by plotting, for each t_{Si} , the difference in CV characteristics from devices with different gate lengths. By doing so, the capacitance in the low gate-bias regime decreases, which effectively extends the range in which the subthreshold capacitance characteristics can be observed, as will be shown in the next section.

III. RESULT

The procedure outlined in the previous section will be carried out with simulations, and the extracted band offsets will be compared to shifts in V_{TH} . In the following, the body of the reference device is 27 nm thick, i.e., sufficiently thick for quantum confinement to be negligible [5], [21]. Thus, the extracted band edge shift in the thinnest layer is relative to the conduction band minimum or valence band maximum in bulk silicon.

A. Verification of Simulations

The simulations have been performed with Synopsys Sentaurus [22]. Quantum confinement is accounted for by employing the density gradient model, which applies a quantum correction to the classical charge distribution and has proven to be adequate in reproducing the effect of quantum confinement on the device characteristics [23]. Furthermore, the Philips Unified Mobility model with Lombardi transversal field dependence was used [24], [25] with the default parameters. The Si/SiO₂ barrier height is 3.17 eV for electrons and 4.71 eV for holes, and the Si bulk band gap is 1.12 eV at 300 K.

First, the simulations are verified with existing experimental data obtained from [16]. The measured devices are long-channel (100) silicon-on-insulator (SOI) MOSFETs [26] with the backside of the wafer as back-gate contact (denoted as SOIDG); t_{Si} ranges from 27 nm down to 5 nm, the channel length is 25 μm , and the oxide and buried oxide (BOX) thicknesses are 25 and 400 nm, respectively (i.e., t_{oxf} and t_{oxb} , respectively). Fig. 2 shows the measured and simulated subthreshold curves for the SOIDG devices with a t_{Si} of 27 nm. Since the effect of quantum confinement on the mobility and DOS is not included in the current TCAD models, the initial simulations are verified with the measured data from only the

Fig. 3. Simulated and measured subthreshold curves for $T = 300\text{--}450\text{ K}$ and $L = 25\text{ }\mu\text{m}$. The inset shows $\ln(I_{DS})$ versus $1000/T$, the slope of which gives the gate-channel work function difference $\Delta\phi_{ms}$.

thickest device, which exhibits no significant impact of quantum confinement. Good agreement is observed in both weak and strong inversion. The curves have been fitted by adjusting solely the work function ϕ_m of the (n^+ poly) gates. The required adjustment was directly extracted from the temperature dependence of the measured subthreshold current itself, as exemplified in the inset of Fig. 3. The third set of curves shows the simulated data for a fully symmetric device having the same t_{Si} but with $t_{oxf} = t_{oxb} = 2\text{ nm}$ [e.g., see Fig. 1(a)]. When operated in DG mode, the subthreshold curves of the SOIDG and symmetric device indeed coincide, as pointed out in Appendix A of this work. Hence, the existing subthreshold current measurement data are fully comparable with the symmetric case since the $t_{oxf} \ll t_{oxb}$ condition is fulfilled in our SOIDG device. Furthermore, the subthreshold current calculated with (1) is shown as well, demonstrating good agreement.

Fig. 3 shows the simulated subthreshold curves for the SOIDG NMOS for different temperatures, along with the measured data. The temperature ranges from 300 to 450 K, and we verified that the subthreshold slope linearly varies with temperature. This observation confirms that the temperature dependence of the exponential term in (5) is dominant. The slight increase in current at low gate bias and the highest temperature originates from thermal generation of carriers. The inset shows $\ln(I_{DS})$ versus the inverse temperature, from which the previously mentioned difference in gate and channel work function can directly be extracted. Good correspondence between measured and simulated data is observed, demonstrating that the simulations can be used with confidence for further investigations.

B. Extracted Band Offsets From $I_{DS}(T)$ Versus ΔV_{TH}

The simulations presented in the following have been performed on symmetric devices, with a t_{ox} of 2 nm, an L of $1\text{ }\mu\text{m}$, and a t_{Si} in the range of 3–27 nm; $|V_{DS}| = 25\text{ mV}$, and the V_{GS} at which η_{rat} and θ_{rat} are recorded was -0.775 V for PMOS and -0.450 V for NMOS, unless stated otherwise. The work function ϕ_m of the ideal gate was set equal to χ_s , i.e., the electron affinity of bulk Si (4.07 eV).

Fig. 4. Simulated current ratio for several values of t_{Si} , with the 27-nm- t_{Si} device as reference. $L = 1\text{ }\mu\text{m}$. The slope increases for decreasing t_{Si} , corresponding to an upward shift in energy of the conduction band edge.

Fig. 5. Conduction band offset extracted from the slope of the subthreshold current ratio in Fig. 4. (Dashed line) Theoretical band offset calculated with (4) and $m_z^* = 0.916m_0$. (Open symbol) The shift in threshold voltage is significantly larger than the values extracted from $I_{DS}(T)$ and temperature dependent.

Fig. 4 plots $\ln(\eta_{rat})$ versus the inverse temperature for a set of simulated NMOS devices, with t_{Si} ranging from 9 nm down to 3 nm. The slope increases for decreasing t_{Si} , which corresponds to an upward shift in energy of the conduction band edge (i.e., a wider band gap). In addition, the offset in η_{rat} clearly increases for decreasing t_{Si} , which generally represents a change in the combination of mobility and DOS [hence, the prefactor in (5)]. However, in this case, the observed change in offset is solely due to a reduction in the DOS since, in these simulations, only bulk mobility models are employed, which exhibit no direct t_{Si} dependence. Furthermore, we stress that, in the subthreshold regime, the electric field normal to the gates is low. Hence, closer inspection confirms that the mobility is essentially constant throughout the entire channel, irrespective of t_{Si} .

The band offsets extracted from the slope of η_{rat} are shown in Figs. 5 and 6 for NMOS and PMOS devices, respectively, along with the extracted shift in “experimental” threshold voltage (ΔV_{TH}) for different temperatures and the SOIDG PMOS $I_{DS}(T)$ data from [16]. Again, all values are referenced to the thickest device (with a t_{Si} of 27 nm), which, by definition, exhibits no band edge shift (bulk band gap). For reference, the

Fig. 6. Valence band offset extracted from the measured [16] and simulated subthreshold current ratios on PMOS DG devices. (Dashed line) Analytically calculated minimum of the lowest subband calculated with (4) and $m_z^* = 0.291m_0$ (HH). The shift in threshold voltage is also depicted.

first subband minimum is also shown, which was calculated with the (100) quantization effective masses [27], [28].

Although ΔV_{TH} shows the same trend, i.e., increasing V_{TH} for decreasing t_{Si} , the figures clearly show that the extracted values are significantly higher than their respective $I_{DS}(T)$ counterparts. This can be explained by noting that quantum confinement alters both the band gap and the DOS: Splitting of the bulk conduction and valence band into subbands gives the following: 1) a wider band gap through the offset of (mainly) the first subband and 2) reduction in the available states due to the emerging energy gaps, which separate the subbands. In the $I_{DS}(T)$ method, shifts in the band edges are extracted from the *slope* of the current ratio, whereas changes in the DOS and mobility can be derived from the *offset* in the current ratio; hence, $I_{DS}(T)$ measurements allow for an investigation of band edge shifts separate from the mobility and DOS, as suggested by (5). In contrast, ΔV_{TH} consists of a combined change in band gap, mobility, and DOS, thus amplifying the apparent impact of quantum confinement. Furthermore, it is interesting to note that the threshold voltage exhibits strong temperature dependence. While the latter is exploited in the $I_{DS}(T)$ measurements, it shows up as an additional source of error when determining the band edge shifts based on ΔV_{TH} .

The values obtained with the $I_{DS}(T)$ method closely reproduce the analytically calculated lowest energy in each band, particularly for the NMOS. The slight discrepancy in the valence band offset is attributed to the approximations employed in both the density gradient model, which involves a single fit parameter to account for the different hole effective masses [23], and the single heavy hole effective mass used in the analytical calculation; in fact, those masses depend on the anisotropy and dimensionality of the confined system [28].

C. Impact of $\Delta\mu$ on the Extracted Offset and on ΔV_{TH}

The results in the previous section have shown that the shifts in V_{TH} are fairly large with respect to the expected shift in band edge, whereas the extracted band offsets from $I_{DS}(T)$ are in close agreement with the theoretical values. In this regard, it is

Fig. 7. Simulated subthreshold current ratio for (open symbol) fixed and (filled symbol) modified mobility; $L = 1 \mu\text{m}$. The mobility was manually reduced by 30% ($t_{Si} = 6 \text{ nm}$) to 65% ($t_{Si} = 3 \text{ nm}$) relative to the mobility in the reference device [cf. (6)].

Fig. 8. Conduction band offset extracted from the subthreshold current ratio in Fig. 7 for (open symbol) fixed and modified mobility. (Squared symbol) The shift in threshold voltage was found to increase with decreasing mobility, whereas the band offset extracted from $I_{DS}(T)$ remains unchanged.

illustrative to investigate the impact of a change in mobility on η_{rat} , on the resulting values of ΔE_x , and on the corresponding ΔV_{TH} . As of yet, a direct t_{Si} dependence due to, e.g., thickness fluctuation is not incorporated in the current TCAD mobility models, so the impact of a change in mobility is emulated by artificially setting the low-field mobility to a fixed value for each t_{Si} . Although the mobility is reported to decrease with decreasing t_{Si} , with a local maximum around $t_{Si} \approx 3\text{--}4 \text{ nm}$ [7], the exact choice of the mobility values in this work does not affect the generality of the conclusion. The mobility was manually reduced by 15% ($t_{Si} = 9 \text{ nm}$) to 65% ($t_{Si} = 3 \text{ nm}$) relative to the mobility in the reference device. The resulting η_{rat} is shown in Fig. 7, demonstrating that the offset in η_{rat} is modified in direct proportion to the mobility reduction, whereas the slope remains unchanged. The effect of a change in mobility on the extracted ΔE_C and ΔV_{TH} can be observed in Fig. 8, which shows the conduction band offset and the threshold voltage shift with and without modified mobility. The figure clearly illustrates that the values obtained with the $I_{DS}(T)$ method remain unchanged, whereas the extracted ΔV_{TH} is sensitive to a t_{Si} -dependent change in mobility.

Fig. 9. Simulated capacitance versus voltage characteristic of a 5-nm gated p-i-n diode, for $L = 1 \mu\text{m}$ and $L = 2 \mu\text{m}$, showing the “single” capacitance and the normalized differential capacitance [$C_{\text{diff}} = (C_2 - C_1)/W(L_2 - L_1)$]. Only the n-type inversion is shown. (Dashed line) Subthreshold gate capacitance calculated with (2).

Similarly, the impact of variation of typical (strong) inversion-related device parameters has been considered, such as the S/D series resistance and the oxide thickness. In fact, we have verified that changing the series resistance and oxide thickness indeed does not affect the subthreshold current, as predicted by (1) and the corresponding assumption of a long channel with low V_{DS} . In contrast, V_{TH} and ΔV_{TH} differ from the previously obtained values; for example, adding a 2-k Ω resistor to the S/D contacts of a device with a t_{Si} of 5 nm to emulate the S/D series resistance produces 10% smaller ΔV_{TH} , compared with that of the device without the artificial series resistance.

D. Separation of $\Delta\mu$ and ΔDOS

Since both the mobility and the DOS determine the prefactor in (5), it is not possible to trace a t_{Si} -dependent change in the offset of η_{rat} back to either the mobility or the DOS from the *IV* measurements alone. Hence, the effect of a change in DOS on I_{DS} would produce results that are very similar to the simulations with a modified mobility, which were previously shown. If, in addition to the *IV* measurements, Q_i is determined from *CV* characteristics, the individual contribution of the mobility and the DOS can be extracted. To illustrate this procedure, the DOS is manually modified through N_C and N_V , which represent the effective DOS in the conduction and valence bands, respectively.

The *CV* simulations have been performed on gated p-i-n diodes having a geometry that is identical to the structure shown in Fig. 1(a), only with p^+ source doping. The main merit of a p-i-n device is that the n- and p-type inversions can independently be investigated, thereby providing the possibility to extract both the conduction and valence band offsets on a single device. Fig. 9 shows a typical n-type inversion capacitance characteristic for two devices with $t_{Si} = 5 \text{ nm}$ and channel lengths of $1 \mu\text{m}$ and $2 \mu\text{m}$. The plot shows the “single” capacitance curves, along with the “differential” capacitance calculated with $C_{\text{diff}} = (C_2 - C_1)/W(L_2 - L_1)$. Performing the measurement differentially clearly facilitates a more accu-

Fig. 10. Effect of decreasing mobility and DOS on the (a) subthreshold current and (b) capacitance ratio. Curve (1) in (a) shows the original current ratio for a t_{Si} of 5 nm, with the 27-nm- t_{Si} device as reference. Manually reducing the mobility in the 5-nm- t_{Si} device by 40% increases the offset in η_{rat} in direct proportion [curve (2)]. Setting, in addition, the DOS to 70% of its original value results in an additional increase in the offset [curve (3)]. (b) The subthreshold capacitance ratio is only sensitive to the DOS reduction, showing a proportionally increasing offset [curve (2)] relative to the curve with unchanged DOS [curve (1)].

rate determination of the subthreshold characteristics, because the capacitance in the low bias regime is significantly reduced. Furthermore, the values calculated with (2) are depicted as well, demonstrating good agreement.

Fig. 10(a) shows η_{rat} for an NMOS device with a t_{Si} of 5 nm for three cases: 1) original mobility and original DOS; 2) reduced mobility and original DOS; and 3) reduced mobility and reduced DOS. As concluded before, reducing the mobility in the thinnest device increases the offset of η_{rat} in direct proportion. Likewise, a reduction in the DOS, in this case to $0.7 \times$ its original value (for both N_C and N_V), gives an additional offset as expected based on (5). In fact, the ratio of the DOS and mobility in the reference device and the thin device [hence, the prefactor in (5)] can be found by extrapolating $\ln(\eta_{\text{rat}})$ to $1000/T \rightarrow 0$, i.e., when the last term in (6) reduces to zero. Indeed, the additional increase in the offset of $\ln(\eta_{\text{rat}})$ is in agreement with the expected value of $\ln(1/0.7)$. The slight increase in the slope is explained by recalling that the quantum correction potential depends on the carrier distribution; hence, when modifying the DOS, its value relative to the original value (N_{ref}) will appear as an additional contribution, equal to $k_b T \ln(N_C/N_{\text{ref}})$, to the applied quantum

correction potential. This directly translates into a slightly steeper slope of η_{rat} , which corresponds to an additional band edge shift of $k_b T \ln(N_C/N_{\text{ref}}) = k_b T \ln(0.7) \approx 9 \text{ meV}$.

The procedure is repeated for the ratio of the subthreshold capacitance θ_{rat} [cf. (7)], the result of which is shown in Fig. 10(b). The curves with and without modified mobility exactly coincide, thus confirming that the capacitance is insensitive to a mobility variation. Hence, the observed increase in the offset of the upper branch [curve (2)] with reduced DOS is solely due to the reduction in the DOS.

In summary, the shift in conduction and valence band edge can be extracted from the slope of η_{rat} . The offset of η_{rat} is determined by both the mobility and the DOS. In order to disentangle these two quantities, additional subthreshold capacitance measurements can be carried out to extract the change in DOS. A possible t_{Si} -dependent change in mobility can then be derived from the remaining difference in the offset between the ratio of the currents and capacitances.

E. Discussion

The method for extracting ΔE_x , mobility, and DOS involves a few assumptions. This section covers some sanity checks that are instrumental in determining the applicability of the $I_{DS}(T)$ method. Most importantly, (5) assumes that the exponential temperature dependence is much stronger than the temperature dependence of the prefactor. This assumption, however, generally holds under typical operating conditions: Although the mobility and DOS do change with temperature, only a *difference* in temperature dependence from layer to layer will introduce errors in the extracted band offsets. The aforementioned assumption can easily be verified by assuring that the subthreshold slope varies linearly with temperature and yields essentially equal values for the t_{Si} range under consideration. The latter is a clear manifestation of volume inversion, which is a typical feature of UTB devices.

The ideality of the subthreshold slope is greatly determined by the concentration of interface states. Hence, one might argue that high- κ gate dielectrics, which generally exhibit a higher interface state density compared with SiO_2 [29], may hamper the reliable application of the $I_{DS}(T)$ method. Although the subthreshold slope may deviate from the ideal values (i.e., 60 mV/dec at 300 K) due to the presence of interface states, sufficient requirements are given as follows: 1) the subthreshold slope is approximately equal for the considered t_{Si} range and 2) it exhibits a linear temperature dependence. Furthermore, a linearly temperature-dependent subthreshold slope implies that, for η_{rat} , the actual value of the gate bias, provided that $V_G < V_{\text{TH}}$, is not important: The difference in V_G at which I_{ref} and I_{thin} are recorded is simply subtracted when converting the slope of η_{rat} to ΔE_x .

The results shown in this work are obtained from long-channel (1 μm) devices, with low V_{DS} (25 mV), to ensure that the actual barrier height is determined solely by the gate (bias and work function) and the intrinsic body. For short-channel devices, the barrier is lowered due to the proximity of the source and drain; hence, we verified that the extracted work function difference between gate and channel increases,

i.e., the source/channel barrier decreases, for smaller L and increasing V_{DS} .

IV. CONCLUSION

In this paper, shifts in the valence and conduction band edge have been extracted from the temperature dependence of the subthreshold current. The results have been compared with shifts in the threshold voltage, showing that, with the $I_{DS}(T)$ method, shifts in the band edges can separately be observed from changes in mobility and DOS, which cannot be accomplished with the ΔV_{TH} method. The observed shifts in V_{TH} are generally much ($> 3\times$) larger than the expected band edge shifts, whereas the band offsets extracted from the $I_{DS}(T)$ measurements are in very close agreement with the theoretical values. Hence, ΔV_{TH} generally overestimates the quantum-confinement-induced shift in band alignment.

A change in mobility and DOS can further be quantified with additional temperature-dependent subthreshold CV measurements. Since the capacitance does not depend on the mobility, any change in DOS is directly reflected in the subthreshold capacitance, irrespective of a possible change in mobility.

APPENDIX A

UTB SOI UNDER SUBTHRESHOLD CONDITIONS

The aim of this appendix is to illustrate that an UTB device with very asymmetric front- and back-gate oxide thicknesses (t_{oxf} and t_{oxb} , respectively) can be considered as a fully symmetric device under subthreshold conditions. In the following, the subscript “f” and “b” refer to the front and back interface, respectively. Furthermore, we assume that the front and back gates are equally biased.

From Fig. 1(b), we derive

$$\frac{\varepsilon_{\text{ox}}}{t_{\text{oxf}}}(V_G - \Delta\phi_f - \psi_{\text{sf}}) = \varepsilon_{\text{Si}}F_f \quad (9a)$$

$$\frac{\varepsilon_{\text{ox}}}{t_{\text{oxb}}}(V_G - \Delta\phi_b - \psi_{\text{sb}}) = \varepsilon_{\text{Si}}F_b \quad (9b)$$

where F_f and ψ_{sf} are the electric field and the potential at the gate-channel interfaces, respectively; ε_{ox} and ε_{Si} are the dielectric constants of the gate dielectric and silicon, respectively; and $\Delta\phi_f$ is the difference in work function between the gate and the channel. Furthermore, in the subthreshold, we have $\psi_{\text{sb}} - \psi_{\text{sf}} = -F_0 t_{\text{Si}}$, with $F_b = F_f = F_0$. Combining (9a) and (9b) gives [12]

$$F_0 = \frac{\Delta\phi_b - \Delta\phi_f}{\frac{\varepsilon_{\text{Si}}}{\varepsilon_{\text{ox}}}(t_{\text{oxf}} + t_{\text{oxb}}) + t_{\text{Si}}}. \quad (10)$$

After substitution in (9), the potential at either surface of the body is obtained as

$$\psi_{\text{sf}} = V_G - \left[\frac{\Delta\phi_f(\varepsilon_{\text{ox}}t_{\text{Si}} + \varepsilon_{\text{Si}}t_{\text{oxb}}) + \Delta\phi_b\varepsilon_{\text{Si}}t_{\text{oxf}}}{\varepsilon_{\text{ox}}t_{\text{Si}} + \varepsilon_{\text{Si}}(t_{\text{oxf}} + t_{\text{oxb}})} \right] \quad (11a)$$

$$\psi_{\text{sb}} = V_G - \left[\frac{\Delta\phi_b(\varepsilon_{\text{ox}}t_{\text{Si}} + \varepsilon_{\text{Si}}t_{\text{oxf}}) + \Delta\phi_f\varepsilon_{\text{Si}}t_{\text{oxb}}}{\varepsilon_{\text{ox}}t_{\text{Si}} + \varepsilon_{\text{Si}}(t_{\text{oxf}} + t_{\text{oxb}})} \right]. \quad (11b)$$

Assuming $t_{\text{oxf}} = t_{\text{oxb}}$ and $\Delta\phi_b = \Delta\phi_f$ (hence, a fully symmetric device), (11a) and (11b) reduce to $\psi_{\text{sf}} = \psi_{\text{sb}} = V_G - \Delta\phi_f$, independent of t_{ox} . Interestingly, the same result is obtained when $t_{\text{oxb}} \gg t_{\text{oxf}}$, which, e.g., corresponds to an UTB SOI device on a thick BOX layer with the underlying substrate as backplane.

APPENDIX B MOBILITY EXTRACTION IN SUBTHRESHOLD

The following shows how the low-field mobility can be extracted from the subthreshold current and capacitance. With $C_G = dQ_i/dV_G$ and (2), we obtain $Q_i = u_{\text{th}}C_G$. After substitution in (1), the current and capacitance are directly linked through the mobility, as given by

$$I_{DS} = \frac{\mu u_{\text{th}}}{L} \cdot u_{\text{th}} C_G \left[1 - \exp\left(\frac{-V_{DS}}{u_{\text{th}}}\right) \right]. \quad (12)$$

Hence, the low-field mobility can be extracted as follows:

$$\mu = \frac{I_{DS}}{C_G} \cdot \frac{L}{u_{\text{th}}^2} \frac{1}{1 - \exp\left(\frac{-V_{DS}}{u_{\text{th}}}\right)}. \quad (13)$$

Equation (13) can be shown to also hold for any SOI DG device, provided that the front and back gates are equally biased. Generally, the Q_i in a UTB DG device in the subthreshold is given by [30]

$$Q_i = -qt_{\text{Si}}n_i u_{\text{th}} \left[\frac{\exp\left(\frac{\psi_{\text{sb}}}{u_{\text{th}}}\right) - \exp\left(\frac{\psi_{\text{sf}}}{u_{\text{th}}}\right)}{\psi_{\text{sb}} - \psi_{\text{sf}}} \right] \quad (14)$$

with ψ_{sf} and ψ_{sb} as given in (11a) and (11b). Furthermore, noting that both gates are equally biased and assuming that volume inversion occurs, we use

$$\frac{\partial \psi_{\text{sf}}}{\partial V_G} = \frac{\partial \psi_{\text{sb}}}{\partial V_G} = 1 \quad (15)$$

and hence

$$\frac{\partial}{\partial V_G} \left\{ \exp\left(\frac{\psi_{\text{sf}}}{u_{\text{th}}}\right) \right\} = \frac{1}{u_{\text{th}}} \exp\left(\frac{\psi_{\text{sf}}}{u_{\text{th}}}\right). \quad (16)$$

Then, with (14), the subthreshold gate capacitance is obtained by

$$\begin{aligned} C_G &= \frac{\partial Q_i}{\partial V_G} = -qt_{\text{Si}}n_i u_{\text{th}} \frac{\partial}{\partial V_G} \left\{ \frac{\exp\left(\frac{\psi_{\text{sb}}}{u_{\text{th}}}\right) - \exp\left(\frac{\psi_{\text{sf}}}{u_{\text{th}}}\right)}{\psi_{\text{sb}} - \psi_{\text{sf}}} \right\} \\ &= -qt_{\text{Si}}n_i \left\{ \frac{\exp\left(\frac{\psi_{\text{sb}}}{u_{\text{th}}}\right) - \exp\left(\frac{\psi_{\text{sf}}}{u_{\text{th}}}\right)}{\psi_{\text{sb}} - \psi_{\text{sf}}} \right\} \\ &= \frac{Q_i}{u_{\text{th}}}. \end{aligned} \quad (17)$$

Hence, the low-field mobility can directly be determined from the measured subthreshold gate capacitance and drain current;

this holds for fully symmetric DG devices and asymmetric DG SOI devices, irrespective of the oxide thickness and work function of the gates, provided that the gates are equally biased.

Furthermore, note that, for a symmetric DG MOSFET, for which $\psi_{\text{sf}} = \psi_{\text{sb}} = \psi_s$, (14) yields, after applying Taylor's expansion

$$Q_i = -qt_{\text{Si}}n_i \exp\left(\frac{\psi_s}{u_{\text{th}}}\right)$$

which is equivalent to (2).

In conclusion, with (13), it is possible to extract the low-field mobility, without any further approximations, in contrast to the commonly used expression $\mu_{\text{eff}} = L/(Q_i V_{DS}/I_{DS})$; the latter is derived from only the drift component of the drain current and thus neglects the diffusive part, which is dominant in the subthreshold (hence, low-field) regime.

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