An Electrically Programmable Split-Electrode Charge-Coupled Transversal Filter (EPSEF)

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Abstract—A CCD split-electrode transversal filter (EPSEF) with analog controlled tap weights is described. The programmable tap weighting utilizes a novel analog multiplier for sampled data, based on charge profiling underneath a resistive gate structure. The EPSEF device concept and the performance data of a prototype filter with eight programmable taps are presented. Applications of the EPSEF in several programmed filter functions and in an adaptive filter system are demonstrated.

I. Introduction

CHARGE-coupled devices are very well suited to perform transversal filter functions on analog signals. Several filter implementations have been reported in the open literature and recently the subject has been comprehensively reviewed [1], [2]. The most compact and widely applied CCD filter structure is the split-electrode transversal filter with fixed impulse response [3]-[5]. Such CCD filters are expected to compete successfully with digital filter implementations, if real-time operation is required. The accuracy of the CCD filters, however, cannot come up to the level of the digital filters.

In adaptive filter and correlator applications, programmable filters are required. Here real-time operation is a prerequisite, rather than a high coefficient accuracy. CCD filters are very well suited to be made programmable and the search for reliable and compact, electrically programmable structures is obvious. Several programmable CCD-filter concepts have already been proposed and implemented [6]-[14]. Two different programmable filter architectures have evolved: the serial-in, parallel-out (SIPO) configuration [Fig. 1(a)] with tap weighting at the output [7]-[10] and the parallel-in, serial-out (PISO) configuration [Fig. 1(b)] with tap weighting at the input [11]-[13].

The programmable tap weighting may be either binary (0, 1 or -1, 1), or fully analog. Digitally programmable filters may be composed of several binary weighted filters in parallel or they apply on-chip multiplying digital-to-analog converter (MDAC) modules for the tap weighting. The digitally programmable analog filter is suited for applications in systems that are controlled by microprocessors or computers. Analog-controlled tap weights are particularly suited to perform real-time analog correlation and fast parallel updating of the tap-weight coefficients in adaptive filter applications by analog tap-weight control.

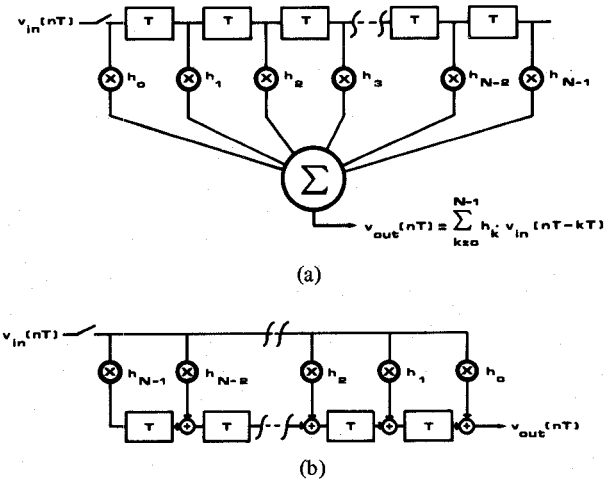

Fig. 1. Block diagrams of a transversal filter: (a) serial-in, parallel-out configuration; (b) parallel-in, serial-out configuration.

The majority of the analog programmable filters have been designed in the SIPO configuration and use floating gate sensing [7]-[10] at the distinct taps, followed by analog tap-weight multiplication. The tap weighting is performed by analog multipliers [8], [9], analog-controlled conductances [7], or by analog-controlled variable capacitances [10]. Except in the last approach, the floating gate sensing requires a voltage-to-current conversion at each tap and signal summation is performed in the current domain. In [10], a constant-voltage sensing technique is applied for capacitive sensing of the capacitively weighted signals at the floating sense gates.

This paper deals with the design and performance of an analog programmable filter based on a novel concept: the electrically programmable split-electrode CCD transversal filter (EPSEF) [14]. The design applies the serial-in, parallel-out structure and combines the advantages of the compact constant-voltage sensing method of the split-electrode filter with analog programmable tap-weight factors. The key to this design is the in-channel voltage-controlled charge profiling and partitioning, preceding the sense operation.

In Section II the EPSEF device concept is described in more detail. Section III deals with the voltage-controlled charge profiling by a resistive polycrystalline silicon gate structure. The partitioning and sensing of the weighted signal-charge packets is described in Section IV. In Section V the design

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parameters of an eight tap prototype implementation and its performance data are presented. In Section VI some possible applications of the EPSEF are demonstrated. The EPSEF has been applied as the programmable filter unit in an adaptive filter system.

II. Basic Operation of the EPSEF

A sampled data transversal filter generates an output signal according to the expression

$$v_{\text{out}}(nT) = \sum_{k=0}^{N-1} h_k v_{\text{in}}(nT - kT). \tag{1}$$

Here, T is the sampling time interval, which is equal to the unit time delay, N is the number of taps, and h_k is the weight factor of the kth tap. From (1) it is clear that a transversal filter has to perform three functions: signal delay, multiplication of the delayed signals by weight factors, and summation.

In CCD transversal filters, the delay is obtained by shifting signal-charge packets along the $Si\text{-}SiO_2$ interface under control of clock pulses on the gate electrodes. At the CCD input circuit, the input voltage is sampled and a voltage-to-charge conversion is performed to define the charge packets. At the sense taps of SIPO structured devices an inverse conversion of charge-to-voltage is performed. These conversions are implicit in the expression (1) that is generally applied to CCD transversal filters. Taking into account an input voltage-to-charge conversion function $\mathcal{F}$, an explicit operator notation $\mathcal{D}$ for the delay of the charge sample by a period T, and an output charge-to-voltage conversion function $\mathcal{G}$, (1) becomes

$$v_{\text{out}}(nT) = \sum_{k=0}^{N-1} h_k \cdot [\mathcal{G}(\mathcal{D}^k(\mathcal{F}(v_{\text{in}}(nT - kT))))]. \tag{2}$$

The meaning of the delay operation $\mathcal{D}^k$ in (2) is simply that the signal that has been sampled for instance at the time moment $(nT - kT)$ is stored during a period kT, and, consequently, this signal will be available at time nT. The multiplication by h_k as well as the summation may precede the charge-to-voltage conversion $\mathcal{G}$ if the latter is a linear function:

$$v_{\text{out}}(nT) = \mathcal{G}\left(\sum_{k=0}^{N-1} h_k \cdot [\mathcal{D}^k(\mathcal{F}(v_{\text{in}}(nT - kT)))]\right). \tag{3}$$

Implementation of the CCD transversal filter according to (3) is attractive because it needs only one charge-to-voltage conversion instead of the N conversions that are required in (2). The well-known split-electrode transversal filter concept is an example of the implementation of (3) and it applies the very linear constant-voltage sensing. The multiplication of the delayed charge packet at the kth tap by the tap-weight factor h_k is obtained by sensing a fraction h_k of the signal-charge packet Q_k.

In order to provide for tap-weight factors of dual polarity, a positive and a negative summing bus has been arranged (Fig. 2). The fractional sensing of the charge packets is achieved by means of a split in the sense electrode, which divides the sense gate area A into a part $A_{r,k}$, attached to the positive summing bus, and a part $A_{l,k}$, attached to the negative summing bus. By means of a differential amplifier at the filter output, the resulting tap-weight factor h_k is now equal to

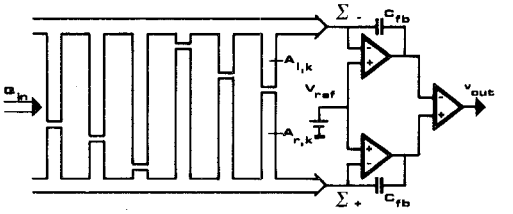


Fig. 2. Schematic of the split-electrode transversal filter with fixed weighting coefficients.

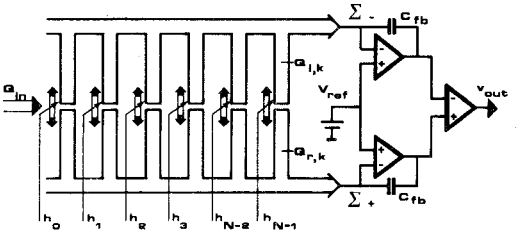


Fig. 3. Schematic of the EPSEF. Charge profiling and charge partitioning is performed before the charge sensing.

$$h_k = (A_{r,k} - A_{l,k})/A. \tag{4}$$

The sense-gate voltage remains virtually constant as the charge induced in the sense electrodes is compensated via the feedback capacitor C_{fb}. This permits the connection of the sense gates of one polarity to the same sense amplifier, thus combining the summation and the charge-to-voltage conversion at the feedback capacitor of the sense amplifier. The high performance and the compact structure of the split-electrode filters challenged the designers to apply this concept to the implementation of several filter functions [1]-[5].

For analog *electrically programmable* CCD filters too, the *split-electrode* concept offers the advantages of a compact and accurate sense and sum circuit. Just as in the fixed split-electrode filters, the tap-weight multiplication in a programmable filter has to be performed by charge partitioning between the positive and negative sense-gate segments. In the electrically programmable split-electrode CCD transversal filter, voltage controlled profiling in the direction perpendicular to the charge packet transport is applied. The profiled charge packet is then partitioned into a left and a right signal packet, prior to the transfer towards the split sense-electrodes. The concept of the EPSEF is shown schematically in Fig. 3.

The charge profiling is obtained under a resistive gate. By means of the tap-weight control voltages, a gate-voltage gradient in the transverse direction is introduced, which profiles the underlying inversion-charge packet. The CCD channel of the subsequent section is separated into two parallel sections by means of a stopper-diffusion split in the middle of the channel. At the transfer from the profiling resistive gate into the next storage stage, the charge packet is partitioned into a left- and a right-hand charge packet, according to the profile, set up under the resistive gate. The left and right charge packets are sensed under the equally sized positive and negative split-electrode sense-gate segments. In the next storage element the left and right charge packets are merged

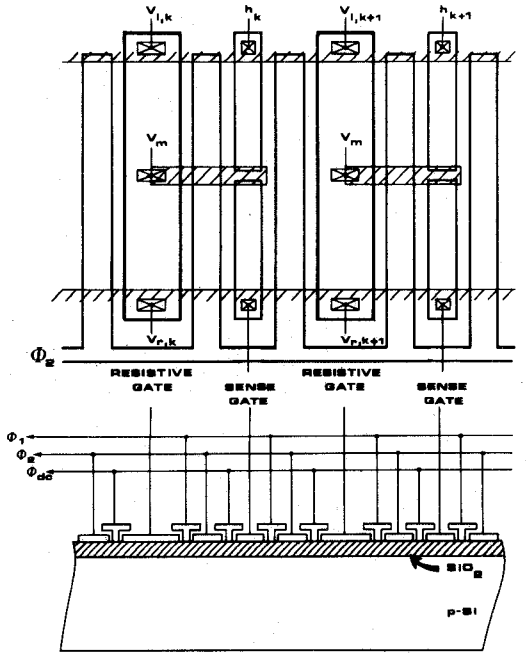


Fig. 4. (a) Schematical layout of two filter sections of the EPSEF. The shaded areas indicate channel stopper diffusions. Only the storage gates implemented in the first polysilicon level are drawn. The gaps between those gates are covered with transfer gates in the second polysilicon level. (b) Cross section along the CCD channel.

and the charge packet is ready for the profiling under the next resistive gate. The arrangement of the profiling resistive gates, the charge partitioning channel-splits, and the sense gates are visualized schematically in Fig. 4.

In conclusion, the key to electrical programmability of the split-electrode filter is to perform the charge profiling and partitioning apart from the charge sensing. The charge profiling by means of a resistive-gate structure is described in the next section.

III. Charge Profiling

In the EPSEF, the profiling of the charge packet is performed in a storage well with a gate composed of resistive polycrystalline silicon on top of it. A constant dc voltage V_m is applied at the center contacts of the resistive gates. The profiling in the kth filter segment is controlled by the voltages $V_{l,k}$ and $V_{r,k}$ at the left and right end contacts. The position-dependent gate voltage $V(y)$ causes a wedge shaped surface potential well (Fig. 5). Assuming a homogeneous resistivity of the polysilicon layer, the charge portions $Q_{l,k}$ and $Q_{r,k}$ under the left and right parts of the resistive gate are found by straightforward analysis (see Appendix) as

$$Q_{l,k} = \left(\frac{V_m - V_{r,k}}{2V_m - V_{l,k} - V_{r,k}}\right) Q_k \tag{5}$$

and

$$Q_{r,k} = \left(\frac{V_m - V_{l,k}}{2V_m - V_{l,k} - V_{r,k}}\right) Q_k \tag{6}$$

where $Q_k = Q_{l,k} + Q_{r,k}$ is the total charge packet at the kth filter section. The tap control voltages are $V_{l,k} = V_b - V_{tw,k}$ and $V_{r,k} = V_b + V_{tw,k}$, where V_b is the common tap bias voltage and $V_{tw,k}$ is the differential tap control voltage applied to the kth resistive gate. Note that V_b differs from the voltage V_m at the center contact, so that the wedge shape of the potential across the resistive gate is maintained for a considerable range of the differential tap control voltage $V_{tw,k}$. With use of these notations, (5) and (6) become

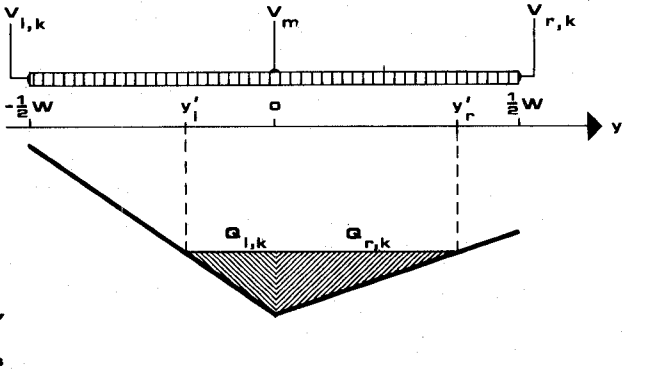


Fig. 5. Cross section of a profiling resistive polysilicon gate. The tap control voltages are $V_{l,k} = V_b - V_{tw,k}$ and $V_{r,k} = V_b + V_{tw,k}$. In the lower part, a schematic diagram of the wedge-shaped surface potential is shown. The shaded areas indicate the left- and right-hand charge packets.

$$Q_{l,k} = \frac{1}{2}\left(1 - \frac{V_{tw,k}}{V_m - V_b}\right) Q_k \tag{7}$$

and

$$Q_{r,k} = \frac{1}{2}\left(1 + \frac{V_{tw,k}}{V_m - V_b}\right) Q_k. \tag{8}$$

The tap-weight factor that results from differential sensing of $Q_{r,k}$ and $Q_{l,k}$ is defined as

$$h_k = (Q_{r,k} - Q_{l,k})/Q_k. \tag{9}$$

The substitution of (7) and (8) in (9) results in

$$h_k = \frac{V_{tw,k}}{V_m - V_b}. \tag{10}$$

Besides the homogeneous resistivity of the polysilicon, mentioned before, the following assumptions have been made in the derivation of (10).

1) The dynamic range of the charge profiling according to (7) and (8) is limited by the condition that the charge packet should not reach the channel edges under the resistive gates because otherwise (5) and (6) will no longer be valid. In n-channel devices, therefore, the common voltage at the center contacts V_m should be considerably higher than V_b, and $V_{tw,k}$ should be less than $(V_m - V_b)$ in order to preserve the wedge shape of the potential well. This implies a tradeoff between the charge handling capacity and the maximum tap-weight setting.

2) The contacts via which the control voltages V_m, $V_{l,k}$, and $V_{r,k}$ are applied are assumed to be line contacts in parallel with the direction of the CCD channel. Contact resistance has not been taken into account.

3) Edge effects due to fringing fields at the edges of the resistive gate have been disregarded.

4) The charge partitioning should be performed according

to the distribution below the left and right halves of the resistive gate.

In practice, the simple expression (10) for the tap-weight h_k is subject to a number of errors, which should be understood for a full assessment of the EPSEF. The errors arising in the process of charge profiling will be discussed in the remainder of this section. We distinguish between errors that exist in the steady state (static distortion) and errors that occur because the time period for the charge profiling is too short to attain to the steady state (dynamic distortion).

The dynamic distortion will limit the maximum operating frequency. This will be governed by either the *RC*-time constant of the resistive gate or by the settling time of the charge redistribution in the inversion channel underneath. In the present EPSEF device, the *RC*-time constant of the resistive gate is of the order of 10 ns. The settling time for approaching a steady-state charge redistribution of the inversion charge in the wedge-shaped potential well to within 0.1 percent accuracy, is 3 μs. This limits the maximum clock frequency of this device to 250 kHz.

In the remainder of this section only static distortion effects are discussed.

1) A constant contact resistance R_c at the interconnection points with the resistive gate affects (10) for the tap-weight factor by a constant factor of the order of $(1 + 4R_c/R_p)$ in the right-hand expression. Here R_p is the resistance of one-half of the resistive gate. Differences in contact resistance between left- and right-hand contacts disturb the linearity between the actual tap-weight and the applied tap-weight voltage $V_{tw,k}$. To reduce the contact resistance, the contact areas in the resistive polysilicon have been heavily doped. The result is a conductive area around the contact window.

2) The finite dimensions of the conductive center contact cause an equipotential area A_c that distorts the wedge shape of the potential well. If the inversion charge under A_c is denoted as $Q_{m,k}$, (5)-(8) apply to the remaining charge portion $(Q_k - Q_{m,k})$ instead of to Q_k and the resulting error in the tap-weight factor is found as

$$\Delta h_k = -h_k Q_{m,k}/Q_k. \tag{11}$$

The expression for $Q_{m,k}$ is found by straightforward analysis as

$$Q_{m,k} = \gamma(-1 + \sqrt{1 + 2Q_k/\gamma}) \tag{12}$$

with

$$\gamma = \frac{A_c^2 C_{ox}}{A_r}(V_m - V_b)(1 - h_k^2). \tag{13}$$

Here A_r denotes the area of the resistive gate between the center contact and the outer contact. C_{ox} is the gate oxide capacitance per unit area.

As the ratio $Q_{m,k}/Q_k$ depends on Q_k, it causes nonlinear distortion. From (11)-(13) it is seen that the distortion decreases with increasing Q_k and h_k. A small differential voltage $(V_m - V_b)$ decreases the distortion at the expense of dynamic range. A design criterion follows from (13) for the active area A_c under the equipotential contact region. A_c can

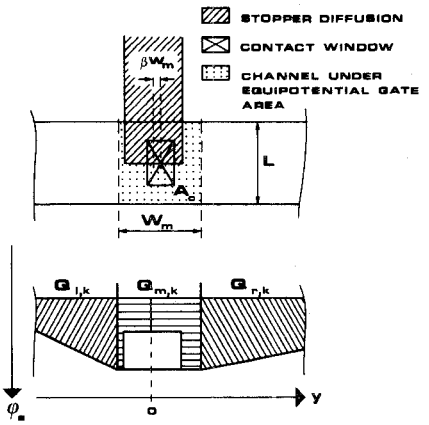


Fig. 6. Upper part: top view of the center contact area of the resistive gate with channel-split diffusion and conductive contact area. A misalignment βW_m of the contact with respect to the channel split is indicated. Lower part: Schematic presentation of the charge portions $Q_{l,k}$, $Q_{m,k}$, and $Q_{r,k}$ corresponding to the upper scheme. The white rectangle under $Q_{m,k}$ indicates the decrease of the amount of charge under the conductive contact area due to the extension of the channel-split diffusion.

be made smaller than the conducting contact area by extension of the channel-stopper diffusion split under the resistive gate contact (see Fig. 6). At moderate signal levels, the second harmonic distortion caused by this center contact effect has been calculated for our design to be about -45 dB.

3) Nonuniform sheet resistivity of the resistive polysilicon may degrade the linearity of the tap-weight setting. The effect of random nonuniformities over small distances is expected to be negligible due to averaging over the total gate area. The most severe deviation may be caused by a resistivity gradient in the transverse direction. If this resistivity gradient is constant, the deviation $\Delta h_k'$ of the tap-weight factor can be estimated [15] as

$$\Delta h_k' \leqslant \frac{W}{R}\frac{dR}{dy} \tag{14}$$

where R is the sheet resistivity of the resistive polysilicon and W is the CCD channel width.

4) Other systematic variations in material parameters (e.g., oxide thickness and substrate doping) may cause deviations in the charge redistribution and in the charge sensing in a similar way as in split-electrode filters with fixed coefficients [22]. These effects are not expected to limit the device performance severely.

IV. Charge Partitioning and Sensing

The resistive polysilicon redistribution gate was used for profiling the charge density of the inversion charge in the transverse direction. The inversion charges $Q_{l,k}$ under the left half and $Q_{r,k}$ under the right half have to be sensed separately in order to implement the tap-weight factor h_k of (9). The resistive profiling gate is not well suited for sensing. Therefore, the charge packets $Q_{l,k}$ and $Q_{r,k}$ are partitioned by transferring the profiled charge packet into two parallel sections of the CCD that are separated by a narrow stopper-diffusion split in the middle of the channel.

During this partitioning, no signal flow is allowed in the

transverse direction under the middle contact of the profiling redistribution gate. This requires a fast leading edge of the clock pulse on the first transfer gate of the split channel section. The transversal charge flow is also thwarted by the extension of the channel-split diffusion under the profiling gate. In the preceding section we have seen that such an extension also reduces the harmonic static distortion. Another advantage of the extension is a reduction in partition noise. The arguments for a considerable extension of the channel split under the redistribution gate have to be traded off against the increase of the time constant for the charge profiling under the redistribution gate. The latter requires a high conductance between the left- and right-hand charge packets.

An obvious cause of partitioning errors is a misalignment between the middle contact of the redistribution gate and the channel-split diffusion. If this misalignment is indicated as βW_m (see Fig. 6; W_m is the width of the conductive contact area) it causes an offset $\Delta h_k''$ in the actual tap-weight value equal to

$$\Delta h_k'' = \frac{2\beta W_m L}{A_c} \frac{Q_{m,k}}{Q_k}. \tag{15}$$

Here L denotes the length of the resistive gate and A_c is again the channel area under the conducting contact area of the gate. Expression (15) holds under the condition that the extension of the channel-split diffusion is completely covered by the conductive contact region A_c of the profiling gate. The alignment of the middle contact and channel-split diffusion with respect to other masks is not critical because proper operation is limited to charge packet sizes that do not reach the outer channel edges under the profiling gate.

The sensing of the partitioned signal-charge packets occurs when they have been transferred towards the split-electrode sense gates. The magnitude of the sensed charge packets is determined by the partitioning and the sense gate area has no influence. Consequently no critical alignment is necessary for the position of the split between the two sense gates. The constant-voltage sensing is applied and the attractive features of this method are fully exploited in the EPSEF. The equal size of the left and right sense gates is an additional advantage because the parasitic capacitances and the clock feedthrough are equal for both sides, irrespective of which filter function has been programmed.

V. EPSEF Implementation and Performance

An 8-tap EPSEF device has been implemented in n-channel surface CCD technology with double level overlapping polysilicon gates. One delay element is composed of two storage gates in the first polysilicon level and two transfer gates in the second level. Clocking of the profiling gates and of the split sense gates are avoided by operating the CCD in a $1\frac{1}{2}$-phase mode. For each delay section only one storage-gate can be kept at dc level, which implies that the profiling gates and sense gates have to be implemented at alternate CCD delay sections. The profiling gates, the intermediate clocked storage gates, and the sense gates are at the first polysilicon level. In Fig. 4 a schematic top view of one filter section is shown. The first polysilicon gate layer is obtained by chemical vapor-deposition of pure polycrystalline silicon. A uniform and reproducible sheet resistivity can be obtained in the range of 5-10 kΩ/□ by lightly doping of the polysilicon layer with phosphorus [16], [21]. Lower sheet resistivity would lead to undesired higher power dissipation in the resistive gates. The conductive polysilicon regions are doped from a chemical vapor-deposited oxide layer with a high phosphorus concentration. The contact areas in the resistive gates are also heavily doped in the same masking step in order to provide a low contact resistance with the aluminum interconnection layer. The other technological steps are standard in our n-channel surface CCD processing. The EPSEF processing requires six masks for standard CCD processing and one additional mask for the resistive polysilicon definition. Technological and layout parameters are summarized in Table I.

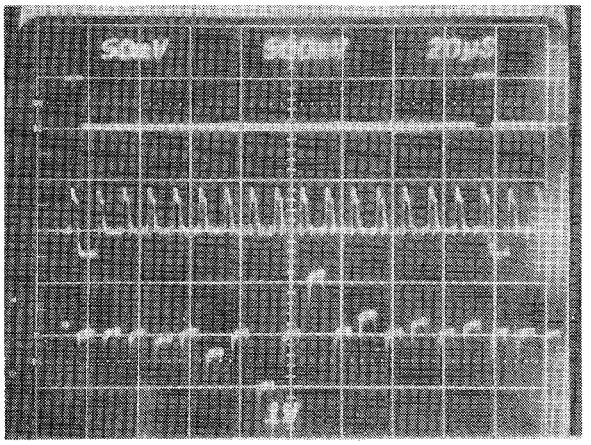
TABLE I
EPSEF Parameters

Substrate doping	$N_a = 1.5\ 10^{15}$ cm^{-3}
Oxide thickness	$d_{ox} = 0.10$ μm
Sheet resistivity of resistive polysilicon	$R_r = 6.5$ kΩ/□
Sheet resistivity of conducting polysilicon	$R_s = 50$ Ω/□
Channel width	$W = 400$ μm
Length of storage and sense gate	$L = 15$ μm
Length of transfer gate	$L_t = 10$ μm
Length of resistive gate	$L_r = 30$ μm
Width of channel splitting stopper diffusion	$W_s = 15$ μm
Width of contact area in resistive gate	$W_m = 20$ μm
Overlap of resistive gate and channel stopper	$L_{ov} = 15$ μm

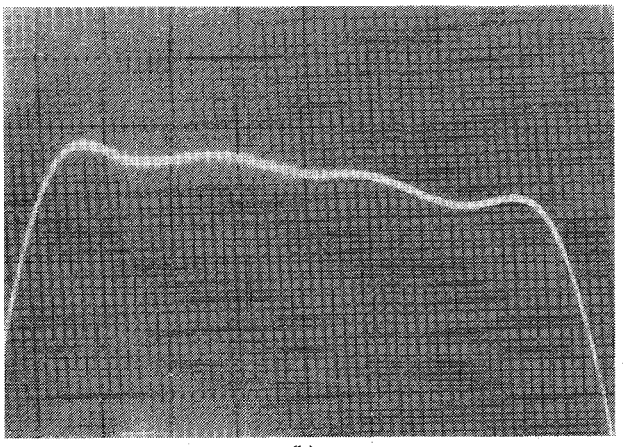
The filter structure with sense electrodes at alternate delay elements may be employed advantageously in two different ways. If the intermediate stages are considered as zero tap-weight elements, filters with a transfer function periodicity equal to $0.5f_c$ may be programmed. An example of such a filter is the Hilbert transformer with an odd number of taps [17]. In this application, the present EPSEF can be considered as a 15-element filter with eight programmable taps [see Fig. 7(a) and (b)].

In the other mode, the input signal plus dc background level is sampled every second clock period, while in the intermediate clock periods samples of the dc background signal are injected. The filter output now alternately represents a filter-output sample of the input signal plus background and of the dc background level. Subtraction of the alternate output samples provides the filtered input signal without offset due to the dc background signal. In this mode the device represents a transversal filter with four-quadrant multiplication between tap-weight factor and input signal. An additional advantage is that the subtraction at the output compensates the leakage charge in subsequent charge packets. This allows filter operation at low clock rates (200 Hz).

In the prototype EPSEF currently available, the tap-weight factors are set by external tap-weight voltages. For fixed filter applications with manual adjustment facility, external voltage-dividing potentiometer circuits are used. The filter performance was measured on a number of filter functions such as delay line function (only one tap at nonzero value), integrator, Hilbert transformer, Barker coded correlator, and low-pass filter. The diversity of these filter functions illustrates the ver-



(a)



(b)

Fig. 7. (a) Impulse response and (b) frequency response of the EPSEF, programmed as a 15-tap Hilbert transformer. The tap weights have been set according to (10), without trimming.

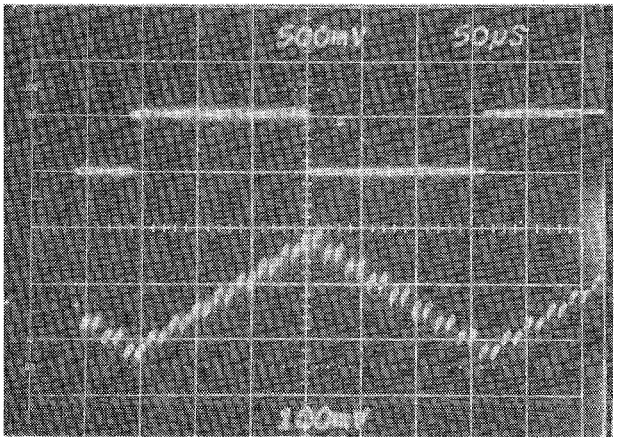


Fig. 8. Response to a square-wave input signal. All tap-weight factors have been set to the same value.

satility of the EPSEF. In Fig. 8 all filter coefficients have been set to the same value and the integral response to a square wave input signal is shown. The performance data of the EPSEF are summarized in Table II.

In addition to the tabulated data it is noted that replacement of the devices required adjustment of the tap-weight voltages $V_{tw,k}$ by maximal 0.1 V, which is 5 percent of the maximum tap-weight voltage range. The tap-weight control inaccuracy

TABLE II
EPSEF PERFORMANCE DATA

Transfer inefficiency per transfer	7.10^{-4}
Nonlinear distortion ($h_1 = 0.25$)	−42 dB
Signal/noise ratio ($h_1 = 0.25$, bandwidth: 50 kHz)	50 dB
Dynamic range (measured by 7 bit Barker code)	>50 dB
Clock frequency	200 Hz–250 kHz
Power consumption/tap	0.6 mW
Tap-weight control range	$-0.35 \leq h_k \leq 0.35$
Tap-weight control voltage range $V_{tw,k}$	$-1.4\ \text{V} \leq V_{tw,k} \leq 1.4\ \text{V}$
Tap-weight control nonlinearity	<1 percent

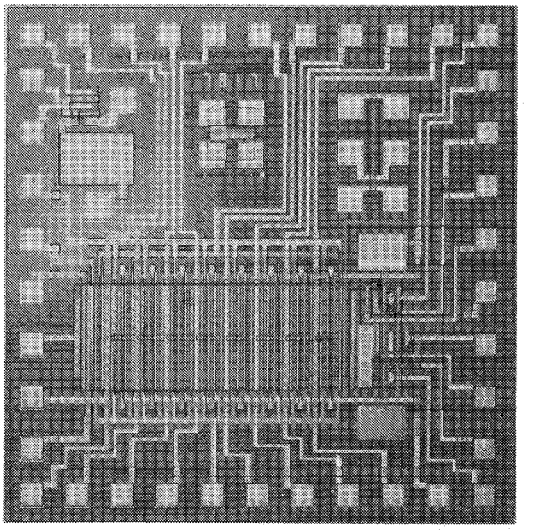


Fig. 9. Photomicrograph of the EPSEF. Chip size is 2 × 2 mm^2.

of the tap weights of one device was within 1 percent. Fig. 9 shows a photomicrograph of the EPSEF chip.

VI. APPLICATIONS

Probably the most promising application of the EPSEF is in adaptive filtering. A straightforward algorithm to determine the tap-weight factors in adaptive filters is the least mean square (LMS) algorithm described by Widrow *et al.* [18]. White *et al.* [19] have demonstrated the application of a modified version: the clipped data LMS algorithm, in combination with a programmable CCD transversal filter. We have also used the clipped data LMS algorithm to demonstrate the operation of the EPSEF as the linear combiner in an adaptive filter system. A block diagram of the adaptive filter system is shown in Fig. 10.

In essence the function of the algorithm is to optimize the tap-weight factors h_0–h_7 in order to minimize the power content of the output signal $e(t)$ as far as the correlated components of the input signals $d(t)$ and $x(t)$ are concerned. In other words, the algorithm controls the tap-weight factors h_0–h_7 in such a way that the response $y(t)$ of the EPSEF on the input signal $x(t)$, resembles $d(t)$ as closely as possible. The clipped data LMS algorithm have been hardware-implemented on printed circuit board. The required functions are: a comparator for the detection of the sign of the input signal $x(t)$, a binary shift register that delays the sign information in parallel with the actual signal sample in the EPSEF, and an

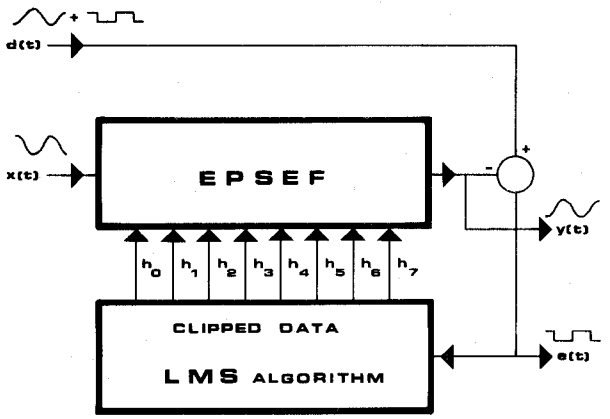


Fig. 10. Block diagram of the adaptive filter system, with the EPSEF as the linear combiner.

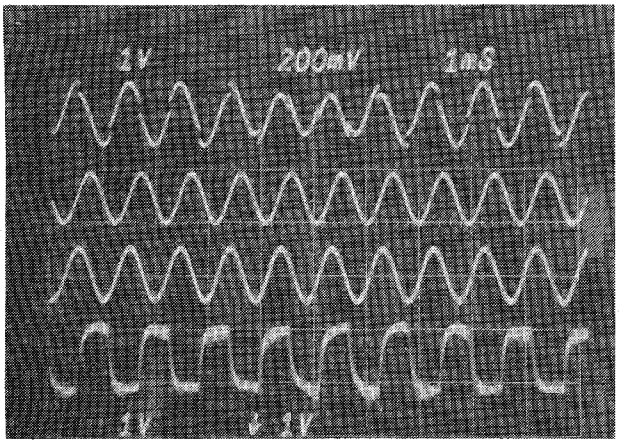
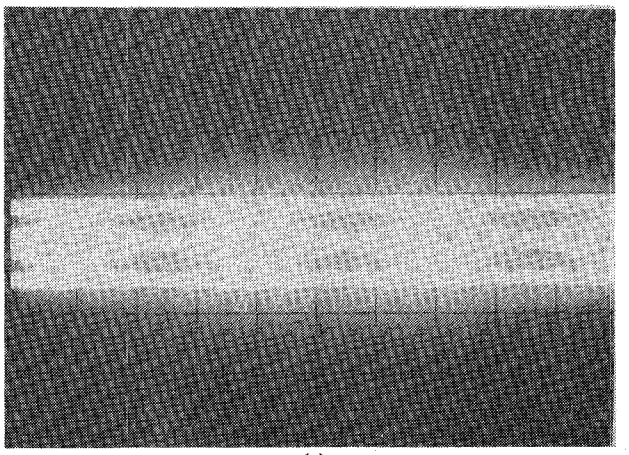
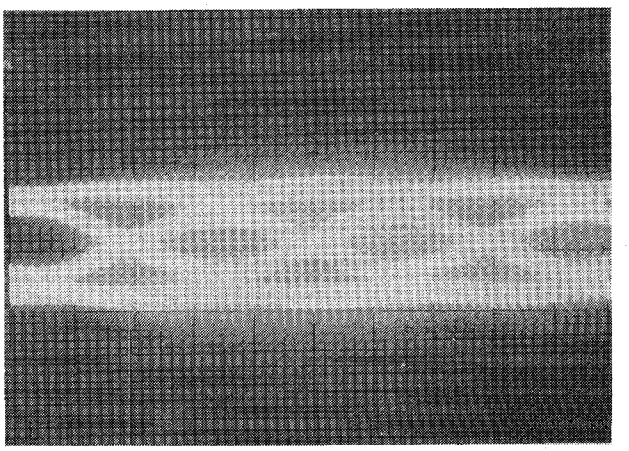


Fig. 11. Input and output signals of the adaptive filter system *a:* input $d(t)$, 1 V/div.; *b:* reference input $x(t)$, 1 V/div; *c:* output $y(t)$, 1 V/div.; *d:* output $e(t)$, 200 mV/div.; horizontal scale: 1 ms/div.; clock frequency of the EPSEF: f_c = 25 kHz.



(a)



(b)

Fig. 12. (a) Eye pattern of a random pulse rate that has passed a low pass filter; (b) eye pattern of the same setup after insertion of the EPSEF, programmed as the inverse of the low-pass filter.

integrator circuit for each programmable tap. The integrator circuit integrates the signal $e(t)$ multiplied by the appropriate sign information. With this adaptive system, parallel updating of the tap-weight factors is performed. The system adapts very fast (within 400 clock cycles) to variations in the input signals. In Fig. 11 the separation of a strong sinusoidal interference in the output signal $e(t)$ was attenuated by 40 dB with respect to the input signal $d(t)$.

Another promising application of programmable CCD transversal filters is as equalizers in data transmission along analog communication channels [20]. To demonstrate this application we simulated a channel characteristic with a fourth-order Butterworth low-pass filter. Fig. 12(a) shows the eye pattern of the unequalized channel. At the synchronized time moments, no clear detection of the positive and negative pulse pattern is possible. Fig. 12(b) shows the eye pattern after insertion of the EPSEF, programmed as a filter with a transfer function that is the inverse of the transfer function of the Butterworth low-pass filter. The eye opening is clearly visible and correct detection of the positive and negative data values at the synchronized time moments is possible.

The EPSEF design is potentially applicable in real-time analog correlator chips. The EPSEF already performs signal delay and analog multiplication at the subsequent taps. The output circuit is also incorporated and operates independently of the tap-weight programming. The extension to a correlator system requires a second CCD delay line, antiparallel to the EPSEF, which may be tapped by floating sense gates. A simple source-follower buffer or inverter stage can convert the tapped signals to a voltage and impedance level suitable for supplying the control voltages for the redistribution gates of the EPSEF. The EPSEF technology also allows the on-chip integration of the hardware required for the LMS algorithm for adaptive filter systems. In the present design the number of external connections for the tap-weight control sets a limitation for the implementation of longer filters. On-chip tap-weight control will permit the implementation of longer filters with more programmable taps.

VII. Conclusion

By effectuating the tap-weight multiplication in the charge domain, an electrically programmable split-electrode CCD transversal filter has been realized. The in-channel multiplication by analog tap-weight factors is based on electrically controlled charge profiling and partitioning of the charge packets, followed by differential charge sensing. In the EPSEF device, the charge profiling is accomplished by means of a resistive polysilicon gate that provides the control of the underlying

potential well. The partitioning is implemented by means of a stopper-diffusion split that separates the CCD section between the profiling gate and the sense gate segments into two parallel channels. Charge sensing and summation are carried out by means of the well-known split-electrode technique with constant-voltage sensing. The EPSEF device is a highly linear programmable filter with a low power dissipation and a very compact layout.

Because the tap-weight control circuitry is separate from the output sense-and-summation circuit, the device is very versatile. In comparison with split-electrode filters with fixed tap-weight factors, the dynamic range is reduced by 10 dB because the maximum tap-weight factor in the EPSEF is about one-third. The charge splitting is performed at the point with the highest charge density, which causes an increased partition-noise level. The performance data of the EPSEF (Table II) compare well with other analog programmable CCD transversal filters.

The in-channel tap-weight factor multiplication has been described for a surface channel CCD, but it applies as well to buried channel CCD's. In buried channel CCD's, however, the sensing of the partitioned charge packets (which will have unequal charge densities) may cause additional distortion due to the difference in gate-channel capacitance. In devices of both types, the charge redistribution is a linear function of the differential voltage applied to the outer contacts of the resistive gate. This analog multiplication principle may also find application in CCD input circuits and other sampled data structures.

Appendix

The Inversion-Charge Profile Under a Resistive Gate

For the sake of clearness and simplicity the polysilicon gate is assumed to have a homogeneous sheet resistivity. The contacts to the resistive gate are assumed to be line contacts parallel to the CCD channel. Contact series resistance is neglected. Consider the potential in a cross section (Fig. 5) of the CCD channel along the resistive gate. The gate potential varies linearly with the distance y from the center contact and when appropriate voltages are applied, a wedge-shaped potential well exists with

$$V_g(y) = \frac{-2y}{W}(V_l - V_m) + V_m \qquad \text{for } -\tfrac{1}{2}W < y \leqslant 0 \quad \text{(A.1)}$$

and

$$V_g(y) = \frac{2y}{W}(V_r - V_m) + V_m \qquad \text{for } 0 \leqslant y < \tfrac{1}{2}W. \quad \text{(A.2)}$$

In the absence of inversion charge, the surface potential $\phi_{s0}(y)$ at the Si-SiO_2 interface is a function of the gate potential $V_g(y)$. Here y denotes the distance from the center contact. If inversion charge is injected, the surface potential changes to $\phi_s(y)$, which depends on the gate potential along the resistive gate and on the total amount of injected charge. If the inverted region extends from y_l' until y_r' (see Fig. 5), $\phi_s(y) = \phi_{s0}(y)$ for $-\frac{1}{2}W < y < y_l'$ and for $y_r' < y < \frac{1}{2}W$ while $\phi_s(y) = \phi_{s0}(y_l') = \phi_{s0}(y_r')$ for $y_l' \leqslant y \leqslant y_r'$.

The inversion-charge density $Q_I(y)$ may be expressed as

$$Q_I(y) = \int_{\phi_{s0}(y)}^{\phi_s(y)} [C_{ox} + C_d(\phi_s)]\, d\phi_s \quad \text{(A.3)}$$

where C_{ox} is the oxide capacitance and $C_d(\phi_s)$ is the depletion capacitance per unit area. By tedious calculations one arrives at

$$Q_I(y) = -[V_g(y) - V_g(y')]\, C_{ox}. \quad \text{(A.4)}$$

This expression can also be derived directly along the following lines: the same inversion charge density $Q_I(y)$ is obtained by changing the gate potential at y from $V_g(y')$ to $V_g(y)$, while the surface potential is kept constant at $\phi_{s0}(y')$. No change of depletion charge density will occur and (A.4) is a direct result of the integral expression

$$Q_I(y) = -\int_{V_g(y')}^{V_g(y)} C_{ox}\, dV_g. \quad \text{(A.5)}$$

If the charge packet Q_k at the kth profiling gate inverts the Si-SiO_2 interface from y_l' until y_r' (Fig. 5), the inversion charge under the left and right half of the profiling gate is equal to

$$Q_{l,k} = L \int_{y_l'}^{0} Q_I(y)\, dy \quad \text{(A.6)}$$

and

$$Q_{r,k} = L \int_{0}^{y_r'} Q_I(y)\, dy. \quad \text{(A.7)}$$

With (A.1), (A.2), and (A.4) it is seen that the integrand of (A.6) varies in the interval $[0, y_l']$ comformably with the integrand of (A.7) in the interval $[0, y_r']$ and the ratio of the charge packets is

$$\frac{Q_{l,k}}{Q_{r,k}} = \frac{-y_l'}{y_r'}. \quad \text{(A.8)}$$

From the condition $Q_I(y_l') = Q_I(y_r') = 0$ it follows with (A.4) that $V_g(y_l') = V_g(y_r')$. Substitution in (A.1) and (A.2) gives

$$\frac{-y_l'}{y_r'} = \frac{V_{r,k} - V_m}{V_{l,k} - V_m}. \quad \text{(A.9)}$$

With (A.6) and (A.7) and remembering that $Q_k = Q_{l,k} + Q_{r,k}$, the following expressions are derived

$$Q_{l,k} = \left(\frac{V_m - V_{r,k}}{2V_m - V_{l,k} - V_{r,k}}\right) Q_k \quad \text{(A.10)}$$

and

$$Q_{r,k} = \left(\frac{V_m - V_{l,k}}{2V_m - V_{l,k} - V_{r,k}}\right) Q_k. \quad \text{(A.11)}$$

Expressions (A.10) and (A.11) have been derived here for surface channel CCD's, but they also hold for buried channel CCD's. In buried channel CCD's, the mobile channel charge, rather than the inversion charge has to be considered. The

simple expression (A.4), however, is not valid because of the capacitance between gate and channel is not constant. This will hinder the linear sensing of the partitioned charge packets with different charge densities in buried channel CCD's. It is easily seen that in this case too, the mobile charge density profile under the right half of the gate can be obtained by conformal mapping of the profile under the left half of the gate. As only this property of (A.3) and (A.5) has essentially been used in the previous derivation, the results (A.10) and (A.11) also hold for buried channel CCD's.

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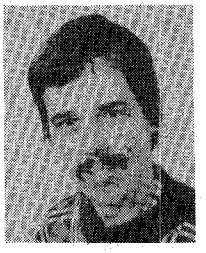

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