Magnetic-film atom chip with 10 μm period lattices of microtraps for quantum information science with Rydberg atoms

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We describe the fabrication and construction of a setup for creating lattices of magnetic microtraps for ultracold atoms on an atom chip. The lattice is defined by lithographic patterning of a permanent magnetic film. Patterned magnetic-film atom chips enable a large variety of trapping geometries over a wide range of length scales. We demonstrate an atom chip with a lattice constant of 10 μm, suitable for experiments in quantum information science employing the interaction between atoms in highly excited Rydberg energy levels. The active trapping region contains lattice regions with square and hexagonal symmetry, with the two regions joined at an interface. A structure of macroscopic wires, cutout of a silver foil, was mounted under the atom chip in order to load ultracold ^{87}Rb atoms into the microtraps. We demonstrate loading of atoms into the square and hexagonal lattice sections simultaneously and show resolved imaging of individual lattice sites. Magnetic-film lattices on atom chips provide a versatile platform for experiments with ultracold atoms, in particular for quantum information science and quantum simulation. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4874005]

I. INTRODUCTION

The last decade has witnessed the development of lattice structures for trapped ultracold neutral atoms or ions, where they can be coherently controlled and manipulated. These lattices have already been very successful as platforms to simulate a large variety of quantum phenomena, including quantum many-body physics.[1–10]

For neutral atoms, optical lattices have been the norm, with lattice parameters of about 0.5 μm and interaction among neighbouring sites provided by tunneling. Lattices with larger lattice parameters, in the range of 5–10 μm, are now attracting increasing interest.[11,12] This longer length scale is well suited to implement tunable, switchable interactions among individually addressable sites, by exciting atoms into highly excited Rydberg levels. This approach is presently subject of intense theoretical and experimental investigation.[13–18]

We recently demonstrated an alternative technique to create two-dimensional neutral-atom lattices, based on a patterned film of magnetic iron-platinum (FePt) alloy on an atom chip.[19,20] This hybrid system combines the advantages of lithography techniques with cold atom experiments. Magnetic lattices offer unique opportunities that are in many ways complementary to those offered by the optical variety.[21–23] They can be used to extend the range of length scales to both larger and smaller lattice parameters, each giving access to very different regimes of quantum simulation.[24] While smaller (~100 nm) length scales could push Hubbard models into parameter regimes beyond what is now achievable using optical lattices,[25,26] in this paper we concentrate on the longer length scale.

Here, we present a detailed description of an improved setup for magnetic-film atom chip lattice experiments, utilizing 10 μm lattice spacings, geared toward the Rydberg route described above. This atom chip is an important advance toward the application of chip-based magnetic lattices as a quantum information platform where interactions will be mediated by exciting atoms to Rydberg levels. The spacing of 10 μm is within reach of dipole-dipole interactions between atoms in highly excited Rydberg levels.[16–18,27] At the same time the lattice spacing is large enough to easily resolve individual traps, providing optical access at will, using off-the-shelf optics. Since the atom-to-chip trapping distance scales with the lattice period, these chip based traps also provide access to measurements of the interaction of (Rydberg) atoms with the surface at the micrometer scale.[28–31]

Magnetic lattices offer virtually unlimited flexibility in the design of lattice patterns, including non-periodic patterns and controlled amounts of disorder. Regions of different functionalities, or lattices with different length scales or geometries can be combined in a single pattern. As an example of

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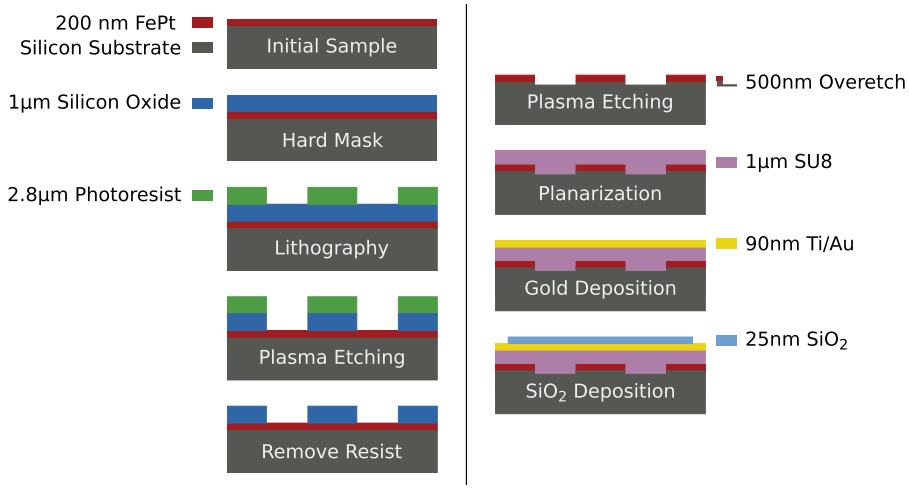

FIG. 1. Processing steps in the chip fabrication sequence, see text.

the design flexibility that magnetic lattices have to offer, we demonstrate the loading of atoms into a square and a hexagonal lattice that are joined at an interface.

The paper is structured as follows. In Sec. II, we present the microfabrication procedure used for the fabrication of this atom chip. In Sec. III, we describe the technical aspects of the chip mount assembly. In Sec. IV, we present our first experimental results and demonstrate the loading of atoms into the microtraps.

II. MICRO-FABRICATION OF THE MAGNETIC FILM ATOM CHIP

The atom chip is based on iron platinum, a hard magnetic material, so that the magnetization is robust against externally applied magnetic fields that are small compared to the coercivity.[32] The FePt films were supplied by Hitachi Research San Jose and have already been used in the fabrication of our previous generation of atom chips.[20] The films have high remanent magnetization ($M_r = 670$ kA/m), coercivity ($\mu_0 H_c = 0.95$ T), and Curie temperature (estimated $T_C \gtrsim 450\,^\circ$C).[33] Using scanning electron microscopy (SEM) we find that the size of individual grains of FePt within our samples is typically 40 nm. This grain size currently poses no limitation for the 10 μm period lattices presented here. The atom chip consists of a 200 nm thick FePt film deposited on a 330 μm thick silicon substrate, 15 $\times$20 mm^2 in size.

The magnetic lattice pattern has been designed using an optimization algorithm for creating traps in arbitrary lattice configurations, while optimizing for maximum trap stiffness.[34] The optimization typically yields a binary pattern containing pixels with either zero or maximal magnetization. Such patterns can easily be produced by etching away the pixels with zero magnetization. The versatility of this technique allows us to optimize both the square and hexagonal lattice geometries used in our experiment. These two designs are then connected together at an interface. With an eye on the intended application as a quantum information platform, an obvious difference of the two geometries is the number of nearest neighbors of each lattice site.

A. Patterning, etching, and planarization

The design pattern is transferred to the FePt film by UV-optical lithography at the fabrication facility of Ben-Gurion University of the Negev, Israel. The lithography procedure is shown in Fig. 1. First, a lithographic mask is made by depositing a layer of 1 μm of silicon oxide onto the FePt, followed by 2.8 μm of photo-resist. After the exposure and development of the resist, the silicon oxide is plasma-etched. The remaining photo-resist is removed by wet etching. Using the silicon oxide as the mask, the FePt is then etched by direct argon ion etching to complete the pattern transfer (Fig. 2).

The chip surface also acts as a mirror for the magneto-optical trap (MOT)[35,36] and for the imaging beams. Therefore, optical flatness is required to reduce the formation of interference fringes resulting from light reflecting off the etched and non-etched regions of the chip. As the height difference between etched and non-etched regions (including overetch) is similar to the wavelength of the light (780 nm) used for cooling and imaging of the atoms, interference effects are particularly relevant. The etched surface is therefore planarized with the polymer SU8, commonly used as a photo-resist. After deposition, the chip is baked at 150 °C for 24 h, to increase the hardness of the SU8 and to limit its outgassing in ultra-high vacuum. The total thickness of the deposited SU8 is 1 μm with a flatness of less than 9 nm, as measured by atomic force microscopy (AFM).

B. Reflective and protective coatings

After planarization a 90 nm thick gold coating is deposited, giving the surface the necessary reflective properties for the mirror MOT. In previous experiments, we found that the non-uniform adsorption of rubidium atoms onto the gold chip surface led to stray electric fields. These could be observed as energy shifts of Rydberg levels by electromagnetically induced transparency (EIT) spectroscopy.[28] To prevent the direct exposure of the gold surface to rubidium vapor, an extra layer of 25 nm of quartz (SiO_2) is deposited on top of the

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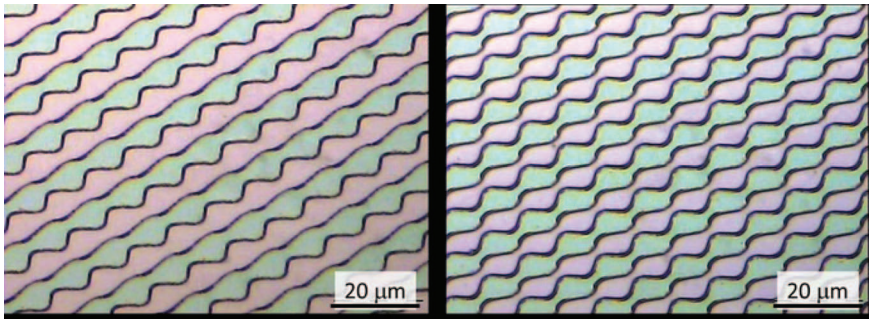

FIG. 2. Patterns on the chip after the etching process. The alternating strips are etched and non-etched regions. The pattern on the left generates a magnetic lattice with square translational symmetry. The lattice pattern on the right has hexagonal (equilateral triangular) symmetry.

gold surface.[37] Rubidium atoms adsorb less strongly to quartz than to gold and are more easily removed via light-induced atomic desorption (LIAD) with blue or ultraviolet light.[38,39] The corners of the chip are left uncoated with quartz so that the gold surface can be electrically grounded to the mount. As the final step in the preparation of the atom chip, the FePt layer is magnetized by applying an external magnetic field of 5 T in the out-of-plane direction.

III. DESIGN AND CONSTRUCTION OF THE ATOM CHIP MOUNT

The chip is clamped on top of a construction of silver wires. These wires support electrical currents and serve to magnetically trap atoms before they are loaded into the chip lattice. The silver wire pattern is glued on top of a copper mounting structure for mechanical stability and to transport heat away from the chip. The glue also acts as an electrical insulator. The entire construction is mounted in ultrahigh vacuum. This section describes the various components.

A. Supporting wire pattern

The wire pattern design as shown in Fig. 3 features two opposing "h"-shaped silver wires. Each "h"-wire can be used in either a "U" or a "Z" configuration. The U-sections in the h-wires are complemented by an additional set of U-wires for greater current capacity and more flexibility in positioning. Sending current through the U-wire allows us to trap atoms in a MOT near the surface. The Z-wires, in combination with an external bias magnetic field, create an Ioffe-Pritchard (IP) type magnetic trap.[36,40,41] This IP trap is used to load atoms and to position the initial cloud before loading the atoms into the final magnetic microtraps. The Z-wires are centered beneath one magnetic lattice region out of the possible two regions, shown as a red-brown patch in Fig. 3 [around $(x, y) = (0, 0)$]. Having duplicate trapping regions gives us the possibility of switching the orientation of the chip or use the second trapping region, should the first region be damaged.

The outermost wires along the y-direction can be used as "pinch" wires, providing extra axial confinement for the Z-wire trap. Unfortunately, the silver wires have not been

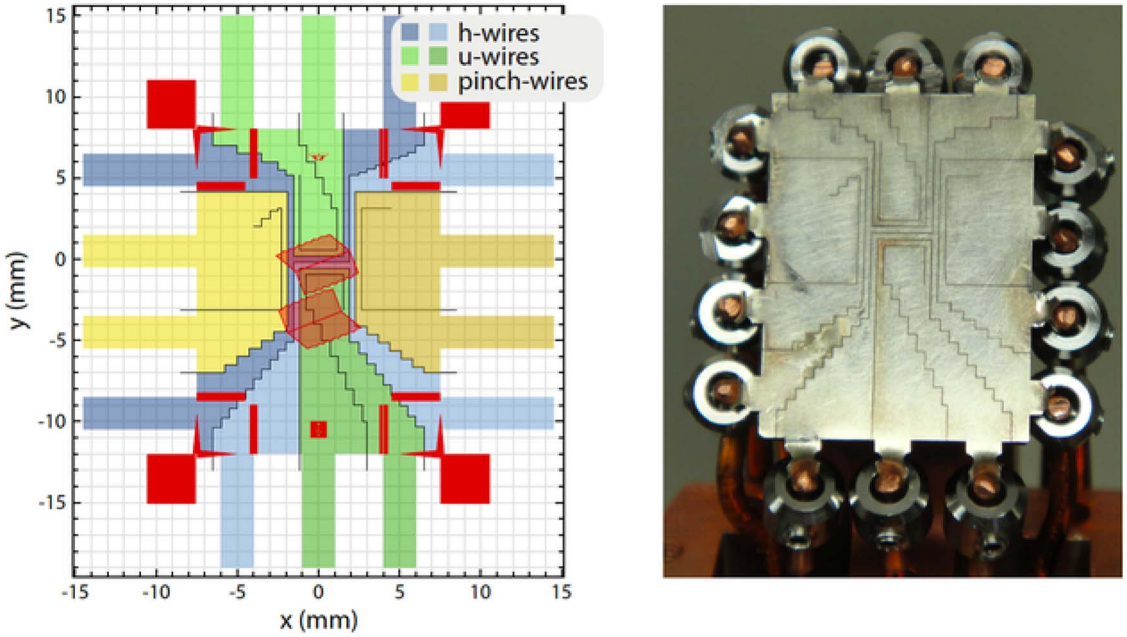

FIG. 3. Silver foil: (Left) schematic drawing with Z- and U-wires for atom trapping. Overlayed in red-brown are the two regions of permanent magnet patterns. (Right) Image of the silver foil, glued onto its copper base, and fully connected.

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useful for delivering radio-frequency (RF) magnetic fields to the atoms for forced evaporative cooling. This is due to the strong capacitive coupling between the wires and the copper base, effectively shorting the RF current before the power reaches the active part of the chip.

The fabrication procedure of the silver wire pattern begins with the preparation of a 250 μm thick sheet of tempered, flattened silver foil (Goodfellow). This foil is first annealed in argon gas with 5% H_2 at 650 °C and then reflattened at a pressure of 10 kN/cm^2.

Spark erosion is used to cut the foil into the trapping wire pattern shown in Fig. 3. For the spark erosion, AGIE EMT 1.1 LF equipment is used with a wire of 50 μm diameter (sample courtesy of Microcut). During the cutting process the wires are held together in a frame, which remains in place until after the gluing stage. After rinsing with ethanol, the trapping wires are argon plasma-etched in an AJA sputtering device and coated on the gluing side with ~40 nm chromium to promote adhesion.

We use a low out-gassing, high thermally conducting, electrically insulating epoxy (Epotek H77S) to fill the gaps between the trapping wires and secure the silver foil to the copper base. The mixed H77S epoxy is degassed for 1 h at 40 °C after which ~0.05 g is applied to the chromium coated side of the trapping wires. After waiting until the gaps are filled, the trapping wire foil is carefully placed on the sandblasted and leveled copper base. The trapping foil is forced onto the copper base by capillary action, leaving only a monolayer of glue filler grains in-between the silver and the copper. The 20 μm boron nitride (BN) filler grains of the H77S act both as an electrical insulator and a separator, keeping the trapping wires away from the copper base with minimal thermal resistance. The glue is hardened for 1 h at 150 °C. Excess glue on the top of the foil is ground away.

B. Mechanical construction

The electrical connections to the silver wires are provided by 14 Kapton insulated copper wires leading to a 20-pin vacuum feedthrough. The current is limited to 10 A per pin by the maximum loading of the vacuum feedthrough. IR imaging of the wires placed outside the vacuum reveals a ~10 K temperature rise at 20 A (using two feedthrough pins in parallel), as shown in Fig. 4. This test shows that the heat is mainly concentrated in the connections to the electrical feedthrough, where temperatures up to 60 °C have been observed. Using square wires cutout of silver foil allows us to run high currents as close as possible to the magnetic structure. This creates a very localized and high-gradient magnetic trap, with field gradients up to ~15 T/m and usable radial trap frequencies up to ~2 kHz.

The silver flaps extending from the trapping wires are connected to the vacuum feedthrough with 1.5 mm diameter Kapton-insulated, oxygen-free-high-conductivity (OFHC) copper wires. To protect the silver joints, the silver flaps are pre-bent in order to prevent damage by thermal expansion, and the tips of the clamping screws are slightly rounded to minimize torsion. To allow a current of 20 A to flow through the Z-shaped wires, two pins of the feedthrough are connected

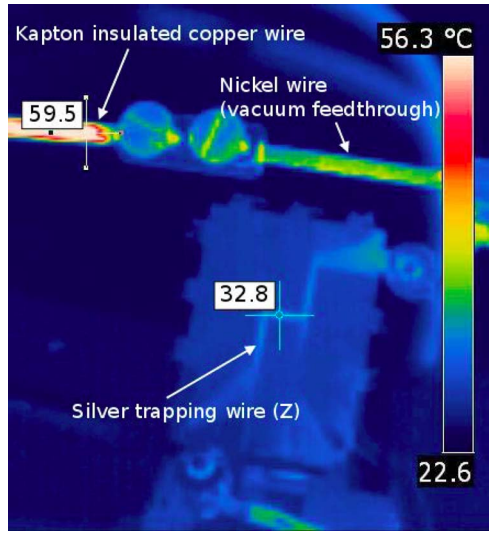

FIG. 4. Heating bench test of the silver foil and a connector to the vacuum feedthrough. The lower part shows a thermal infrared image of one of the Z-wires while carrying 20 A. The upper part of the image shows one connector to the vacuum feedthrough. Note that inside the vacuum system these components are far away from each other. They have been arranged on the bench to appear in one picture.

in parallel. The titanium socket for the rubidium dispenser is screwed onto the copper base keeping the dispenser just below the line of sight of the atom chip surface.

The chip is clamped directly onto the silver wires by four titanium springs, allowing for easy replacement of the chip. The chip surface is electrically grounded to the copper base via the titanium springs.

The copper base carrying the atom chip is glued (Epotek E4110LV) to a copper support tube, providing a good thermal connection to the vacuum parts with high mechanical stability (Fig. 5). The copper support tube is attached onto a reducing flange and attached to a CF63 cube. The resulting structure containing the mounted chip is finally enclosed by a glass cuvette, which is connected to the same reducing flange and serves as the experimental chamber.

C. In-vacuum lens mount

The chip mount and vacuum chamber are designed to allow for as much optical access as possible. Our starting point for the experiments is based on laser trapping and cooling ^{87}Rb atoms in a standard mirror MOT configuration.[36] The mirror MOT uses four 780 nm wavelength laser beams, with two counter-propagating beams reflected by the chip at a 45° angle. An extra 780 nm beam is used for absorption imaging. For good optical imaging resolution, as well as addressing of single sites, an aspheric lens with numerical aperture NA = 0.4 (Edmund Optics NT47-727, F = 18.75 mm, D = 15 mm) is mounted directly above the chip, inside the vacuum system. Based on these parameters we expect a diffraction-limited optical resolution of 1.2 μm (Rayleigh criterion), well below the trap lattice spacing of 10 μm. We also expect a detection sensitivity of approximately a single atom per site per shot.[42,43] The lens is held by a titanium lens holder, which is connected to the base mount by two quartz

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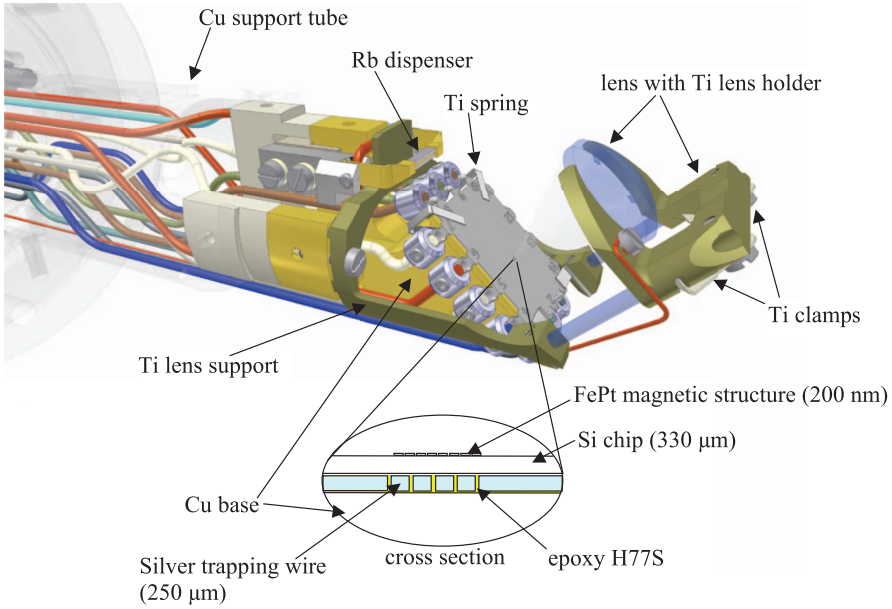

FIG. 5. Schematic of design for the atom chip mount.

rods, as shown in Fig. 6. The lens holder is fastened to the rods by two clamps, relying only on the mechanical flexibility of the clamps in order to minimize stress on the quartz rods and to prevent them from breaking. The clamps, lens support, and lens holder are all made of titanium to minimize influences on the magnetic field. The lens surface facing the chip was coated with Indium Tin Oxide (ITO) and a dielectric anti-reflection coating. The ITO coating is electrically connected to one of the pins in the electrical feedthrough and to the lens holder by a droplet of conducting Epotek E4110LV glue. This can be used to apply an electric field using the lens surface as an electrode and the chip surface as a (ground) counter electrode, as explained in Sec. II B. The ability to create an electric field gradient above the chip is an important tool for the future manipulation of Rydberg atoms.

Focusing the lens on the atoms is done by un-tightening the screws holding the clamps, and gently tapping on the lens holder. A laser beam passing through the lens is reflected by the chip and the outcoming light is compared to a reference beam traveling an equal distance (to correct for the natural divergence of the beam). The reference and chip beams are projected onto a CCD and the $1/e^2$ size is compared. When the reference and chip beams are of equal size and divergence, the lens is focused on the chip. We started with the lens too close to the chip, giving a strongly divergent beam. By tapping from this side toward equally sized beams we avoid a focus of the beam in between the camera and the chip. The depth of focus for the chosen optics is 5.2 μm. Since the atoms are trapped at $\sim$7 μm from the chip surface we cannot bring both the atoms and their reflections into the focus simultaneously. We chose to focus on the surface of the chip and use outside lenses for optional corrections. Beam divergence indicates that we have moved the focal point of the lens to within 15 μm from the surface of the chip. With a tapping precision of about 20 μm, this was accepted as optimal. After focusing, the clamps are tightened and the cuvette is carefully positioned over the entire assembly. To ensure that the lens stays in focus during the bakeout procedure, several thermal cycling tests have been performed. The imaging system is completed with extra lenses outside the vacuum system, to focus the image onto a CCD camera, and to adjust the magnification. Final focusing is done by moving the outside lenses and the position of the CCD camera.

D. Vacuum setup

The vacuum system for our experiment is based on a stainless steel (SS 304) cube containing six CF-63 ports. Opposite to the glass cuvette containing the chip, a 20 pin/10 A feedthrough is mounted for the electrical connections to the silver wires and the dispenser. The other four ports are used to connect the ion getter pump, the ion gauge, the turbo pump valve, and an extra 4-pin feedthrough for the electric field connections and *in vacuo* thermocouple. All materials used in the vicinity of the atom chip have been carefully chosen to be nonmagnetic, including: copper, silver, titanium, chromium, Kapton-insulated copper wires, Epotek glue, a rubidium dispenser, and SS 316 steel screws (Fig. 5).

A bakeout procedure is required in order to reach ultra high vacuum pressures. Bakeout temperatures are limited to 150 °C in order to prevent loss of magnetization of the FePt structure on the chip. After initial pumping with a turbo pump, a titanium-sublimation pump, and an ion getter pump, we gradually heat the whole system to 150 °C. After pumping for a week and subsequent cooling, a base pressure of 1×10^{-11} mbar has been achieved. As the atomic source we use enriched rubidium dispensers (Alvatec, s-type) to minimize the required gas load while achieving sufficient vapor pressure for a MOT. The dispenser is located along one of the short edges of the chip and is used in pulsed-mode[44] to extend the lifetime of the atoms in the trap as we use a single-chamber.

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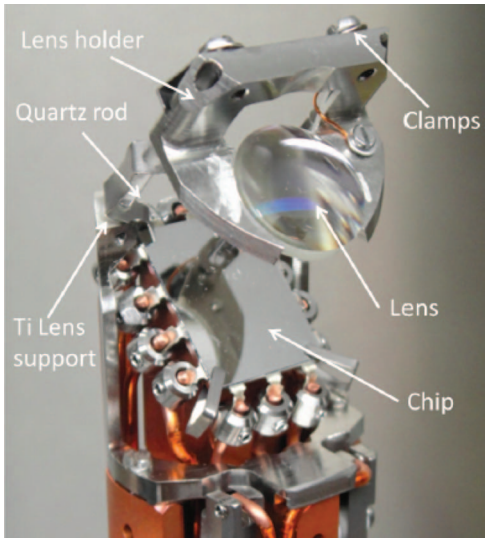

FIG. 6. Mounted atom chip and in-vacuum lens attached to the Ti-lens holder.

IV. LOADING ATOMS INTO THE MICROTRAPS

After the bakeout and alignment, we initially load 7×10^7 atoms of ^{87}Rb into the MOT using the dispenser in pulsed-mode. The initial cloud is then positioned using the U-wire, and cooled to 50 μK using optical molasses. After optical molasses, the cooled atomic cloud is optically pumped into the $|F = 2, m_F = 2\rangle$ state. The atoms are then loaded into the magnetic trap using the Z-wire of the chip, in combination with external magnetic coils.

Once in the magnetic trap, the atomic cloud is further compressed and cooled to 10 μK by performing RF-evaporation. In order to load atoms into the microtrap array, the atomic cloud needs to be brought closer to the chip surface. This can be done by decreasing the current through the Z-wire I_Z, and/or increasing the external bias field component B_y perpendicular to the central Z-wire section. Both methods compress the atomic cloud and push it toward the surface. Starting at a distance of approximately 600 μm from the surface we compress the trap from a radial trap frequency of $\omega = 2\pi \times 200$ Hz-$2\pi \times 800$ Hz and move the trap to a distance of approximately 200 μm from the chip. Typical trap parameters at this point in the loading sequence are: $I_Z = 17.5$ A, $B_x = -1.5$ G, and $B_y = 50$ G.

To lower the atomic cloud into the microtraps, we turn off the current through the Z-wire and ramp the bias fields to $B_x = 2$ G and $B_y = 5$ G. The microtraps are located at a distance to the chip of 6.6 μm with a calculated radial trap frequency of $\omega = 2\pi \times 25$ kHz for the square lattice and $2\pi \times 40$ kHz for the hexagonal lattice. The component of the external field along the quantization axis of the IP field at the center of the atomic cloud is changed during the loading procedure, to prevent this component from crossing zero field. This turns out to be crucial to prevent spin-flips and thereby loss of a large fraction of the trapped atoms. An absorption image of a successfully loaded lattice of microtraps is shown in Fig. 7.

The atom chip has active trapping regions containing both square and hexagonal lattice geometries. These are clearly distinguishable in Fig. 7 where the hexagonal lattice is on the left hand side and the square lattice on the right hand side. Initial analysis has been done to determine the atom number and temperature; these values are dependent on the bias field. Based on 41 absorption images and on the analysis of 175 (435) traps for the square (hexagonal) lattices, respectively, we determine that we have on average ~360 atoms per site in the square region and ~440 atoms in the hexagonal region. *In situ* temperature measurements based on RF-induced atom loss spectroscopy show average temperatures of 35 $\pm$ 6 μK and 32 $\pm$ 5 μK for the square and the hexagonal regions, respectively. We find that the offset field at the trap

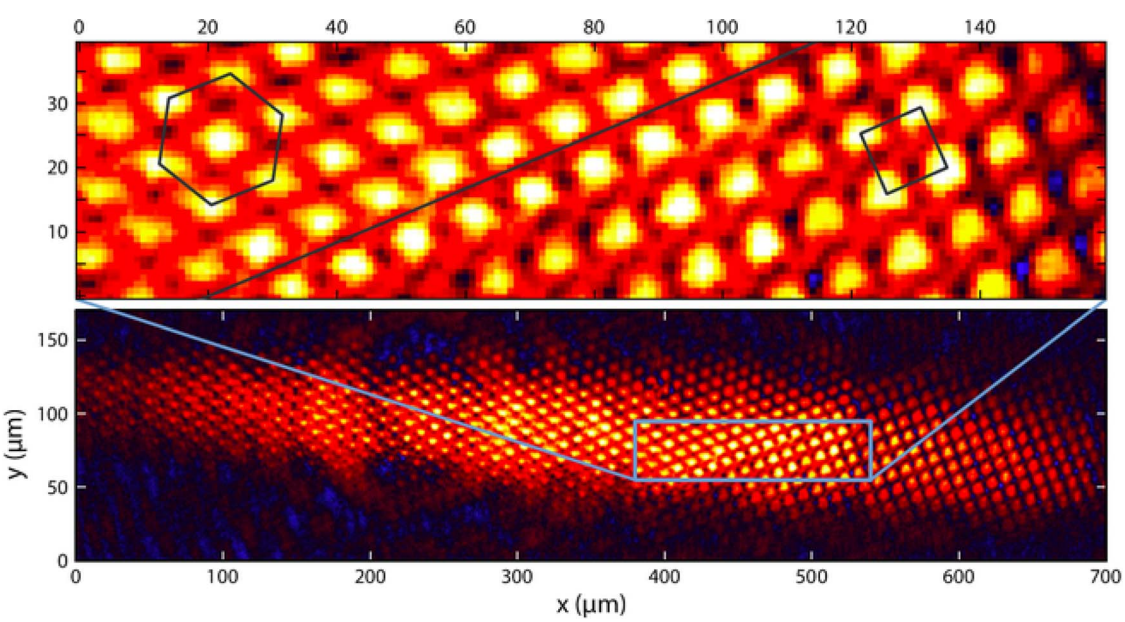

FIG. 7. Absorption imaging of the loaded magnetic lattice. The rubidium atoms are loaded simultaneously into hexagonal (left side) and square (right side) lattices. A magnified view of the center region with the crossover between both geometries is shown in the upper part.

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bottoms is 2.72(4)(16) G for the square and 1.97(3)(14) G for the hexagonal region, where the parentheses present the fitting error and the trap-to-trap variation, respectively.

V. CONCLUSION AND OUTLOOK

We have described the design and construction of an advanced atom chip based on a lattice of permanent magnetic microtraps for neutral atoms. Considerations which we have taken into account include: the electrical current load and thermal load of the preliminary magnetic trap based on current conducting wires, the possibility for rapid chip exchange, the mechanical stability of the chip, compactness and space limitations, optical accessibility and the requirement to image with a resolution in the micrometer range, and the needs of ultra-high vacuum. Following the construction and initial testing, the new atom chip has been placed in vacuum and finally tested by loading rubidium atoms into the magnetic microtraps after a sequence of compression and cooling stages. Having atoms in a 10 μm spacing lattice on an atom chip will allow us to access the Rydberg dipole-dipole interaction regime required for quantum information experiments.

The same approach using magnetic lattices on a chip could also be used for scaling down the lattice period to the 100 nm range. The distance between the traps and the chip surface will scale down linearly with the lattice period. Nevertheless, we estimated in previous work that the microtraps will easily overcome the Van der Waals attraction to the surface.[24] While no longer compatible with Rydberg excitation, these lattices would push Hubbard models that are now studied in optical lattices into novel parameter regimes.[25,26] In particular, the tunneling rates and interaction energies will be greatly increased compared to optical lattices. We also estimated that heating due to Johnson noise originating in the conducting surface[45–48] should not be prohibitive, owing to the small thickness of the magnetic films and their low conductivity. The strong heating effects observed in ion traps[49] close to surfaces do not play a role either, since no radio-frequency fields are involved.

To reach smaller dimensions, we will need new materials and new methods of fabrication which include magnetic films with smaller grain size. In addition, it will be necessary to switch from UV optical lithography to e-beam lithography. The ultimate limits on permanent magnet atom chips will be determined to a large extent by advances in the fields of magnetic materials and magnetic storage.

Several exciting directions for the development of atom chips based on permanent magnetic films lie ahead. Technological advances such as multi-layering can be exploited to enable single site addressability with large parallelism. An atom chip of multi-layers will allow the incorporation of a layer of electrodes, which can be fabricated from a low conductance material with reduced Johnson noise such as ITO. This electrode layer will enable single site addressability by having tiny local electric fields act on the atom, taking it in and out of resonance with RF, microwave, or light radiation. The ability to address a single atom within a large-scale two-dimensional atomic register enables the demonstration of algorithms which have so far been out of reach for both neutral atom and ion systems, and stands at the foundation of digital quantum simulation.

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