Design of Active N-path Filters

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***Abstract*—A design methodology for synthesis of active N-path bandpass filters is introduced. Based on this methodology, a 0.1-to-1.2 GHz tunable 6th-order N-path channel-select filter in 65 nm LP CMOS is introduced. It is based on coupling N-path filters with gyrators, achieving a "flat" passband shape and high out-of-band linearity. A Miller compensation method is utilized to considerably improve the passband shape of the filter. The filter has 2.8 dB NF, +25 dB gain, +26 dBm wideband IIP$_3$ (Δf = +50 MHz), an out-of-band 1dB blocker compression point B$_{1dB,CP}$ of +7 dBm (Δf = +50 MHz) and 59 dB stopband rejection. The analog and digital part of the filter draw 11.7 mA and 3-36 mA from 1.2 V, respectively. The LO leakage to the input port of the filter is ≤ -64 dBm at a clock frequency of 1 GHz. The proposed filter only consists of inverters, switches and capacitors and therefore it is friendly with process scaling.**

***Index Terms*—N-path, bandpass, filter, tunable, passive mixer, gyrator, BPF, channel select, CMOS, high out-of-band linearity, IIP$_3$, compression point.**

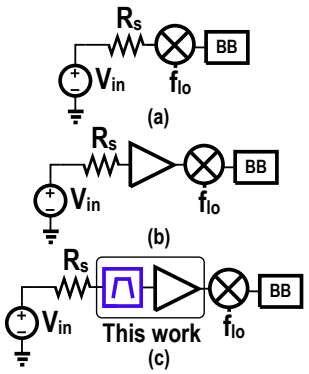

Fig. 1. (a) A mixer-first receiver (b) Addition of an LNA to improve the sensitivity of the receiver but at the cost of degradation in linearity (c) Proposed work

I. Introduction

CURRENT CMOS receivers exploit SAW filters to sufficiently attenuate large out-of-band blockers to prevent SNR degradation due to increase in noise and distortion. To cover different standards, multiple SAW filters should be utilized which clearly increases cost and form factor. Therefore, it is desirable to have an integrated bandpass filter with the following features: 1) high selectivity to mitigate large out-of-band blockers to relax the out-of-band linearity requirement of the subsequent stages in the receiver chain; 2) high dynamic range (DR) and 3) a flexibly tunable center frequency. A simple yet effective way to enhance the linearity of the receiver is to eliminate the LNA from the receiver chain. In this manner, mixer-first receivers [1], [2] achieve an excellent linearity but at the cost of degradation in the NF. It should be noted that due to $1/f$ noise issues, mixer-first receivers are not friendly with process scaling. Of course, it is possible to use an LNA to improve the sensitivity of the receiver but at the cost of degradation in out-of-band linearity (Fig. 1(a) and (b)).

There are several techniques to implement an integrated CMOS bandpass filter (BPF). One possible option is to exploit SiP (System in Package) solutions using FBAR resonators with Q-factors in the range of 1k [3]–[5]. However, this method is quite expensive and more importantly, intrinsically, these types of filters have a very limited tunability. Q-enhanced CMOS LC filters [6]–[9] suffer from a limited DR due to the low Q-factor of on-chip inductors and have a limited tuning range. Moreover, due to utilization of inductors, they are not process scalable. G$_m$-C filters [8]–[12] cope with severe trade-offs among different aspects of the design such as f_c, P$_{DC}$, DR and Q-factor and the need for separate tuning circuitry. On the other hand, N-path filters [13]–[23] can provide us with: 1) a flexibly tunable center frequency and 2) potentially high Q-factor and DR. Interestingly, they can decouple the required Q-factor from the DR range of the filter which is an issue in G_m-C filters.

In this work, a widely-tunable 6th order BPF with +25 dB of embedded amplification, bandwidth of 8 MHz and 60 dB of stopband rejection is introduced. In this way, while the blockers are eliminated by filtering, the passband gain of the filter relaxes the noise requirement of the following stages in the receiver (Fig. 1(c)). In [24], our method to increase the order of band-pass N-path filters has been proposed. Here we will describe the exploited design methodology and filter properties, especially its transfer function and noise figure. Furthermore, practically achieved results are compared with theory and simulation. The outline of the paper is as follows: In section II, state-of-the-art N-path filters are discussed briefly. In section III, the proposed idea of an active N-path filter is illustrated and the design methodology is introduced. Moreover, a simple method to calculate the transfer function of conventional N-path filters is shown. In section IV, the design of a sixth-order BPF based on the proposed concept is demonstrated. In section V, we will show the realization and simulation results and in section VI, the measurement results will be shown. In the last section, conclusions will be drawn.

II. State-of-the-Art N-path Filters

Recently, there has been quite some research on N-path filters [2], [15]–[20], [25]–[27]. Although conventional N-path filters [17], [20] provide us with tunable high Q-factor BPFs, they suffer from: 1) harmonic folding; 2) limited stopband rejection due to the switch resistance, typically 15

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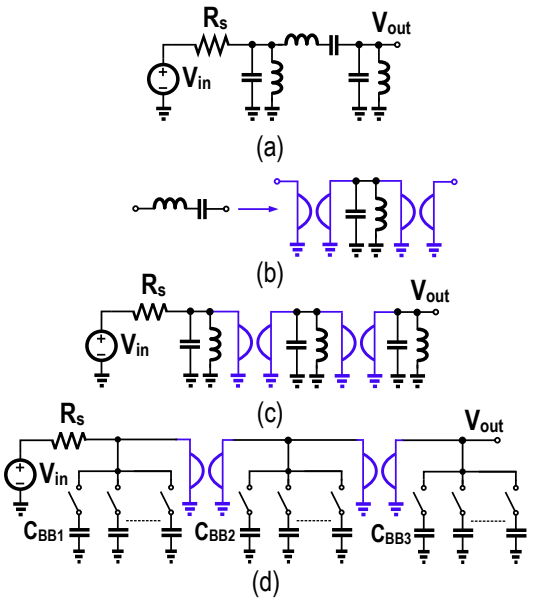

Fig. 2. (a) A 6th-order singly terminated LC BPF (b) Using two gyrators to synthesize a series LC tank by a parallel one (c) Substitution of the series LC tank by a parallel one (d) Substitution of all parallel LC tanks by their switched capacitor counterparts.

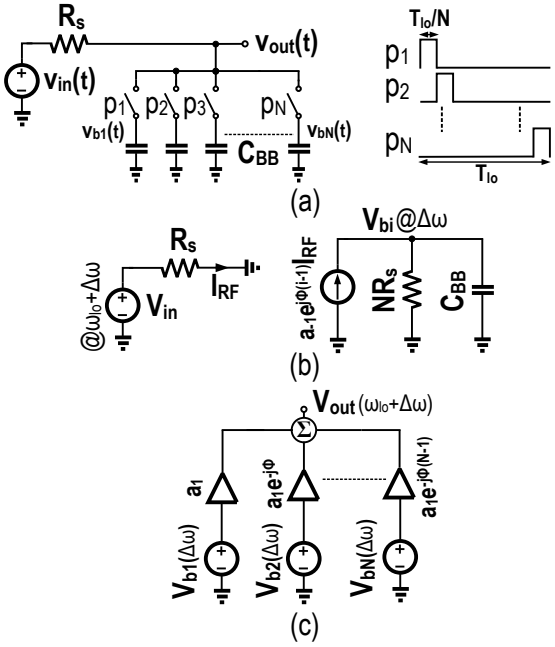

Fig. 3. (a) A general N-path filter with its required non-overlapping clocks (b) A circuit to simplify the calculation of the baseband voltages, V_{bi}, of the N-path filter and (c) Baseband signals, V_{bi} are upconverted to around ω_{lo} at node V_{out} due to the mixing operation of switches.

dB; and 3) poor filter shape. Due to the inherent mixing operation of the switches, it can be shown that signals located at $|kN-1|f_{lo}$ will fold-back into the desired signal located at f_{lo} where k $\in \mathbb{Z}$ and N is the number of phases (folding-back starts from $(N-1)f_{lo}$) [2], [16], [19], [20].

Therefore it is desirable to increase the number of phases in the filter. However, there are trade-offs among the maximum achievable frequency, folding-back issues and the dynamic power consumption. The limited stopband rejection and poor filter shape issues were tackled in [18]. Exploitation of a second set of switches fundamentally eliminates the effect of switch resistance on the ultimate rejection of the filter at the cost of doubling the dynamic power consumption and the additional noise of the second set of switches [16], [18]. Moreover in [16], [18], a novel method has been utilized to increase the order of the filter and obtain a flat passband shape. However, because the G_m cells in this filter architecture are used in baseband, the $1/f$ noise of the G_ms is upconverted to the center frequency of the filter. Therefore, the size of the baseband transistors should be quite large and lots of resistive degeneration is required to lower the NF of the filter. In this paper, we propose a filter architecture where the G_m cells are operating around the center frequency of the filter and therefore their $1/f$ noise performance is not critical and minimum channel length transistors can be utilized in the design of the G_m cells, easing process scaling.

III. High-Order Active N-Path Filters

An N-path filter can emulate an LC tank with a tunable center frequency and constant bandwidth [2], [16], [19]. Therefore, we conjecture that it should be possible to exploit this property to synthesize high-order BPFs. A singly-terminated 6th order LC BPF is illustrated in Fig. 2(a). Parallel LC tanks can be replaced by their N-path counterparts. Therefore, it is required to synthesize the series LC tank from a parallel one. The series LC tank can be synthesized using two gyrators as illustrated in Fig. 2(b). By substituting the series LC tank in Fig. 2(a) with its counterpart in Fig. 2(b), the filter shown in Fig. 2(c) will result. Now, we substitute each LC tank in the filter by its N-path counterpart and the filter is modified to the filter illustrated in Fig. 2(d). The analysis of the filter in Fig. 2(d) can become quite complex. In the following sections we will introduce a compact way to analyze N-path filters and design higher order active N-path filters. This provides both an analysis of the filter in Fig. 2(d), as well as a general design methodology starting with baseband filters that arrives at the same topology as Fig. 2(d).

A. Compact Analysis of Conventional N-path filters

Here, the transfer function of an N-path filter around its switching frequency is analyzed in an intuitive way, simpler than the methods used in [19], [20] where exhaustive analysis has been utilized. A conventional N-path filter with its required clock signals is depicted in Fig. 3(a). The clock signals, $p_i(t)$ $i = [1, N]$, are non-overlapping with a duty-cycle of 1/N. It is assumed that $R_s C_{BB} \gg T_{lo}$ [13] which means that the baseband voltages in Fig. 3(a),V_{bi} $i = [1, N]$, only contain low frequency (baseband) signals. For the time that $p_i(t)$ is high, the current through the source resistance is $[v_{in}(t) - v_{bi}(t)]/R_s$. This can be regarded as the superposition of two currents: an RF current that is caused by $v_{in}(t)$, and a baseband current caused by $v_{bi}(t)$. This allows us to find the baseband voltage of one path, V_{bi}, with the help of the equivalent circuit in

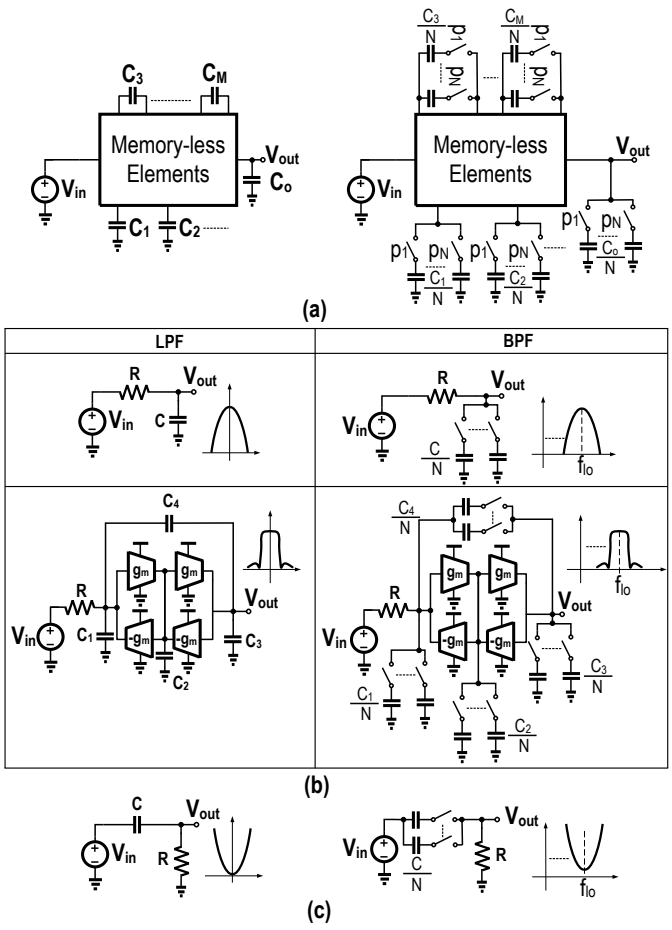

Fig. 4. (a) Illustration of the design methodology (b) Two examples of exploitation of the methodology (c) A case [27] where the methodology should be utilized indirectly.

Fig. 3(b) where the left part works at RF and the right part works at baseband. Firstly, the RF current, $v_{\text{in}}(t)/\text{R}_s$, will be converted to a baseband current due to the mixing operation of $p_i(t)$. Let us assume that the input signal is located at $\omega_{\text{lo}}+\Delta\omega$, $v_{\text{in}}(t)=\text{V}_{\text{in}}e^{j(\omega_{\text{lo}}+\Delta\omega)t}$. In this way, the magnitude of the effective baseband current that goes to the baseband capacitor due to the input voltage is $a_{-1}\text{e}^{j\phi(i-1)}\text{V}_{\text{in}}/\text{R}_s$ where $a_{-1}\text{e}^{j\phi(i-1)}$ is the first Fourier coefficient of $p_i(t)$ and ϕ is the phase difference between $p_1(t)$ and $p_2(t)$. Secondly, the baseband current $-\text{V}_{\text{b}i}/\text{R}_s$ is only present for 1/N$^{\text{th}}$ of the time, so its effect on the baseband voltage $\text{V}_{\text{b}i}$ can be modeled by a shunt resistance of NR_s. Therefore, $\text{V}_{\text{b}i}(j\Delta\omega)$ as a function of input voltage,$\text{V}_{\text{in}}(j(\omega_{\text{lo}}+\Delta\omega))$, will be:

$$\begin{aligned}\text{V}_{bi}(j\Delta\omega) &= a_{-1}e^{j\phi(i-1)}\text{I}_{\text{RF}}\times\frac{\text{NR}_s}{j\text{NR}_s\text{C}_{\text{BB}}\Delta\omega+1} \\ &= \text{N}a_{-1}e^{j\phi(i-1)}\text{G}(\Delta\omega)\text{V}_{\text{in}}(\omega_{\text{lo}}+\Delta\omega),\end{aligned} \tag{1}$$

where $\text{G}(j\Delta\omega)$ is

$$\text{G}(j\Delta\omega)=\frac{1}{j\text{NR}_s\text{C}_{\text{BB}}\Delta\omega+1}. \tag{2}$$

Next, we calculate the effect of the baseband voltages on V_{out}. Due to the transparency of the switches, the voltage of all the baseband nodes, V_{bi}, are upconverted from $\Delta\omega$ to around $\omega_{\text{lo}}+\Delta\omega$ at node V_{out} by the mixing operation of the clock signals. As shown in Fig. 3(c), the contribution of each path to the output node is $\text{V}_{bi}a_1e^{-j\phi(i-1)}$ which can be simplified to $\text{N}|a_1|^2\text{G}(j\Delta\omega)\text{V}_{\text{in}}(j(\omega_{\text{lo}}+\Delta\omega))$ using (1). These signals are added together to construct the output voltage as illustrated in Fig. 3(c). Interestingly, the contribution of all the paths are identical and therefore the output voltage $\text{V}_{\text{out}}(j(\omega_{\text{lo}}+\Delta\omega))$ will be N times the contribution of one path as described in (3).

$$\frac{\text{V}_{\text{out}}(j(\omega_{\text{lo}}+\Delta\omega))}{\text{V}_{\text{in}}(j(\omega_{\text{lo}}+\Delta\omega))}=\text{N}^2|a_1|^2\text{G}(j\Delta\omega)=\text{sinc}^2\left(\frac{\pi}{\text{N}}\right)\text{G}(j\Delta\omega) \tag{3}$$

The transfer function described in (2) is the transfer function of the N-path filter when the switched-capacitor section is substituted by a capacitor of NC_{BB}. Therefore in general, to find the transfer function of the filter: 1) substitute the switches and capacitors with a baseband equivalent capacitor of NC_{BB}; 2) calculate the transfer function of the filter, $\text{G}(s)$; 3) transform this transfer function to around ω_{lo} and 4) multiply the resultant transfer function by $\text{sinc}^2(\pi/\text{N})$. Interestingly, in N-path filters, the bandwidth and center frequency of the filter can be chosen independently. The bandwidth (Hz) of the filter is $1/(\text{N}\pi\text{R}_s\text{C}_{\text{BB}})$ and the Q-factor of the filter is $f_{\text{lo}}\text{N}\pi\text{R}_s\text{C}_{\text{BB}}$.

B. Design Methodology of Higher Order N-path Filters

In order to calculate the transfer function of a general active N-path filter, we need to make two observations: 1) the transfer function of LPTV (Linear Periodic Time Variant) circuits is the same at all the harmonics of the clock frequency (including the zeroth harmonic) except with a different scaling factor [13], [21]–[23], [28].[1] Therefore it is only needed to find the frequency response of the filter at low frequency and the transfer function of the filter around f_{lo}, will be a scaled version of that filter shape, $\text{sinc}^2(\pi/\text{N})$, transformed to f_{lo}, similar to the case described in subsection A. This holds only when the output node of the LPTV circuit is band-limited. If the circuit is not band-limited, it is not possible to neglect the contributions at f_{lo} caused by the filter transfer functions around higher harmonics of f_{lo}; 2) at very low frequencies, the phase difference between different paths of the filter is zero. Therefore the steady-state voltage on different capacitors of one N-path section would be the same and as a consequence, to find the transfer function of the filter, all the capacitors of one section can be connected together. Therefore, to find the transfer function of a general N-path filter at very low frequency, we substitute each switched-capacitor section of the filter with N times the baseband capacitor of that section and then calculate the transfer function of the resultant circuit. Afterwards, the transfer function of the filter around f_{lo}, is this transfer function which is transformed to around f_{lo} and scaled by scaling factor, $\text{sinc}^2(\pi/\text{N})$.

[1]If there is an interaction between the different phases of the N-path filter (e.g. [16]), the transfer function of the filter will not look the same at different harmonics of f_{lo}.

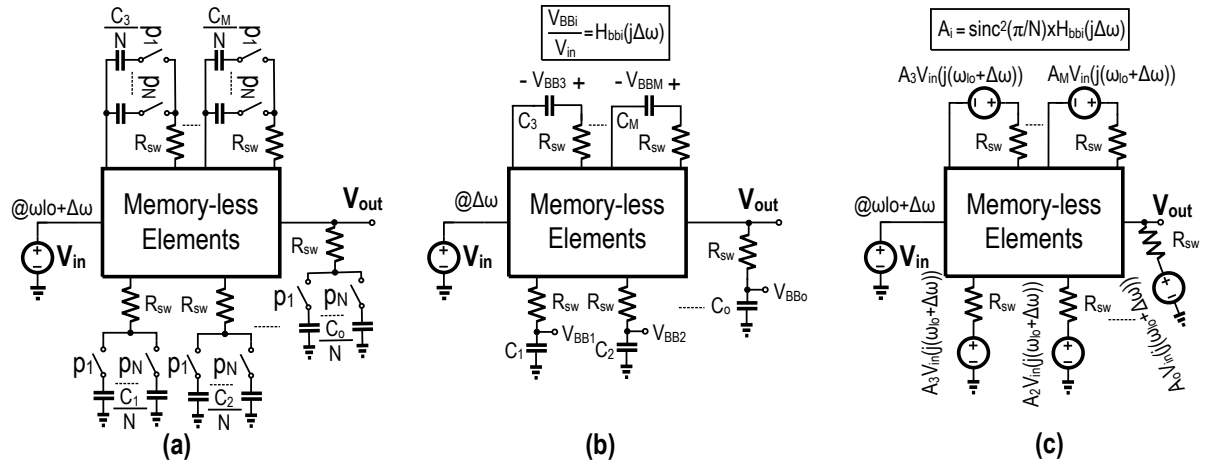

Fig. 5. (a) The effect of switch resistance, R_{sw}, on the transfer function of the filter (b) The LPF version of the N-path filter (c) the transfer function of the filter can be found as a superposition of the different voltage sources.

According to the above discussion, the design methodology is straightforward: 1) choose the desired G_m-C LPF[2] with half the bandwidth of the desired BPF; 2) substitute all the capacitors in the LPF by their N-phase switched-capacitor counterparts with baseband capacitance of 1/Nth of the ones used in the LPF counterpart. The design methodology is illustrated in Fig. 4(a). A few examples of this methodology are given in Fig. 4(b). One example where the methodology should be utilized indirectly is illustrated in Fig. 4(c) [27] due to the fact that its low-frequency counterpart is not band-limited. Of course in this case, if the voltage around the switched capacitor part is taken as output, the methodology can be exploited to find the transfer function there, T(s), and finally the actual output transfer function can be found by (1-T(s)). It should be noted that all the components inside the box in Fig. 4(a) should be memory-less. As it was discussed, all the baseband capacitors in the LPF counterpart should be converted to their switched-capacitor counterparts in the resultant N-path BPF. However, the parasitic capacitors introduced by active components to the internal nodes of the filter can not be converted to their switched-capacitor counterpart. This deviation in the synthesis can potentially distort the passband shape of the N-path BPF. The effect of parasitic capacitance on N-path filters is explored in subsection D and we will deal with this issue in section V. Finally, in contrast to LTI circuits, cascading two N-path filter sections does not necessarily result in the product of their individual gains, as shown in Appendix A.

C. The Effect of Switch Resistance on N-path Filters

In reality, the switches have a non-zero switch resistance and this potentially can modify the transfer function of the resultant filter (Fig. 5(a)). To find the effect of switch resistance on the frequency response of the filter, the LPF counterpart of the filter is illustrated in Fig. 5(b) (substitution of all the switched-capacitor sections by a capacitor of N times their baseband capacitance). Here, the transfer function of the filter from its input voltage source, $V_{in}(\Delta\omega)$ to every baseband voltage, $V_{bbi}(j\Delta\omega)$, $i = [1, M]$ is calculated, $H_{bbi}(j\Delta\omega)$, where M is the number of switched-capacitor sections of the BPF. Afterwards, each of these transfer functions will be transformed to around the clock frequency by a scaling factor, $A_i(j(\omega_{lo}+\Delta\omega)) = \text{sinc}^2(\pi/N) \times H_{bbi}(j\Delta\omega)$. Now, the total transfer function of the filter can be found by superposition as illustrated in Fig. 5(c). Therefore in general, a non-zero switch resistance: 1) modifies the poles of the filter; and 2) introduces some unwanted zeros into the transfer function of the filter (due to the superposition). For typical values of switch resistance, these unwanted zeros are far outside the passband of the filter. These zeros are responsible for the limited stopband rejection of the filter. In general, because the non-zero switch resistance reduces the quality factor of baseband capacitors, it reduces the Q-factor of the resultant filter.

D. The Effect of Parasitic Capacitance on N-path Filters

Because an N-path filter emulates an RLC tank, it is intuitively expected that the addition of parasitic capacitance at the input node of the filter only lowers the center frequency of the filter and does not introduce loss. However as will be shown here, it does introduce voltage loss. As we will see, if the input impedance of the filter is modeled by an RLC tank, the values of L and C are independent from the value of the parasitic capacitance. However, the resistive part of the RLC tank decreases as C_p increases. The transfer function of the filter shown in Fig. 6(a) around f_{lo} is [16], [25]:

$$H(j(\omega_{lo}+\Delta\omega)) = \frac{Y_s(j(\omega_{lo}+\Delta\omega))}{\frac{NC_{BB}j\Delta\omega}{\text{sinc}^2(\pi/N)} + \sum_{m=-\infty}^{+\infty} \frac{Y_s(j(Nm+1)\omega_{lo})}{(1+mN)^2}}. \quad (4)$$

If the series in the denominator of (4) is called Y_{eff} [16], then Y_{in} in Fig. 6(a) will be:

[2]Any types of LPF such as op-amp RC can be used, however because the active devices should operate at high frequencies, G_m-C is preferred over the other types of LPF.

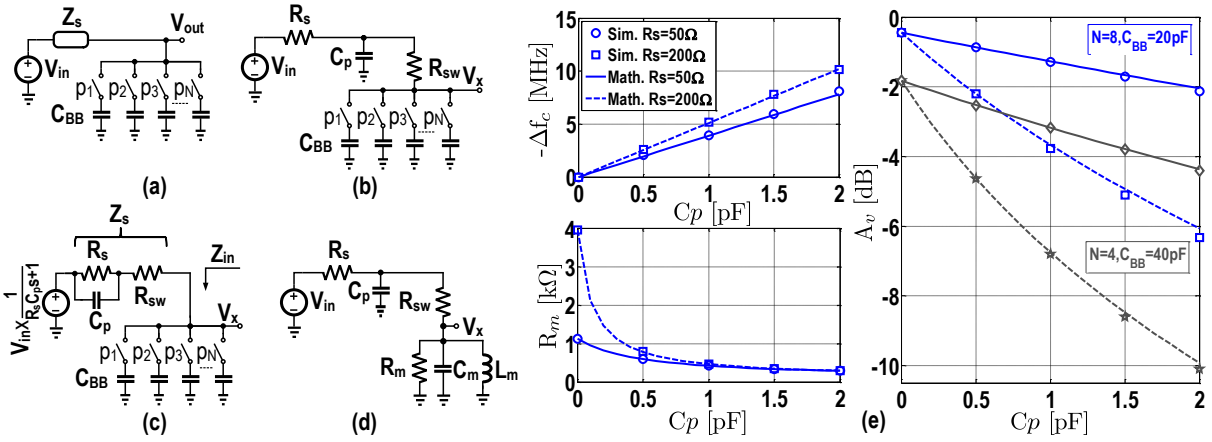

Fig. 6. (a) An N-path filter with general source impedance (b) The effect of parasitic capacitance C_p on N-path filter (c) Making the model compatible with part (a) (d) The effect of parasitic capacitance on the input impedance of N-path filter (e) The effect of parasitic capacitance on N-path filters: change in the center frequency of the filter Δf_c, input impedance at center frequency of the filter R_m, and voltage gain A_v for two different values of source resistance, $R_s = 50\ \Omega$ and $200\ \Omega$ as a function of parasitic capacitance C_p; $f_{lo} = 1$ GHz, $R_{sw} = 10\ \Omega$, $C_{BB} = 20$ pF and $N = 8$; Also, the effect of parasitic capacitance on voltage gain of filter is shown for $N = 4$ and 8.

$$\mathrm{Y_{in}} = \mathrm{Re}(\mathrm{Y_{eff}}) - \mathrm{Re}(\mathrm{Y}_s) + j \times \left(\frac{\mathrm{NC_{BB}}\Delta\omega}{\mathrm{sinc}^2(\pi/\mathrm{N})} + \mathrm{Im}(\mathrm{Y_{eff}}) - \mathrm{Im}(\mathrm{Y}_s) \right). \tag{5}$$

Now by exploiting (4-5), the effect of parasitic capacitance on the performance of the N-path filter is investigated (Fig. 6(b)). The N-path filter illustrated in Fig. 6(b) is converted to the circuit shown in Fig. 6(c) to be compatible with Fig. 6(a). In this case, $\mathrm{Y}_s(s)$ is $1/(\mathrm{R}_s + \mathrm{R}_{sw}) \times (\mathrm{R}_s\mathrm{C}_p s + 1)/(\mathrm{R}_s||\mathrm{R}_{sw}\mathrm{C}_p s + 1)$. Consequently, the transfer function of the circuit in Fig. 6(c) from $\mathrm{V_{in}}$ to V_x can be found by:

$$\mathrm{H}(j(\omega_{\mathrm{lo}} + \Delta\omega)) = \frac{1}{j\mathrm{R}_s||\mathrm{R}_{sw}\mathrm{C_p}\omega_{\mathrm{lo}} + 1} \times \frac{1}{\mathrm{R}_s + \mathrm{R}_{sw}} \times \frac{1}{j\left(\frac{\mathrm{NC_{BB}}\Delta\omega}{\mathrm{sinc}^2(\frac{\pi}{\mathrm{N}})} + \mathrm{Y_i}\right) + \mathrm{Y_r}}, \tag{6}$$

where $\mathrm{Y_r}$ and $\mathrm{Y_i}$ are (7) and (8), respectively.

$$\mathrm{Y_r} = \frac{1}{\mathrm{R}_s + \mathrm{R}_{sw}} \times \sum_{n=-\infty}^{+\infty} \frac{1 + (1+n\mathrm{N})^2(\mathrm{R}_s||\mathrm{R}_{sw})\mathrm{R}_s\mathrm{C_p}^2\omega_{\mathrm{lo}}^2}{(1+n\mathrm{N})^2[1 + (1+n\mathrm{N})^2(\mathrm{R}_s||\mathrm{R}_{sw})^2\mathrm{C_p}^2\omega_{\mathrm{lo}}^2]} \tag{7}$$

$$\mathrm{Y_i} = \frac{1}{\mathrm{R}_s + \mathrm{R}_{sw}} \times \sum_{n=-\infty}^{+\infty} \frac{(\mathrm{R}_s - \mathrm{R}_{sw}||\mathrm{R}_s)\mathrm{C}_p\omega_{\mathrm{lo}}}{(1+n\mathrm{N})[1 + (1+n\mathrm{N})^2(\mathrm{R}_s||\mathrm{R}_{sw})^2\mathrm{C}_p^2\omega_{\mathrm{lo}}^2]} \tag{8}$$

As can be deduced from (6), the center frequency of the filter (9) shifts to the lower frequency.

$$\omega_c = \omega_{\mathrm{lo}} - \frac{\mathrm{Y_i} \times \mathrm{sinc}^2(\frac{\pi}{\mathrm{N}})}{\mathrm{NC_{BB}}} \tag{9}$$

$$|\mathrm{H}(j\omega_c)| = \frac{1}{(\mathrm{R}_s + \mathrm{R}_{sw}) \times \mathrm{Re} \times \sqrt{(\mathrm{R}_s||\mathrm{R}_{sw})^2\mathrm{C}_p^2\omega_{\mathrm{lo}}^2 + 1}} \tag{10}$$

The input impedance of the filter can be modeled by an RLC tank (Fig. 6(d)) where:

$$\frac{1}{\mathrm{R}_m} = \mathrm{Y_r} - \frac{1}{\mathrm{R}_s + \mathrm{R}_{sw}} \frac{1 + (\mathrm{R}_s||\mathrm{R}_{sw})\mathrm{R}_s\mathrm{C}_p^2\omega_{\mathrm{lo}}^2}{1 + (\mathrm{R}_s||\mathrm{R}_{sw})^2\mathrm{C}_p^2\omega_{\mathrm{lo}}^2}, \tag{11}$$

$$\mathrm{C}_m = \frac{\mathrm{NC_{BB}}}{2\mathrm{sinc}^2(\pi/\mathrm{N})}, \ \mathrm{L}_m = \frac{1}{\mathrm{C}_m \times \omega_{\mathrm{lo}}^2}. \tag{12}$$

Therefore the only thing that is modified by parasitic capacitance is the tank's resistance R_m which reduces as C_p increases and this stands for the raise in the loss of the filter. The effect of parasitic capacitance on change of the center frequency (9), and the impedance of the filter at its center frequency (11) for two different values of source resistance, $\mathrm{R}_s = 50\ \Omega$ and $200\ \Omega$, $f_{\mathrm{lo}} = 1$ GHz, $\mathrm{R}_{sw} = 10\ \Omega$, $\mathrm{C_{BB}} = 20$ pF and $\mathrm{N} = 8$ is shown in Fig. 6(e).

Moreover, the effect of input parasitic capacitance on the voltage gain of the N-path filter for two different number of phases, $\mathrm{N} = 4$ and 8, is illustrated in Fig. 6(e). As can be seen, the effect of parasitic capacitance is much more pronounced in the case of lower number of phases and higher values of source resistance. This effect can be explained intuitively. Every time a switch is on, there is a charge sharing between the baseband capacitor and the parasitic capacitor, leading to energy loss and hence lowering the gain of filter. This effect can be mitigated by lowering the harmonic content of the filter by increasing the number of phases.[3] The effect of parasitic capacitance on an active N-path filter can be deduced from the above discussion:

[3]Please note that increasing the number of phases also increases the parasitic capacitance of the switches. Therefore, in a case where the parasitic capacitance of the switches is the main contributor, increasing the number of phases is not quite beneficial.

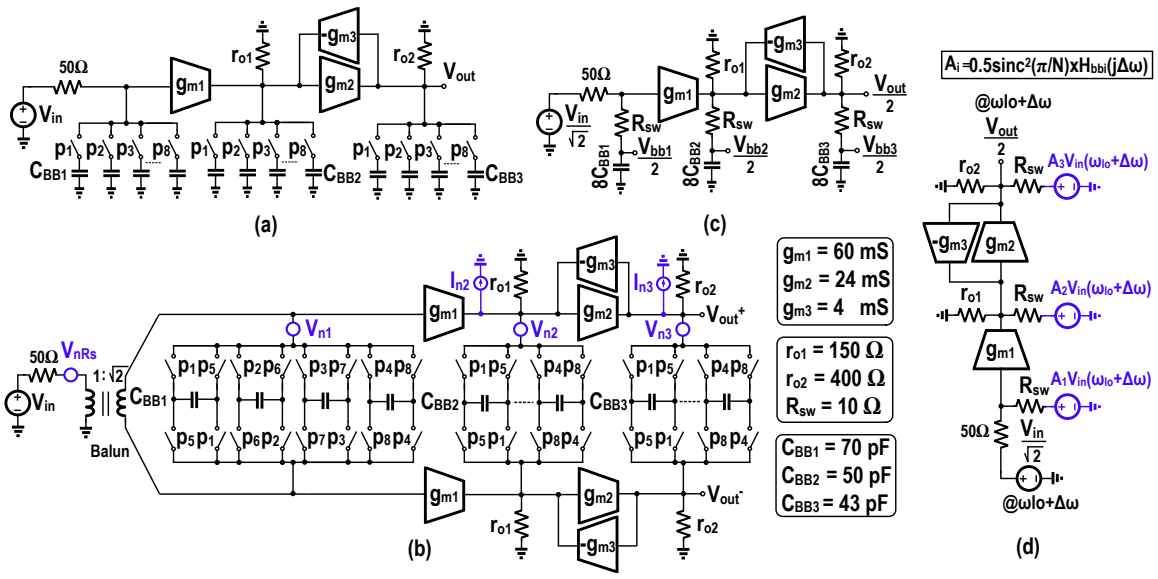

Fig. 7. (a) Proposed 6th order N-path BPF (b) Using differential circuit to be resilient to common mode noise and utilization of differential clocking scheme to eliminate the gain of the filter at DC and even harmonics of the clock frequency (c) The LPF counterpart of the filter to be used in the design process (d) Using the technique proposed in section III to calculate the effect of switch resistance on the transfer function of the filter.

1) it lowers the effective impedance of the internal nodes of the filter and consequently de-Qs the filter shape; 2) due to the reduction of the center frequency of switched-capacitor sections, it introduces an extra phase shift to each node of the filter which potentially can lead to an unwanted peaking in the passband shape of the filter. These effects are exacerbated as the switching frequency increases.

IV. Design of the Proposed Filter

To reduce the number of active components and hence lowering the power consumption and increase the dynamic range of the filter, the first gyrator in the proposed filter (Fig. 2(d)) is substituted by a single G_m cell. In this way, the filter can be seen as stagger tuning a 2^{nd} and a 4^{th} order BPF (Fig. 7(a)). The gyrator is realized using two G_m cells. In contrast to conventional gyrator design, two different values have been assigned to the feedforward and return G_ms of the gyrator. As we will see later, the noise contribution of the gyrator will be lowered and at the same time a decent amount of gain can be achieved. We chose 8 phases in our design. As discussed previously, increasing the number of phases is beneficial in reducing the folding-back issues and hence decreasing the NF of the filter (less noise-folding from higher harmonics of f_{lo}) and lowering the spurs. However, there are tradeoffs among folding-back, maximum achievable frequency and dynamic power consumption. A differential structure is exploited to combat common-mode disturbance. To eliminate bandpass filtering at even harmonics of the clock frequency, a differential clocking scheme is utilized (Fig. 7(b)). In this way, the even Fourier coefficients of the effective clock signals are zero and hence there is no gain at DC and other even harmonics of the filter. To save area, capacitors are made differential.

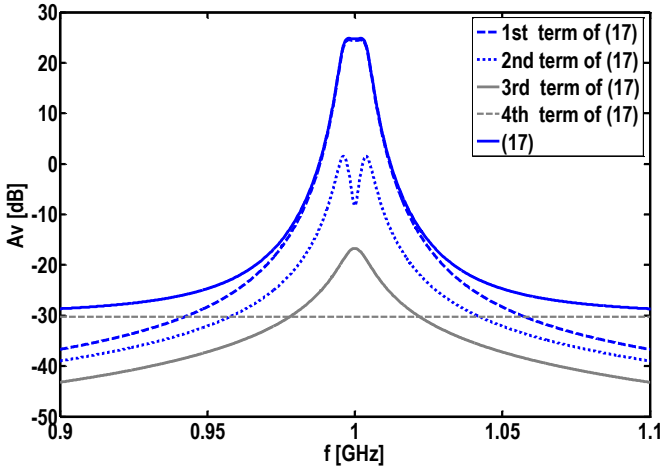

Fig. 8. The impact of different terms of (17) on the total transfer function of the filter; the 1^{st} term is dominant in the passband and the 4^{th} term determines the ultimate-rejection of the filter.

A. Transfer Function of the Filter

As discussed in the design methodology, by substituting each switched-capacitor section with an equivalent baseband capacitance of NC_{BBi}, the single-ended LPF counterpart of the filter shown in Fig. 7(c) will result. Transfer function of this filter by assuming $R_{sw} = 0\ \Omega$ is described by:

$$H_{LPF}(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{H_0}{(1 + s/p_1)(as^2 + bs + 1)} \qquad (13)$$

where

$$H_0 = \frac{\sqrt{2} g_{m1} g_{m2}}{D} \qquad (14)$$

$$\mathrm{p}_1 = \frac{1}{8\mathrm{C}_{\mathrm{BB1}}\mathrm{R}_s},\ \mathrm{a} = \frac{8^2\mathrm{C}_{\mathrm{BB2}}\mathrm{C}_{\mathrm{BB3}}}{\mathrm{D}}$$
$$\mathrm{b} = \frac{8}{\mathrm{D}}\left(\mathrm{C}_{\mathrm{BB3}}g_{\mathrm{o1}} + \mathrm{C}_{\mathrm{BB2}}g_{\mathrm{o2}}\right). \quad (15)$$

and D is $g_{\mathrm{m2}}g_{m3} + g_{\mathrm{o1}}g_{\mathrm{o2}}$. Because $g_{\mathrm{m2}}g_{\mathrm{m3}}r_{\mathrm{o1}}r_{\mathrm{o2}} \gg 1$, (14) can be simplified to $\mathrm{H}_0 = \sqrt{2}g_{\mathrm{m1}}/g_{\mathrm{m3}}$. The g_{m1} is chosen to be 60 mS to obtain a NF lower than 3 dB. The g_{m3} is 4 mS which leads to a voltage gain of 25.5 dB. Consequently, as discussed in section III, the total transfer function of the filter will be the scaled version of (13) which is translated to around f_{lo}.

$$\mathrm{H}(j(\omega_{\mathrm{lo}} + \Delta\omega)) = \mathrm{sinc}^2(\pi/\mathrm{N}) \times \mathrm{H}_{\mathrm{LPF}}(j\Delta\omega) \quad (16)$$

The effect of switch resistance on the transfer function of the filter can be found using the technique described in section III C. In Fig. 7(c), the transfer functions from the input voltage to the baseband voltages $\mathrm{V}_{\mathrm{bb}i}$ are calculated ($\mathrm{H}_{\mathrm{bb}i}(s)$). To find the total transfer function of the filter, each baseband capacitor is replaced by its equivalent voltage source as shown in Fig. 7(d) [i.e., $0.5\mathrm{sinc}^2(\pi/\mathrm{N})\mathrm{H}_{\mathrm{bb}i}(j\Delta\omega)V_{\mathrm{in}}(j(\omega_{\mathrm{lo}} + \Delta\omega))$]. Afterwards, the total transfer function of the filter around f_{lo} can be found by superposition.

$$\mathrm{H}(j(\omega_{\mathrm{lo}} + \Delta\omega)) = \frac{\sqrt{2}\mathrm{sinc}^2(\frac{\pi}{8})}{1 + \mathrm{D} \times \mathrm{R}_{sw}^2 + (g_{\mathrm{o1}} + g_{\mathrm{o2}})\mathrm{R}_{sw}} \times \Big[(1 + \mathrm{R}_{sw}g_{o1})\mathrm{H}_{\mathrm{bb3}}(j\Delta\omega) - g_{\mathrm{m2}}\mathrm{R}_{sw}\mathrm{H}_{\mathrm{bb2}}(j\Delta\omega) + g_{\mathrm{m1}}g_{\mathrm{m2}}\mathrm{R}_{sw}^2\mathrm{H}_{\mathrm{bb1}}(j\Delta\omega) + \frac{g_{\mathrm{m1}}g_{\mathrm{m2}}\mathrm{R}_{sw}^3}{\mathrm{sinc}^2(\frac{\pi}{8})(\mathrm{R}_{sw} + \mathrm{R}_s)}\Big] \quad (17)$$

where

$$\mathrm{H}_{\mathrm{bb3}}(s) = \frac{g_{\mathrm{m1}}g_{\mathrm{m2}}(1 + 8\mathrm{C}_{\mathrm{BB1}}\mathrm{R}_{sw}s)(1 + 8\mathrm{C}_{\mathrm{BB2}}\mathrm{R}_{sw}s)}{\mathrm{D}[1 + 8\mathrm{C}_{\mathrm{BB1}}(\mathrm{R}_{sw} + \mathrm{R}_s)s]\,(\mathrm{A}s^2 + \mathrm{B}s + 1)}$$
$$\mathrm{H}_{\mathrm{bb2}}(s) = \frac{-g_{\mathrm{m1}}(1 + 8\mathrm{C}_{\mathrm{BB1}}\mathrm{R}_{sw}s)[g_{\mathrm{o2}} + 8\mathrm{C}_{\mathrm{BB3}}s(1 + g_{\mathrm{o2}}\mathrm{R}_{sw})]}{\mathrm{D}[1 + 8\mathrm{C}_{\mathrm{BB1}}(\mathrm{R}_{sw} + \mathrm{R}_s)s](\mathrm{A}s^2 + \mathrm{B}s + 1)}$$
$$\mathrm{H}_{\mathrm{bb1}}(s) = \frac{1}{1 + 8\mathrm{C}_{\mathrm{BB1}}(\mathrm{R}_{sw} + \mathrm{R}_s)s} \quad (18)$$

$$\mathrm{A} = \mathrm{a} \times [1 + (g_{o1} + g_{o2})\mathrm{R}_{sw} + \mathrm{D} \times \mathrm{R}_{sw}^2], \quad (19)$$

$$\mathrm{B} = \mathrm{b} + 8\left(\mathrm{C}_{\mathrm{BB2}} + \mathrm{C}_{\mathrm{BB3}}\right)\mathrm{R}_{sw}. \quad (20)$$

For low values of switch resistance, to a very good approximation, only the first term between the square brackets in (17) determines the passband shape of the filter. The other remaining terms, merely modify the stopband shape of the filter. It should be noted that (17) will shrink to (16) for $\mathrm{R}_{sw} = 0\ \Omega$. The impact of different terms of (17) on the total transfer function of the filter is shown in Fig. 8 and as discussed, the dominant contributor in the passband is the first term of (17) and the other remaining terms are just responsible for the modification in stopband shape of the filter.

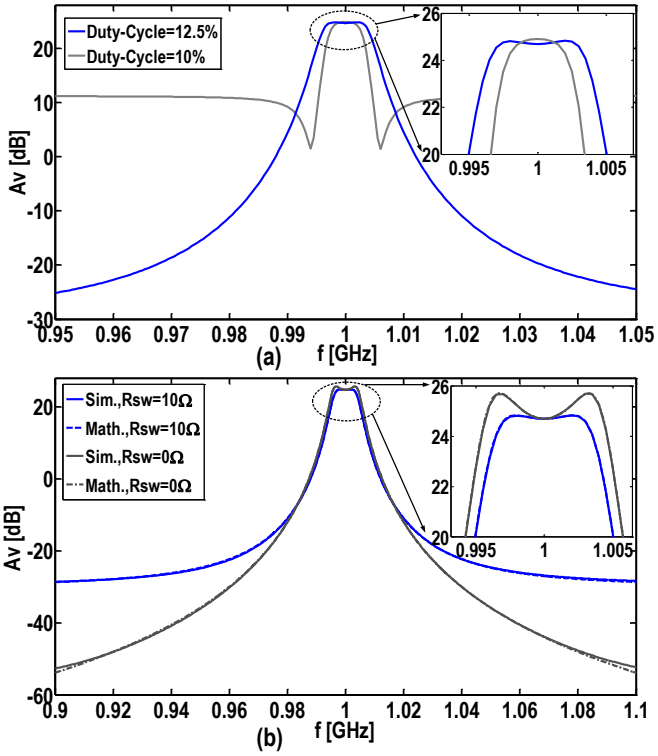

Fig. 9. (a) The simulated transfer function of the filter for $\mathrm{R}_{sw} = 10\ \Omega$ and duty-cycle of 10 % and 12.5 % b) A comparison between simulation and mathematical derivation (17) for R_{sw} of 0 Ω and 10 Ω.

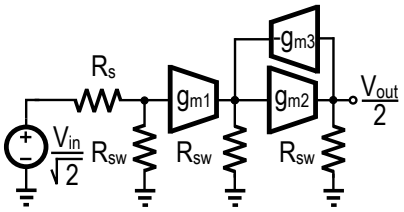

Fig. 10. A simplified schematic of the filter to calculate the stopband gain of the filter; The baseband capacitors are shorted to ground for frequencies far from the passband of the filter and $\sqrt{2}$ is the voltage gain of the BALUN.

Now based on (17), we design a center frequency tunable BPF with bandwidth of 9 MHz. The values of capacitors and G_{m} cells are shown in Fig. 7. In transistor-level implementation, relatively high value of g_{m1} leads to low r_{o1}. In the actual realization, two negative resistors have been added to the internal nodes of the filter (see section V) to increase and control r_{o1} and r_{o2}. Because it is not desirable to use large amount of negative admittance (reduction in DR and increase in P_{DC}), a value of 150 Ω and 400 Ω are chosen for r_{o1} and r_{o2}, respectively. Although exploiting higher values of $\mathrm{r}_{\mathrm{o1,2}}$ reduces the required value of baseband capacitance for a certain bandwidth, it amplifies the effect of parasitic capacitances because the associated decrease in R_{m} (see Fig. 6) is relatively stronger. In general, the non-

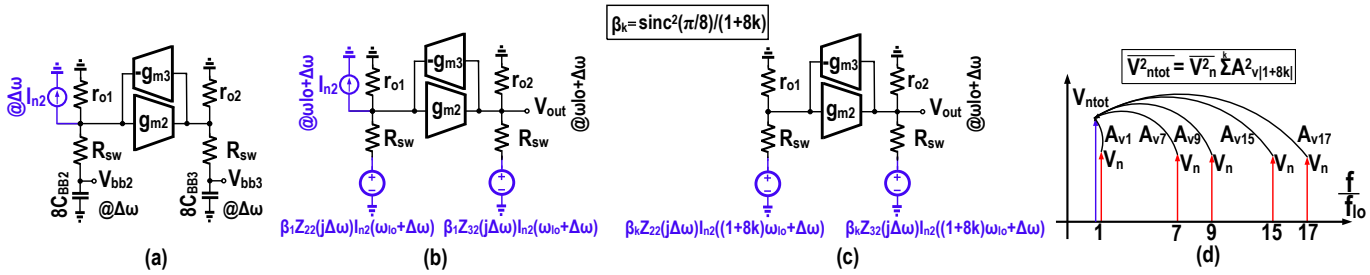

Fig. 11. (a) The low-pass counterpart of the filter to find the transfer function of $I_{n2}(j\Delta\omega)$ to the baseband voltages $V_{bb2,3}(j\Delta\omega)$ (b) Calculation of $V_{out}(j(\omega_{lo}+\Delta\omega))/I_{n2}(j(\omega_{lo}+\Delta\omega))$ by superposition (c) Calculation of $V_{out}(j(\omega_{lo}+\Delta\omega))/I_{n2}(j((8k+1)\omega_{lo}+\Delta\omega))$ by superposition $k\neq 0$ (d) Folding-back of noises located at $|1+8k|f_{lo}$ to f_{lo}.

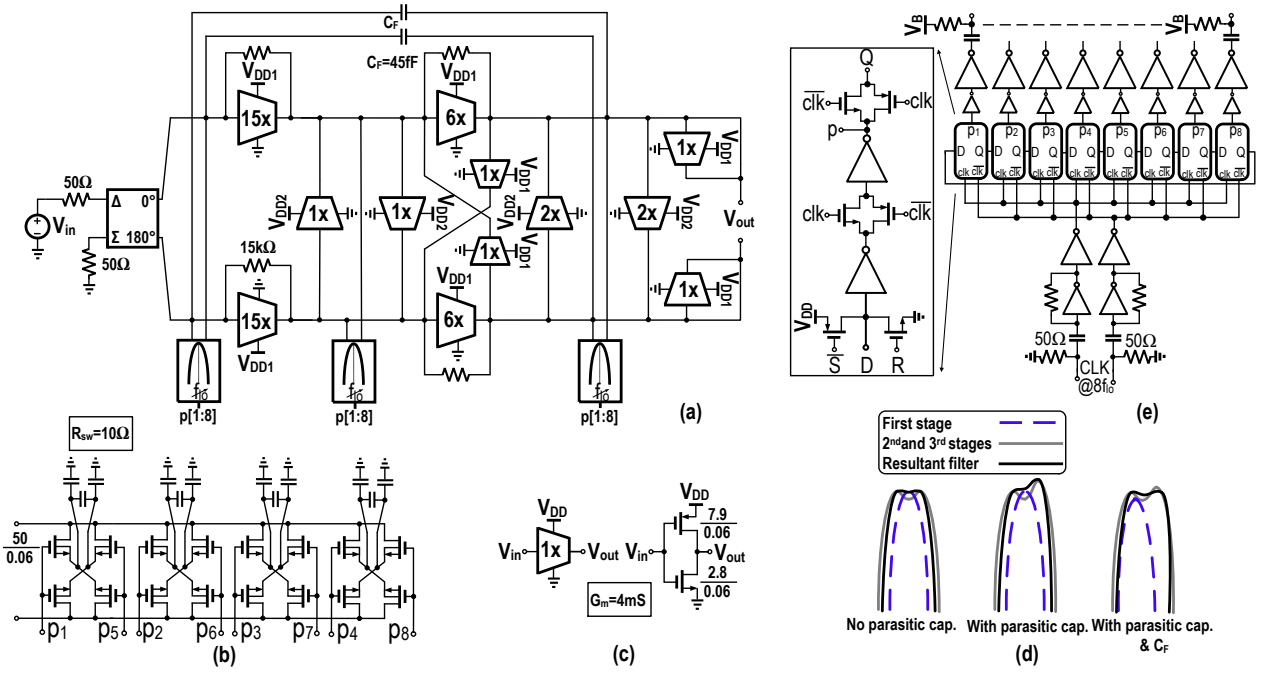

Fig. 12. (a) The transistor level schematic of the filter (b) Implementation of the switches and baseband capacitors (c) The unit G_m cell that is used in the filter with different scaling factors (d) An intuitive explanation of the operation of the proposed Miller-compensation method. (e) Obtaining 8 non-overlapping clocks by utilization of a modulo-8 counter; D flip-flops are implemented using transmission gates.

zero switch resistance lowers the Q-factor of the filter. The simulated transfer function of the filter with component values shown in Fig. 7 is illustrated in Fig. 9(a). Moreover, the effect of 2.5% reduction in the duty-cycle of the clocks is shown in Fig. 9(a) which is a reduction in the stopband rejection of the filter and reduction in the bandwidth of the filter. (The baseband capacitors see their equivalent resistance for a smaller amount of time.) In fact, because there are N time-slots with width of $T_{lo}\,(D_{ideal}-D_{real})$, the gain difference between passband and stopband will be $\text{sinc}^2(\frac{\pi}{N})/[N\,(D_{ideal}-D_{real})]$ for $D_{ideal}>D_{real}$ which in our case is 14 dB (Fig. 9(a)).[4] For perfect duty cycles, the stopband rejection, A_{sb}, (the difference between the passband and stopband voltage gain) of the filter can be found using the simplified circuit shown in Fig. 10 and it is described in (21). For the values used in our design, the stopband rejection is 56 dB. A technique to eliminate the effect of switch-resistance on the ultimate rejection of the filter is discussed in Appendix B.

$$\frac{1}{A_{sb}}=\text{sinc}^2\left(\frac{\pi}{8}\right)\times\left(1+\frac{1}{R_{sw}^2 g_{m2}g_{m3}}\right)\times\left(1+\frac{R_s}{R_{sw}}\right) \quad (21)$$

The simulated transfer function of the filter is compared with its mathematical derivation (17) in Fig. 9(b) for two different values of switch resistance (0 Ω and 10 Ω) and as can be seen they match very well. As can be seen, non-zero switch resistance lowers the Q-factor of the filter.

B. NF of the Filter

Here, the noise performance of the filter is analyzed. At first, it is required to find the transfer function of different noise sources to the output node of the filter (Fig. 7(b)). $V_{n1,2,3}$ represent the switch resistance noise of different sections

[4]In reality, by correct choice of the DC bias voltage of the gate of switches and the rise and fall time of the clock signals (typically in the range of $10-20$ ps), we can be sure that always one of the switches is on.

and $\mathrm{I_{n2,3}}$ represent the noise contribution of the $\mathrm{G_m}$ cells and the r_{o1} and r_{o2} on each node. The same technique that is illustrated in Fig. 5 can be exploited here. The only difference here is that for the input signals (e.g., noise sources) located at $(1+kN)f_{lo}$, the baseband signals are scaled by $\beta_k = \mathrm{N}^2|a_1 a_{(-1-k\mathrm{N})}| = \mathrm{sinc}^2(\pi/\mathrm{N})/(1+k\mathrm{N})$. The input signals located at $(1+k\mathrm{N})f_{lo}$ are downconverted to the baseband signals by the mixing operation of the switches with gain of $\mathrm{N}|a_{(-1-k\mathrm{N})}|$ and then these downconverted signals are upconverted to f_{lo} by the mixing operation of the switches with gain of $\mathrm{N}|a_1|$. As an example, Fig. 11 shows how to find the total noise contribution of $\mathrm{I_{n2}}$ to the output voltage. Using the equivalent LPF counterpart of the filter (Fig. 11(a)), the baseband transfer functions $\mathrm{Z_{i2}}(s) = \mathrm{V_{bbi}}(s)/\mathrm{I_{n2}}(s)$ where $i = 2, 3$ are found. Subsequently, as depicted in Fig. 11(b) and 11(c), after substituting each switched-capacitor section with its equivalent voltage source, $\mathrm{V_{out}}(\omega_{lo}+\Delta\omega)/\mathrm{I_{n2}}((1+8k)\omega_{lo}+\Delta\omega)$ can be found using superposition where $k \in \mathbb{Z}$. If $\mathrm{R}_{sw} \ll r_{o1}, r_{o2}$ and $g_{m2}g_{m3}r_{o1}r_{o2} \gg 1$ and $g_{m2}g_{m3}\mathrm{R}_{sw}^2 \ll 1$, it can be shown that:

$$\frac{\mathrm{V_{out}}(\omega_{lo})}{\mathrm{I_{n2}}((1+8k)\omega_{lo})} \simeq \frac{\beta_k}{g_{m3}}. \tag{22}$$

Now, the total noise contribution due to $\mathrm{I_{n2}}$ can be calculated with the help of Fig. 11(d). Therefore, the noise excess factor due to $\mathrm{I_{n2}}$ will be approximately $\overline{\mathrm{I_{n2}^2}}/4k\mathrm{T}\mathrm{R}_s g_{m1}^2\beta_1$. By exploiting the same procedure, the noise contribution of different noise sources to the output node can be found. It can be shown that the NF of the filter at its center frequency can be found by (by applying the previous assumptions):

$$\begin{aligned}\mathrm{F} \simeq \underbrace{\beta_1^{-1}}_{\mathrm{R}_s} + \underbrace{\beta_1^{-1}\left(\beta_1^{-1}-1\right)\frac{\mathrm{R}_{sw}}{\mathrm{R}_s}\left(\frac{g_{m3}}{g_{m1}}\right)^2}_{\mathrm{R}_{sw}} + \underbrace{\frac{\beta_1^{-1}}{g_{m1}\mathrm{R}_s}}_{g_{m1}} + \underbrace{\frac{\beta_1^{-1}g_{m3}}{g_{m1}^2\mathrm{R}_s}}_{g_{m3}} \\ + \underbrace{\frac{\beta_1^{-1}g_{m,neg1}}{g_{m1}^2\mathrm{R}_s}}_{g_{m,neg1}} + \underbrace{\frac{1}{r_{o1}^2 g_{m2}g_{m1}^2\mathrm{R}_s}}_{g_{m2}} + \underbrace{\frac{g_{m,neg2}}{r_{o1}^2 g_{m2}^2 g_{m1}^2\mathrm{R}_s}}_{g_{m,neg2}}.\end{aligned} \tag{23}$$

where $g_{m,neg1,2}$ are the $\mathrm{G_m}$ cells added to the internal nodes of the filter to control $r_{o1,2}$. Interestingly, it can be shown that the transfer functions from $\mathrm{V_{n1,2,3}}$ to the output of the filter have a bandstop shape and therefore the noise contribution of switches is relatively suppressed at the center frequency of the filter. An exact derivation of the NF is introduced in Appendix C.

V. Realization

The filter was realized in CMOS LP 65 nm technology. The schematic of the proposed filter is illustrated in Fig. 12(a). As discussed in section III, in the methodology, it is assumed that all the components except the baseband capacitors are memory-less elements. However, in reality this is not the case and $\mathrm{G_m}$ cells and switches contribute a large amount of parasitic capacitance to the internal nodes of the filter. These parasitic capacitances and their associated extra phase shifts

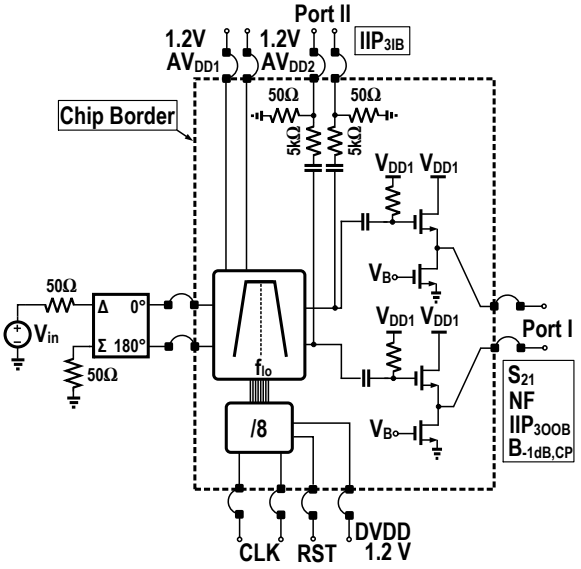

Fig. 13. On-chip measurement interface of the proposed filter.

(In section III, it was shown that besides introducing loss, the parasitic capacitance lowers the effective center frequency of the filter which is equivalent to extra phase shift) can potentially distort the passband shape of the filter. This is the same phenomenon that also occurs in bandpass $\mathrm{G_m}$-C filters [10]. In this work, our aim was to alleviate this issue with minimum additional components.

A simple yet effective way to attain this purpose is to use a Miller compensation method, by including $\mathrm{C_F}$, as shown in Fig. 12. It is possible here due to the uni-lateralization made by $\mathrm{G_{m1}}$ and having a decent amount of gain in the filter. The intuitive explanation is given in Fig 12(d). Two effects are involved in the operation of the Miller compensation: 1) it reduces the effect of parasitic capacitors on the output node of the filter due to its bandwidth enhancement effect at output node of the filter and hence leads to reduction of the passband ripple of the 4^{th} order section; 2) it reduces the center frequency of the 2^{nd} order section and hence the peaking part will see less gain and eventually this leads to the elimination of the peaking in the passband shape of the resultant filter (see subsection A). Each switch in the filter (Fig. 12(b)) is sized (W/L= 50μm/60nm) to obtain an on resistance of around 10 Ω. Each NMOS switch is in a separate p-well with its bulk and source tied together, avoiding an increase in the threshold voltage of the transistor.[5] Large switches are used to reduce their noise, nonlinearity, mismatch between them and to increase the stopband rejection of the filter. Nevertheless, increasing the size of the switches will introduce more parasitic capacitance to the filter nodes which can lead to distortion of the passband shape of the filter. Moreover, large switch transistors increase the dynamic power consumption and the LO leakage to the input port of the filter. Because the drain and source of each switch have a DC bias of 0.6

[5]The parasitic capacitance of the well is in parallel with the baseband capacitors and therefore it is not important.

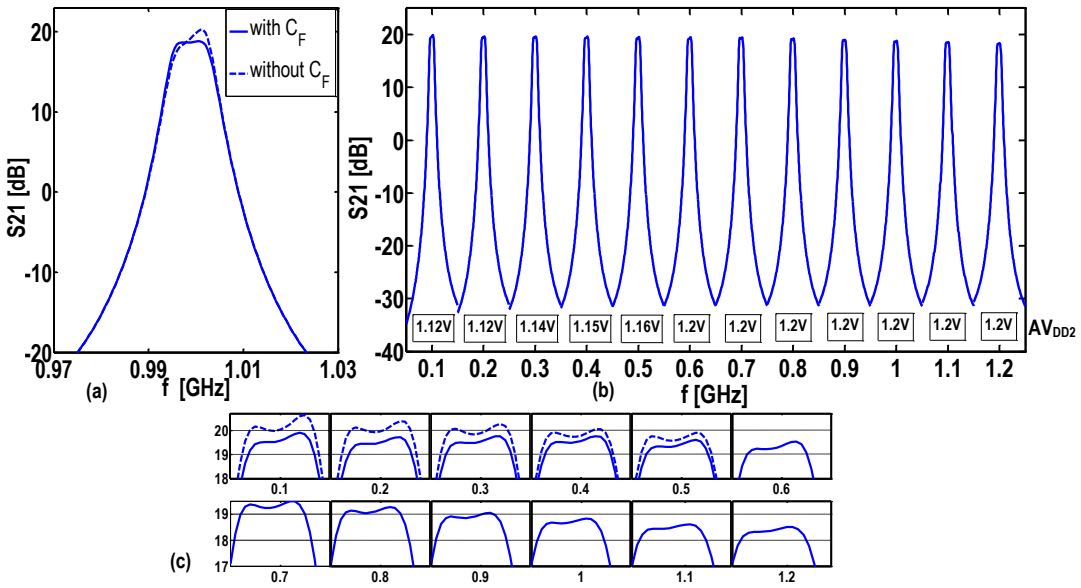

Fig. 14. (a) The simulated transfer function of the filter with and without additional feedback capacitors C_F (b) The simulated transfer function of the filter in the whole tuning range; The utilized value of the separate supply voltage AV_{DD2} is also depicted for each clock frequency. Nominal AV_{DD2} is 1.2 V. (c) The passband details of the filter in the whole tuning range; Also the passband shape of the filter in the case of fixed AV_{DD2} is shown for comparison (the dashed ones).

V (V_{DD}/2), for proper operation (high linearity and low on resistance) of the switches, the low and high levels of the clock signals should be raised by 0.6 V. The clock signals are ac-coupled to the gate of each switch which has a high ohmic resistor to a bias voltage of 0.75 V ($5V_{DD}/8$). The ac-coupling capacitors are sized large enough to minimize the voltage loss due to the capacitive voltage division between the ac-coupling capacitor and the gate capacitance of the switches.[6] The baseband capacitors are realized by a combination of accumulation-mode NMOS and MOM capacitors.

All the G_m cells are based on a self-biased inverter [11] unit-cell (Fig. 12(c)) using minimum channel-length transistors with different scaling factors. Inverter-based G_m cells can achieve a very low 2nd order harmonic distortion citeBram. This feature and the differential nature of the circuit together, lead to a low 2nd order distortion which is limited by the mismatch. To reduce the parasitic capacitance of the G_ms, LVT (low V_{th}) transistors are used in the design which leads to 30% reduction in parasitic capacitance compared to the SVT (standard V_{th}) case.[7] However, using LVT transistors leads to more power consumption. Because $g_m = I_{DC}/(V_{DD}/2 - V_{th})$, therefore as V_{th} decreases, the required DC current for the same g_m increases accordingly. Two negative resistors made of inverters are added to the circuit to control the impedance level of the internal nodes of the filter namely r_{o1} and r_{o2} in the design (see Fig. 7(c)). These negative resistors have a separate supply voltage (AV_{DD2}) with nominal value of 1.2 V. To make the common-mode positive feedback which exists in the gyrator stable, two diode connected inverters are added to the output nodes of the filter. All the G_ms together draw about 11.7 mA from the 1.2 V. A modulo-8 ring counter is used to obtain 8 non-overlapping clock signals with 12.5% duty cycle. The simplified block diagram of the clock generator [29] is shown in Fig. 12(e) where a master clock at 8 times the switching frequency is applied externally. Due to its lower power consumption and higher speed, D flip-flops based on transmission gates have been exploited [29]. Fig. 13 illustrates the on-chip measurement interface of the proposed filter which is also used in the simulations.

Fig. 14(a) illustrates the effect of Miller compensation method on the passband shape of the filter. Without Miller compensation, there is a 1.5 dB peaking in the passband of the filter. The optimum value of the Miller capacitor (45 fF) is found using simulations. The simulated transfer function of the proposed filter in the whole tuning range is illustrated in Fig. 14(b). The utilized value of AV_{DD2} (a separate voltage source for negative resistors) is shown for each clock frequency. As discussed before, the parasitic capacitance at each node of the filter modifies the equivalent resistance of that node. This effect is frequency dependent which means that as clock frequency reduces, the Q-factor of the filter increases. This leads to higher ripples in the passband of the filter for low clock frequencies. As a remedy, the supply voltage of the negative resistors is reduced for low clock frequencies. Albeit the amount of modification in AV_{DD2} is less than $\leq$7%. The simulated passband details of the filter shape in the whole tuning range is depicted in Fig. 14(c) which includes the case where the AV_{DD2} is fixed (1.2 V). The passband gain of the filter varies by 1 dB in the tuning range and the maximum passband ripple is 0.3 dB. As can be seen in Fig. 14(c), the passband ripple of the filter without any modification ($AV_{DD2} = 1.2$ V) is $\leq$ 0.6 dB. In reality, due to PVT variations, the value of the G_m cells changes, leading to a

[6]The voltage loss can be compensated by an slight increase of the DC bias voltage of the clock signals.

[7]The difference between the threshold voltage of the two case is 0.1 V.

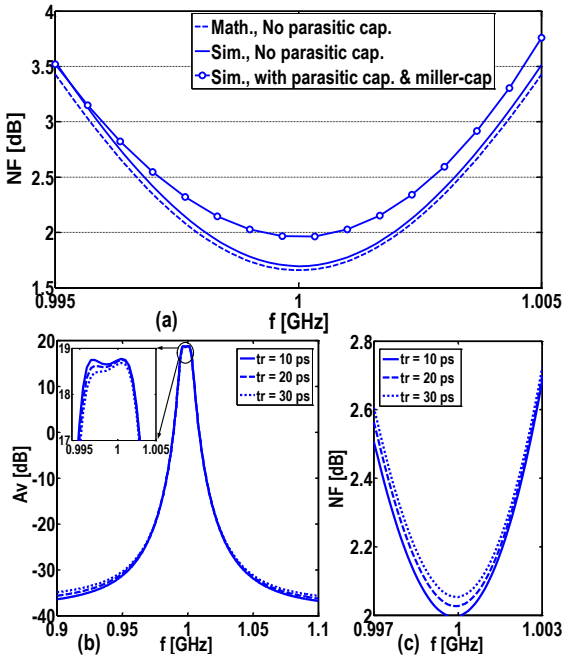

Fig. 15. (a) A comparison between the simulated and calculated NF in the case of no parasitic capacitance and simulated NF in the case of parasitic capacitance and Miller compensation (b) The effect of rise/fall time on the transfer function and (c) noise figure of the filter.

modifcation in the bandwidth of the filter. However, by tuning the supply voltage of the G_m cells, this can be corrected.

A. Simulation Results

The simulated NF of the filter is shown in Fig. 15(a) for two cases: 1) there is no parasitic capacitance in the circuit and 2) there are parasitic capacitances and Miller compensation. Moreover, the mathematical derivation of the noise figure in the case of no parasitic capacitance [(28) in Appendix C] is illustrated for comparison which is in close agreement with simulation. The increased capacitance at the input port of the filter due to the Miller capacitance and its associated loss (see section III) is the cause of 0.3 dB degradation in the NF of the filter compared to the case of no parasitics. The simulated NF of the filter in the whole tuning range is around 2 dB.

The effect of a non-zero rise/fall time of the clock signals on the performance of the filter is illustrated in Fig. 15(b) and (c). As can be seen, for the rise/fall time values shown in Fig. 15(b) and (c), its effect on the transfer function and NF is not considerable. Also, the effect of rise/fall time on the performance of a passive mixer has been shown in [30]. In general, as the rise/fall increases, the average value of the switch resistance increases and this leads to a raise in the NF and a degradation of the filter shape.

Fig. 16(a) shows the simulated phase-noise of on-chip 8-phase LO signals (1 GHz) for a noisy[8] and a noiseless external signal generator (8 GHz). Clearly, in the case of a noisy

[8]The phase-noise has been extracted from the datasheet of an Agilent signal generator E8251A PSG-A and has been used in simulations. This signal generator was utilized in measurements.

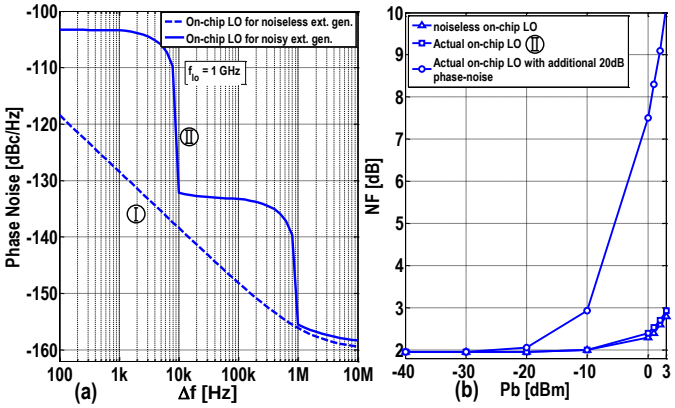

Fig. 16. (a) The simulated phase-noise of on-chip 8-phase LO signals ($f_{lo} = 1$ GHz) for two cases: (I) ideal and (II) noisy external signal generator (at $8f_{lo}$) (b) The simulated NF of the filter when an out-of-band CW blocker is present at $f_{lo} + f_b$ ($f_{lo} = 1$ GHz, $f_b = 20$ MHz) for three cases: 1) noiseless on-chip 8-phase LO signals 2) actual on-chip 8-phase LO signals and 3) actual on-chip 8-phase LO signals with $+20$ dB additional phase-noise.

external signal generator, the phase-noise of the on-chip LO signals for low offset frequencies is dominated by the phase-noise of the external generator which is attenuated by 18 dB $(20\log(8))$. For large offset frequencies, the phase-noise is limited by the noise contribution of the frequency divider and drivers. The NF of the filter, for a blocker located at $f_{lo} + f_b$ with an input power of P_b where f_{lo} and f_b are 1 GHz and 20 MHz respectively, is shown in Fig. 16(b) for three cases: 1) noiseless on-chip LO signals, 2) on-chip LO signals with actual phase-noise [(II) in Fig. 16(a)] and 3) actual on-chip LO signals with $+20$ dB additional phase-noise. As can be seen, in the two cases of noiseless and actual on-chip LO signals, the NFs are similar. This means that the degradation of the NF is mainly due to gain compression rather than reciprocal mixing. However, by increasing the phase-noise of the actual on-chip LO signals by $+20$ dB, the NF considerably increases as the magnitude of the blocker increases. In this case, the blocker noise performance of the filter is limited by reciprocal mixing. The exact mathematical derivation of the effect of phase-noise on N-path filters can be found in [31].

VI. Measurements

The chip micrograph of the proposed filter is illustrated in Fig. 17. The chip has been fabricated in CMOS LP 65 nm technology and the active area of the filter is about 0.27 mm^2. The chip is mounted in a QFN32 package and tested on a printed circuit board. The measured transfer function of the filter in the whole tuning range (0.1 GHz to 1.2 GHz) and the passband shape of the filter are demonstrated in Fig. 18. The maximum passband ripple of the filter in the whole tuning range is less than 0.6 dB. The negative resistances of the filter are slightly changed by tuning their supply voltages (AV_{DD2}) ($\leq 8\%$) over the whole tuning range. However, without any modifications, the passband ripple is still less than 1 dB ($\leq$ 0.6 dB in the simulation) over the whole tuning range. The measured stopband rejection of the filter is 59 dB. The bandwidth of the filter is about 8 MHz which is equivalent to

TABLE I
COMPARISON TABLE

	[This work]	Darvishi [16]	Soorapanth [6]	Ghaffari [20]	Borremans [33]	Mirzaei [19]	Murphy [32]
Circuit Type	Filter				Receiver		
CMOS Tech. [nm]	65	65	250	65	40	65	40
Frequency range [GHz]	0.1-1.2	0.4-1.2	2.14	0.1-1	0.4-6	2	0.08-2.7
IIP_3(OOB) [dBm]	+26	+29	N/A	>+14	+10	-6.3	+13.5
$B_{1dB,CP}$ [dBm]	+7	N/A	N/A	>+2	-8	N/A	<0
NF [dB]	2.8	10	19	3-5	3	5.8	2
Gain [dB]	+25	+3.5	0	-2	+70	+55.8	+70
BW [MHz]	8	20	60	35	0.4-30	4	N/A
Ripple [dB]	<0.6	<0.4	0.7	-	-	-	-
Filter order	6	4	6	2	2 @RF	6	2 @RF
Stop-band rejection [dB]	59	>55	>30	15	<15 @RF	50	<15 @RF
FOM [dB-Hz/mW] [8]	132.5	146.4	129.2	-	-	-	-
V_{DD} [Volts]	1.2	1.2/2.5	2.5	1.2	2.5	1.2/2.5	1.3
Power [mW]	$P_{ana.}$→ 14.4 $P_{dig.}$→ 3.6-43	12.8-21.4	17.5	2-20	75-137.5	21mA	35-78
Area [mm^2]	0.27	0.12	3.51	0.07	2	0.76	1.2

a Q-factor of 125 at center frequency of 1 GHz. Because the bandwidth of N-path filters is constant, as the center frequency of the filter reduces, the Q-factor of the filter will decrease. In this case, the Q-factor of the filter varies from 12.5 at $f_{\rm lo} = 0.1$ GHz to 150 at $f_{\rm lo} = 1.2$ GHz. The passband gain of the filter is about $+25$ dB after de-embedding the loss of the common-drain buffers calculated from simulation. The measured S_{11} varies between -5 dB and -8 dB, in the passband of the filter over the clock frequency range. The measured NF of the filter is shown in Fig. 19(a). It varies from 2.6 dB to 3.1 dB in the tuning range. The filter can attain a low NF because of: 1) the exploitation of asymmetric gyrators; 2) a relatively high value of $g_{\rm m1}$; 3) the utilization of a very small amount of negative admittance; 4) a low switch resistance; and 5) the utilization of 8 phases which leads to less harmonic-folding of the noise at higher harmonics of the clock frequency. The measured out-of-band IIP_3(OOB) and 1dB blocker compression point $B_{-1dB,CP}$ for different offset frequencies from $f_{\rm lo} = 1$ GHz are illustrated in Fig. 19(b). For IIP_3 measurements, two tones which are located at frequency of $f_{\rm lo} + \Delta f$ and $f_{\rm lo} + 2\Delta f$ have been used. For $B_{-1dB,CP}$ measurements, the input power of the blocker located at $f_{\rm lo}+\Delta f$ that leads to a 1 dB reduction in the passband gain of the filter is reported. The measured IIP_3(OOB) of $+26$ dBm and 1dB blocker compression point $B_{-1dB,CP}$ of $+7$ dBm are achieved at Δf of only 50 MHz and $f_{\rm lo}$ of 1 GHz. To demonstrate the resilience of the filter to large out-of-band blockers, the transfer function of the filter at $f_{\rm lo} = 1$ GHz is measured with and without a continuous-wave blocker with an input power of $+2.3$ dBm located only $+20$ MHz far from the center frequency of the filter and it is shown in Fig. 19(c). The filter can achieve excellent out-of-band linearity because of: 1) the first section being passive and hence the first G_m already receives a $2^{\rm nd}$-order filtered signal and the further filtering in the subsequent stages; 2) the very linear differential I/V characteristic of an inverter when loaded with low impedance [11], [32]. The measurement results are

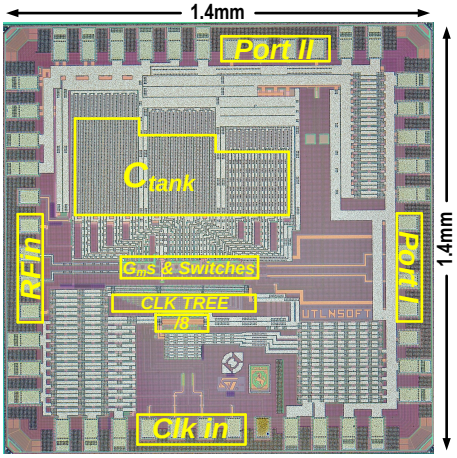

Fig. 17. CMOS LP 65 nm chip micrograph indicating functional blocks.

compared with simulation results in Table II. The in-band linearity of the filter is limited by inverters. However for out-of-band signals, all nodes of the filter see a 10 Ω resistance to the ground. Due to the large amount of attenuation provided by the switched-capacitor sections, the nonlinearity contribution of the inverters is reduced considerably. In this case, the linearity of the filter will be limited to both the linearity of the switches and inverters. The filter draws 11.7 mA and the LO chain draws 3 to 36 mA from 1.2 V in the whole tuning range. The LO feedtrough to the input port of the filter is less than -64 dBm at $f_{\rm lo}$ of 1 GHz. As discussed previously, folding-back starts from $7f_{\rm lo}$. However, due to mismatches between switches and clock signals (the mismatch between the clock signals is the major contributor [16], [19], [20].), folding-back also occurs from $3f_{\rm lo}$ and $5f_{\rm lo}$ with measured normalized gain of -54 dB and -68 dB, respectively.

If the same filter were designed as a conventional G_m-C filter, to synthesize the three resonators, 12 additional

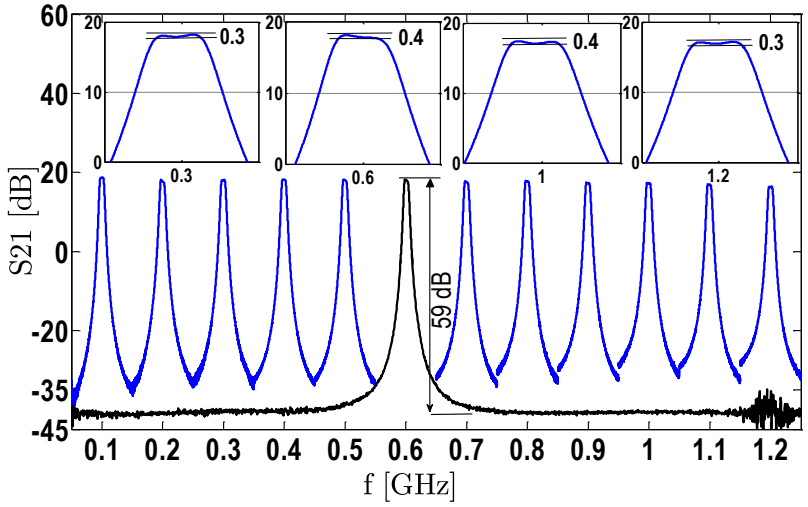

Fig. 18. Measured transfer function of the filter in whole tuning range for the variable AV_{DD2} (the same as the values used in the simulations) (0.1 GHz to 1.2 GHz). The sweeping frequency range for each f_{lo} is 100 MHz except for $f_{lo} = 600$ MHz where a full sweeping range is utilized; In addition, the passband shape of the filter at some center frequencies is shown.

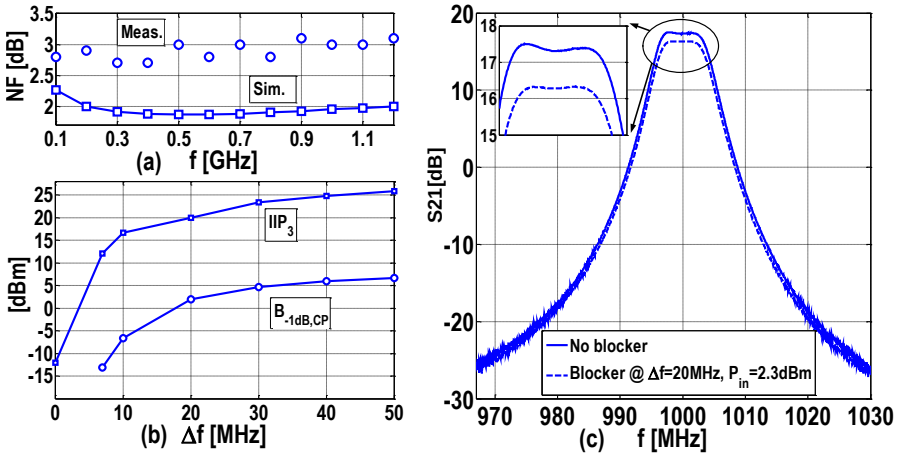

Fig. 19. (a) Measured NF of the filter over the whole tuning range (b) Measured out-of-band IIP_3 and 1dB blocker compression point $B_{-1dB,CP}$ of the filter for different values of offset frequency from center frequency of the filter ($f_{lo} = 1$ GHz) (c) Measuring the transfer function of the filter at f_{lo} of 1 GHz with and without a large out-of-band blocker with input power of $+2.3$ dBm at offset frequency of 20 MHz.

TABLE II
A COMPARISON BETWEEN SIMULATION AND MEASUREMENT RESULTS

	Measurement	Simulation
Gain [dB]	$+25$	$+26$
NF [dB]	$2.6 - 3.1$	$1.9 - 2.3$
$IIP3_{IB}$ [dBm]	-12	-14
$IIP3_{OOB}$ [dBm] (Δf= $+50$MHz)	$+26$	$+30$
P_{-1dB} [dBm]	-23	-26
$B_{-1dB,C}$ [dBm] (Δf= $+50$MHz)	$+7$	$+7.5$
BW [MHz]	8	9
Ripple [dB]	≤ 0.6	≤ 0.3

inverters would be required. Moreover, the output impedance of these extra G_m cells would reduce the impedance level at internal nodes of the filter and hence more negative admittance would be necessary. This would lead to an increase in power consumption of the filter and reduction of the DR of the filter. Also, it would need an additional PLL to correct the center frequency of the filter over process corners [10] which is in contrast to N-path filters where the center frequency of the filter is determined by the switching frequency. In the case of Q-enhanced LC filters, due to the low Q-factor of the on-chip inductors, a large amount of negative resistance would be needed which would definitely reduce the DR of the filter and more importantly LC filters are not tunable and process scalable. Finally, it can be said the DR of the proposed BPF is the same as its LPF counterpart which contains a much lower number of active devices compared to BP G_m-C filters. The filter is compared with state-of-the-art integrated filters [6], [16], [20] and complete receivers [19], [32], [33] in Table I. According to the FOM described in [8], the FOM of our filter is 127.4 dB-Hz/mW at 1 GHz and 132.5 dB-Hz/mW at 0.1 GHz. Compared to [20], much better passband shape, selectivity and stopband rejection are obtained. Compared to [19], better out-of-band linearity, filter shape and NF are accomplished. Compared to [16], the NF is improved by more than 7 dB. The proposed integrated tunable BPF can be

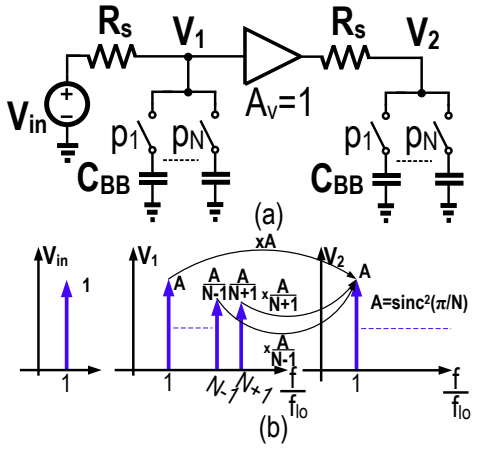

Fig. 20. (a) A cascade of two identical N-path filters (b) A graphical representation of calculation of the total gain of the filter.

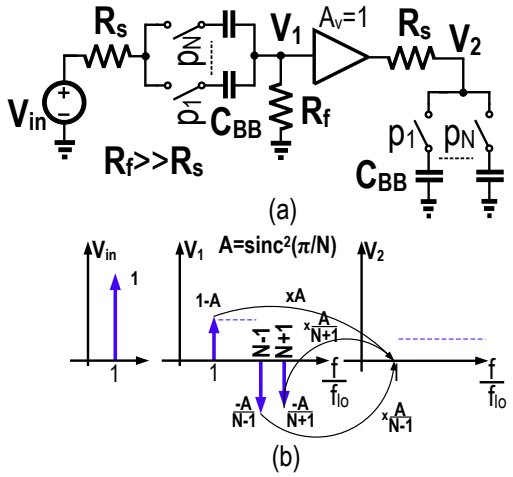

Fig. 21. (a) A cascade of a notch filter [27] and band-pass N-path filter (b) A graphical representation of calculation of the total gain of the filter at f_{lo}.

used as a channel-select SAW-LNA hybrid which is tunable over a decade in frequency. Due to the isolation provided by G_{m1}, when a large out-of-band blocker is not present, it is possible to turn-off the first stage, lowering the dynamic power consumption and improving the NF of the filter.

VII. Conclusion

A design methodology for synthesis of active N-path BPFs is introduced. Based on this methodology, a 0.1-to-1.2 GHz tunable 6^{th}-order N-path channel-select filter in 65 nm LP CMOS is introduced. It is based on coupling N-path filters with gyrators, achieving a "flat" passband shape and high out-of-band linearity. A Miller compensation method is utilized to considerably improve the passband shape of the filter. The filter has 2.8 dB NF, +25 dB voltage gain, +26 dBm wideband IIP_3, +7 dBm $B_{1dB,CP}$ and 59 dB stopband rejection. The analog and digital part of the filter draw 11.7 mA and 3-36 mA from 1.2 V, respectively. The digital power consumption includes all the digital circuitry, namely the inverters that work at $8f_{lo}$, the divider, and the LO distribution network. Because the filter consists of 3 passive-mixer alike stages, the P_d of the filter is 2-3 times higher than the P_d of a passive-mixer. The proposed filter only consists of inverters, switches and capacitors and therefore it is friendly with process scaling.

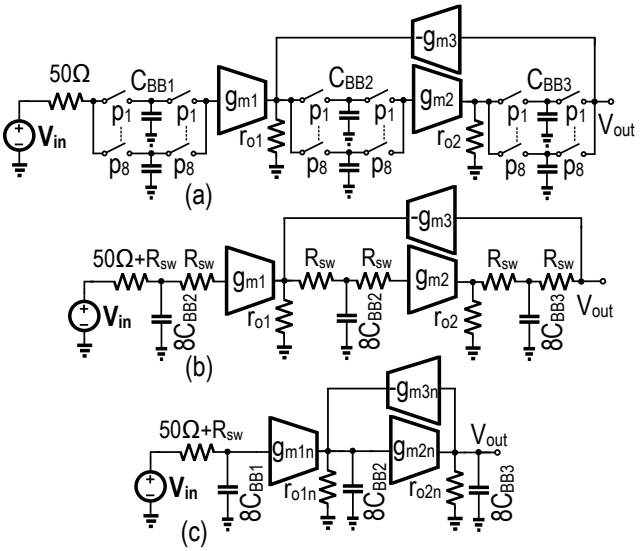

Fig. 22. (a) Elimination of the effect of the switch resistance on the ultimate-rejection of the filter (b) Its LPF counterpart (c) A simplified version of the filter shown in part (b).

Appendix A
Cascading Two N-path Filters

We already know that the gain of a simple N-path filter at its center frequency is $\text{sinc}^2(\pi/\text{N})$. Accordingly, it may be thought that the gain of the cascade of two N-path filters shown in Fig. 20(a) should be $\text{sinc}^4(\pi/\text{N})$. However based on the proposed methodology, also the gain of the cascaded one should be $\text{sinc}^2(\pi/\text{N})$. What causes this discrepancy?

We should make two observations: 1) The first N-path filter other than making a signal at f_{lo} at node V_1, also produces signals at $(1+\text{kN})f_{lo}$ with gain of $\text{sinc}^2(\pi/\text{N})/(1+\text{kN})$ [16]; 2) The second N-path filter other than passing the signal at f_{lo} without any frequency translation, also translates the produced harmonics of the first N-path filter at $(1+\text{kN})f_{lo}$ to f_{lo} at node V_2 by gain of $\text{sinc}^2(\pi/\text{N})/(1+\text{kN})$ [16]. This process is illustrated graphically in Fig. 20(b). Therefore the gain of the filter is $\text{sinc}^4(\pi/\text{N})\times\sum_{k=-\infty}^{\infty}1/(1+k\text{N})^2$ which eventually can be simplified to $\text{sinc}^2(\pi/\text{N})$. It is easy to show that the gain of an N-path notch filter [27] is $1-\text{sinc}^2(\pi/\text{N})$ where as N decreases the depth of notch reduces. Now, consider the N-path filter illustrated in Fig. 21(a). Interestingly, it can be shown that the gain of the filter at f_{lo} at node V_2 is zero and does not depend on the number of phases! Based on the same observations we did above, the total gain of the filter can be found using Fig. 21(b). Consequently, the gain at f_{lo} will be $[1-\text{sinc}^2(\pi/\text{N})]\times\text{sinc}^2(\pi/\text{N})-\text{sinc}^4(\pi/\text{N})\times\sum_{k\neq 0}1/(1+k\text{N})^2$ which finally can be simplified to 0.

APPENDIX B
ELIMINATION OF THE EFFECT OF SWITCH RESISTANCE ON ULTIMATE-REJECTION OF THE FILTER

It is possible to utilize the technique used in [16] to suppress the effect of switch resistance on the stopband rejection of the filter at the cost of doubling the dynamic power consumption. In this way, the out-of-band linearity of the filter improves. (For example, the first G_m cell would see higher stopband rejection.) This is illustrated in Fig. 22(a). The LPF counterpart of the filter is shown in Fig. 22(b) which interestingly can be simplified to the circuit shown in Fig. 22(c). The values of the g_{m1n}, g_{m1n} and g_{m3n} are $g_{m1} \times r_{o1}/(r_{o1} + R_{sw})$, $g_{m2} \times r_{o2}/(r_{o2} + R_{sw})$ and $g_{m3} \times r_{o1}/(r_{o1} + R_{sw})$, respectively. The values of r_{o1n} and r_{o2n} are $r_{o1} + R_{sw}$ and $r_{o2} + R_{sw}$, respectively.

APPENDIX C
NF DERIVATION

Using the same procedure as demonstrated in section III, the exact transfer functions of different noise sources $\omega_{noise} = (1+kN)\omega_{lo}+\Delta\omega$, $k \in \mathbb{Z}$ to the output node ($\omega_{out} = \omega_{lo}+\Delta\omega$) are described in:

$$
\begin{aligned}
\frac{V_{out}|_{\omega_{out}}}{I_{n2}|_{\omega_{noise}}} &= \begin{cases} \beta_1 Z_{n2}(j\Delta\omega) + \alpha_3 & k = 0 \\ \beta_k Z_{n2}(j\Delta\omega) & k \neq 0 \end{cases} \\
\frac{V_{out}|_{\omega_{out}}}{I_{n3}|_{\omega_{noise}}} &= \begin{cases} \beta_1 Z_{n3}(j\Delta\omega) - R_{sw}\alpha_2 & k = 0 \\ \beta_k Z_{n3}(j\Delta\omega) & k \neq 0 \end{cases} \\
\frac{V_{out}|_{\omega_{out}}}{V_{n1}|_{\omega_{noise}}} &= \begin{cases} \beta_1 H_{n1}(j\Delta\omega) - \dfrac{\alpha_3 g_{m1} R_s}{R_s + R_{sw}} & k = 0 \\ \beta_k H_{n1}(j\Delta\omega) & k \neq 0 \end{cases} \\
\frac{V_{out}|_{\omega_{out}}}{V_{n2}|_{\omega_{noise}}} &= \begin{cases} \beta_1 H_{n2}(j\Delta\omega) - \alpha_1 & k = 0 \\ \beta_k H_{n2}(j\Delta\omega) & k \neq 0 \end{cases} \\
\frac{V_{out}|_{\omega_{out}}}{V_{n3}|_{\omega_{noise}}} &= \begin{cases} \beta_1 H_{n3}(j\Delta\omega) + \alpha_4 & k = 0 \\ \beta_k H_{n3}(j\Delta\omega) & k \neq 0 \end{cases}
\end{aligned}
\tag{24}
$$

where

$$
\begin{aligned}
&H_{n1}(s) = \alpha_1[H_{bb2}(s) - g_{m1}Z_{x1}(s)] + \alpha_2[g_{m1}Z_{x2}(s) - H_{bb3}(s)], \\
&- \frac{\alpha_3 R_s g_{m1}}{R_{sw} + R_s} H_{bb1}(s), \\
&H_{n2}(s) = -\alpha_1 H_{x1}(s) + \alpha_2 H_{x2}(s), \\
&H_{n3}(s) = \alpha_1[g_{m3}Z_{x1}(s) - g_{o2}Z_{x3}(s)] - \alpha_2 g_{m3} Z_{x2}(s) - \\
&\alpha_2 g_{o2} Z_{x4}(s), \\
&Z_{n2}(s) = -\alpha_1 Z_{x1}(s) + \alpha_2 Z_{x2}(s), \\
&Z_{n3}(s) = -\alpha_1 Z_{x3}(s) + \alpha_2 Z_{x4}(s),
\end{aligned}
\tag{25}
$$

and

$$
\begin{aligned}
\alpha_1 &= \frac{R_{sw} g_{m2}}{1 + D \times R_{sw}^2 + (g_{o1} + g_{o2})R_{sw}}, \\
\alpha_2 &= \frac{1 + g_{o1}R_{sw}}{1 + D \times R_{sw}^2 + (g_{o1} + g_{o2})R_{sw}}, \\
\alpha_3 &= R_{sw}\alpha_1,\ \alpha_4 = 1 - g_{m3}\alpha_3 - R_{sw} g_{o2} \alpha_2,
\end{aligned}
\tag{26}
$$

and

$$
\begin{aligned}
Z_{x1}(s) &= \frac{g_{o2} + 8C_{BB3}s(1 + g_{o2}R_{sw})}{den(s)}, \\
Z_{x2}(s) &= \frac{g_{m2}(1 + 8C_{BB2}sR_{sw})}{den(s)}, \\
Z_{x3}(s) &= \frac{-g_{m3}(1 + 8C_{BB3}sR_{sw})}{den(s)}, \\
Z_{x4}(s) &= \frac{g_{o1} + 8C_{BB2}s(1 + g_{o1}R_{sw})}{den(s)}, \\
H_{x1}(s) &= \frac{-D(1 + 8C_{BB3}sR_{sw})}{den(s)}, \\
H_{x2}(s) &= \frac{-8g_{m2}C_{BB2}s}{den(s)}, \\
den(s) &= D(As^2 + Bs + 1).
\end{aligned}
\tag{27}
$$

Now, by knowing the transfer function of all the noise sources to the output voltage (24), the total output voltage noise of the filter, including all the folding-back components, can be found (see Fig. 11(d)). (28) is used in section V to calculate the noise figure of the filter.

$$
\begin{aligned}
0.5\overline{V_{out,n}^2}|_{\omega_{out}} &= \left(\sum_{i=2}^{3} \overline{I_{ni}^2} |Z_{ni}|^2 + \sum_{i=1}^{3} \overline{V_{ni}^2} |H_{ni}|^2 \right) \times \left(\beta_1 - \beta_1^2\right) \\
&+ \overline{V_{n1}^2} \left| \beta_1 H_{n1} - \frac{\alpha_3 g_{m1} R_s}{R_s + R_{sw}} \right|^2 + \overline{V_{n2}^2} \left| \beta_1 H_{n2} - \alpha_1 \right|^2 + \\
&\overline{V_{n3}^2} \left| \beta_1 H_{n3} + \alpha_4 \right|^2 + \overline{I_{n2}^2} \left| \beta_1 Z_{n2} + \alpha_3 \right|^2 + \overline{I_{n3}^2} \left| \beta_1 Z_{n3} - \alpha_2 R_{sw} \right|^2 \\
&+ 2kTR_s \left(|H|^2 + \left(\beta_1^{-1} - 1\right) \left| H - \frac{\sqrt{2}\alpha_3 R_{sw} g_{m1}}{R_{sw} + R_s} \right|^2 \right).
\end{aligned}
\tag{28}
$$

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