A Flicker Noise/IM3 Cancellation Technique for Active Mixer Using Negative Impedance

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***Abstract* —** This paper presents an approach to simultaneously cancel flicker noise and IM3 in Gilbert-type mixers, utilizing negative impedances. For proof of concept, two prototype double-balanced mixers in 0.16μm CMOS are fabricated. The first demonstration mixer chip was optimized for full IM3 cancellation and partial flicker noise cancellation; this chip achieves 9dB flicker noise suppression, improvements of 10dB for IIP3, 5dB for conversion gain, and 1dB for input P_{1dB} while the thermal noise increased by 0.1dB. The negative impedance increases the power consumption for the mixer by 16%, and increases the die area by 8% (46x28μm^2). A second demonstration mixer chip aims at full flicker noise cancellation and partial IM3 cancellation, while operating on a low supply voltage ($0.67\times V_{DD}$); in this chip, the negative impedance increases the power consumption by 7.3%, and increases the die area by 7% (50x20μm^2). For one chip sample, measurements show >10dB flicker noise suppression within ±200% variation of the negative impedance bias current; for ten randomly selected chip samples >11dB flicker noise suppression is measured.

***Index Terms* —**Active mixer, flicker noise, direct conversion, CMOS, narrowband, receiver, IIP3, linearity, IM3, distortion cancellation, noise cancellation.

I. INTRODUCTION

CMOS active mixers have high gain but also suffer from high flicker noise as well as from low linearity. While high flicker noise causes serious sensitivity degradation especially in narrowband

direct-conversion receivers, mixers with poor linearity limit the dynamic range of the receiver.

Three major techniques have been presented for flicker noise reduction in CMOS active mixers:

1. Dynamic current injection [1-2]: a pMOS cross-coupled pair injects current into the NMOS mixer transconductor stage only at the switching on/off instants (at $0.5T_{LO}$) in such a way that no DC current flows through the switches then. This is reported to suppress the flicker noise leakage from the switching pair.
2. Double LO switch pairs [3]: extra switches in series driven at 2LO frequency are used in such a way that during the switching period little DC current flows through the major switches that are driven by LO signal, thereby reducing flicker noise leakage.
3. RF leakageless static current bleeding with two resonating inductors [4]. Two inductors are connected between the mixer transconductor stage and the current bleeding circuit. The inductors resonate out the tail capacitance and reduce the RF signal leakage to the current bleeding circuit.

In Technique 1, a large LO swing and large headroom is required, increasing the LO power and decreasing the conversion gain due to the use of small R_{load} [1]. Technique 2 needs a stack of three transistors plus the load, which is not suitable for deep-submicrometer technologies with low supply voltages. Technique 3 needs two inductors which consume significant die area. Common to all the techniques in [1-4] is that the effect of the transistor output resistance on the flicker noise leakage is neglected.

In technologies with long-channel transistors where the output capacitance of transistors is dominant in the transistors' output impedance at RF frequencies, the effect of output resistance on flicker noise leakage can be neglected [1-4]. However, nowadays CMOS technologies offer

transistors with f_T well above 100 GHz, at the same time with lower transistor output resistance and lower supply voltage [5]. Neglecting the effect of output resistance in deep-submicrometer technologies can yield a significant underestimation of the output flicker noise [7]. Taking into account the effect of both output resistance and output capacitance on flicker noise leakage, in this paper we propose a combined flicker noise/IM3 cancellation technique that uses a negative impedance to minimize the flicker noise leakage from the switching pair and to simultaneously improve the linearity. Section II presents the circuit theory behind this flicker noise/IM3 cancellation technique. Section III and IV show a circuit implementation and the measurement and simulation results; the results are summarized in section V.

II. FLICKER NOISE/IM3 CANCELLATION USING A NEGATIVE IMPEDANCE

A. Flicker noise leakage in Gilbert mixers

The double-balanced Gilbert mixer shown in Fig. 1a is widely used as the active downconverter in CMOS receivers. Transistor M_{3a}/M_{3b} convert v_{in} into current that is commuting via switch pair M_{1a}/M_{2a} and M_{1b}/M_{2b} respectively. The flicker noise output of the Gilbert mixer, $v_{fl,out}(t)$, is dominated by the switch pair M_1/M_2, while transistor M_3 is causing thermal noise folding [6-7]. Assuming perfect symmetry in the mixer, the flicker noise leakage mechanism from each switch is the same: it is hence sufficient to focus on flicker noise leakage from one of the switch pair transistors. In [7] the time-varying small signal model shown in Fig. 1b is used to analyze the flicker noise contributed by M_{1a} in one LO period at the mixer output ($v_{fl,out}^{M_{1a}}(t)$). The flicker noise of M_{1a} is modeled by the equivalent gate-referred root mean square (rms) noise voltage $v_{fl,in}^{M_{1a}}$. For a first order approximation of $v_{fl,out}^{M_{1a}}$, a few assumptions are made:

- The LO signal is modeled by a trapezoid shown in Fig. 2a with a rise/fall time (e.g. t_3-t_2)

equal to $\alpha \cdot T_{LO}$.

- In (t_1, t_2), M_{2a} and M_{2b} are off while in (t_3 , t_4) M_{1a} and M_{1b} are off.

Taking into account the transconductance of M_1, M_2 and M_3, and the output admittance of M_3 ($Y_{ds}^{M_{3a}} = g_{ds}^{M_{3a}} + j\omega_{LO}C_{ds}^{M_{3a}}$), the flicker noise contribution of M_{1a} at t_1, $\frac{T_{LO}}{2}$ and t_3 in Fig. 2a are given by:

$$v_{fl,out}^{M_{1a}}\Big|_{t_1} = \frac{-g_m^{M_{1a}} R_L Y_{ds}^{M_{3a}} v_{fl,in}^{M_{1a}}}{g_m^{M_{1a}} + Y_{ds}^{M_{3a}}}\Bigg|_{t_1} \quad (1)$$

$$v_{fl,out}^{M_{1a}}\Big|_{\frac{T_{LO}}{2}} = -g_m^{M_{1a}} R_L v_{fl,in}^{M_{1a}}\Big|_{\frac{T_{LO}}{2}} \quad (2)$$

$$v_{fl,out}^{M_{1a}}\Big|_{t_3} = 0 \quad (3)$$

In (t_1, t_2) M_{1a} and M_{3a} form a cascode amplifier. Due to the finite output impedance of M_{3a} in deep-submicrometer CMOS, the noise contribution from the cascode transistor M_1, given by (1), cannot be neglected. In (t_2, t_3) both M_{1a} and M_{2a} are on, while at $\frac{T_{LO}}{2}$ M_{1a} and M_{2a} act as a balanced differential pair. In this period of time, the output impedance of M_3 has a negligibly small effect on $v_{fl,out}^{M_{1a}}$ as shown by (2). In (t_3, t_4) M_{1a} is assumed to be off, thus $v_{fl,out}^{M_{1a}}$ is zero. Note that the integral (or area) of $v_{fl,out}^{M_{1a}}(t)$ shown in Fig. 2(b) and (c) corresponds to the flicker noise leakage that involves no frequency translation [7]. As a result, the flicker noise at the mixer output contributed by M_{1a}/M_{2a} and M_{1b}/M_{2b} is

$$S_{fl,out} = 4 \times \left| \int_0^{T_{LO}} Re\left[v_{fl,out}^{M_{1a}}(t)\right] dt + j \times \int_0^{T_{LO}} Im\left[v_{fl,out}^{M_{1a}}(t)\right] dt \right|^2$$

$$= \frac{4}{{T_{LO}}^2} \times \left| (t_2 - t_1) \cdot v_{fl,out}^{M_{1a}}\Big|_{t_1} + t_1 \cdot \left(v_{fl,out}^{M_{1a}}\Big|_{\frac{T_{LO}}{2}} - v_{fl,out}^{M_{1a}}\Big|_{t_1} \right) + \left(t_3 - \frac{T_{LO}}{2}\right) \cdot v_{fl,out}^{M_{1a}}\Big|_{\frac{T_{LO}}{2}} \right|^2 \quad (4)$$

For the symmetrical LO signal shown in Fig. 2a, with a rise/fall time equal to $\alpha \cdot T_{LO}$, the time instants t_1, t_2 and t_3 can be rewritten as $t_1 = \alpha T_{LO}/2$, $t_2 = (1-\alpha)T_{LO}/2$, $t_3 = (1+\alpha)T_{LO}/2$. This enables rewriting (4) into

$$S_{fl,out} = \left|(1-3\alpha)\cdot v_{fl,out}^{M_{1a}}\Big|_{t_1} + 2\alpha v_{fl,out}^{M_{1a}}\Big|_{\frac{T_{LO}}{2}}\right|^2 \quad (5)$$

B. Negative impedance for flicker noise cancellation

To minimize the integral of $v_{fl,out}^{M_{1a}}(t)$ in (4) --- hence to minimize the flicker noise leakage --- we apply a negative impedance $Y_{neg} = G_{neg} + j\omega C_{neg}$ between the drain of M_{3a} and M_{3b} as shown in Fig. 3. Using the model shown in Fig.3b, this yields a different $v_{fl,out}^{M_{1a}}$ for the time interval (t_1-t_2):

$$v_{fl,out}^{M_{1a}}\Big|_{t_1} = \frac{-g_m^{M_{1a}} R_L \left(Y_{ds}^{M_{3a}} + 2Y_{neg}\right) v_{fl,in}^{M_{1a}}}{g_m^{M_{1a}} + Y_{ds}^{M_{3a}} + 2Y_{neg}}\Bigg|_{t_1} \quad (6)$$

$$v_{fl,out}^{M_{1a}}\Big|_{\frac{T_{LO}}{2}} = -g_m^{M_{1a}} R_L v_{fl,in}^{M_{1a}}\Big|_{\frac{T_{LO}}{2}} \quad (7)$$

$$v_{fl,out}^{M_{1a}}\Big|_{t_3} = 0 \quad (8)$$

Eq. (6) shows that for $C_{neg} \approx -0.5C_{tail}$ and $G_{neg} \in \left[\frac{-g_{ds}^{M_{3a}} - g_m^{M_{1a}}}{2}, \frac{-g_{ds}^{M_{3a}}}{2}\right]$ the sign of the real part of $v_{fl,out}^{M_{1a}}\Big|_{t_1}$ changes from negative to positive (a detailed derivation is presented in the appendix). At $\frac{T_{LO}}{2}$ the negative impedance has no effect on $v_{fl,out}^{M_{1a}}$ as shown in (7) since M_{1a} and M_{2a} act as a balanced differential pair. In (t_3, t_4) M_{1a} is off, thus $v_{fl,out}^{M_{1a}}$ is zero. Now the new approximated waveform of $v_{fl,out}^{M_{1a}}(t)$ is shown in Fig. 4b. The negative impedance Y_{neg} changes the real part of $v_{fl,out}^{M_{1a}}$ in (t_1, t_2) from negative to positive value, which enables minimization of the area of $v_{fl,out}^{M_{1a}}(t)$ in one LO period. This leads to the cancellation of the flicker noise leakage from the switching pair (M_{1a}/M_{2a} and M_{1b}/M_{2b}). For a complete flicker noise leakage cancellation, (5) equates to zero. Together with (6-7), this equation gives the condition for *complete* flicker noise leakage cancellation:

$$\begin{cases} G_{neg} = -\frac{g_{ds}^{M_{3a}}}{2} - \frac{\alpha g_m^{M_{1a}}}{(1-\alpha)} \\ C_{neg} = -\frac{C_{tail}}{2} \end{cases} \quad (9)$$

Note that for complete cancellation across process and temperature spread, G_{neg} should track the variation of the sum of g_{ds} and g_m and C_{neg} should track C_{tail}.

C. Negative-impedance impact on gain and thermal noise

It was derived in [7] that the first-order Fourier coefficient of the instantaneous voltage gain $F^{M_3}(t) = v_{out}/v_{in}$ in one LO period corresponds to the conversion gain of a mixer. Using the model shown in Fig. 5a, a sufficiently accurate approximation of $F^{M_3}(t)$ is given in Fig. 5b with

$$F^{M_3}|_{t_1} = \left.\frac{-g_m^{M_{1a}} g_m^{M_{3a}} R_L}{g_m^{M_{1a}} + Y_{ds}^{M_{3a}} + 2Y_{neg}}\right|_{t_1} \tag{10}$$

$$F^{M_3}|_{\frac{T_{LO}}{2}} = 0 \tag{11}$$

$$F^{M_3}|_{t_3} = -F^{M_3}|_{t_1} \tag{12}$$

At (t_1, t_2), M_{2a}/M_{2b} are off and M_{1a}/M_{3a} and M_{1b}/M_{3b} (see Fig. 3(a)) forms a differential cascode common-source amplifier. At (t_3, t_4) M_{1a}/M_{1b} are off and M_{2a}/M_{3a} and M_{2b}/M_{3b} form a differential cascode common-source amplifier. At $\frac{T_{LO}}{2}$ M_{1a}/M_{2a} and M_{1b}/M_{2b} are on and there is no output due to the differential symmetry. This yields the voltage conversion gain

$$V_{gain} = \frac{2\sin(\alpha\pi)}{\pi^2\alpha} F^{M_3}|_{t_1} = \frac{2\sin(\alpha\pi)}{\pi^2\alpha} \left.\frac{-g_m^{M_{1a}} g_m^{M_{3a}} R_L}{g_m^{M_{1a}} + Y_{ds}^{M_{3a}} + 2Y_{neg}}\right|_{t_1} \tag{13}$$

Equation (13) shows that the conversion gain is increased under *partial* flicker noise cancelling condition ($G_{neg} \in \left[\frac{-g_{ds}^{M_{3a}} - g_m^{M_{1a}}}{2}, \frac{-g_{ds}^{M_{3a}}}{2}\right]$ and $C_{neg} \approx -0.5C_{tail}$). The reason for this increase is that G_{neg} increases the output impedance for the gm stage and as a result more RF signal current flows to the load R_{load}.

Fig. 6 shows the noise model for the mixer, where two non-correlated noise current $i_{tha}^{Y_{neg}}$ and $i_{thb}^{Y_{neg}}$ model the noise of Y_{neg}. Note that the noise of the negative impedance contributes to the mixer output by the same transfer function as the noise of M_{3a}/M_{3b}. Therefore, Y_{neg} only contributes to thermal noise while no flicker noise leaks to the output for a symmetric mixer. As a result, the mixer thermal noise is dominantly contributed by the thermal-noise folding of: M_{3a}/M_{3b}, M_{1a}/M_{1b}, M_{2a}/M_{2b},

the load R_{Load}, the input source impedance R_s and the negative impedance Y_{neg}. Assuming perfect input matching, the single-side band noise figure (NF) for high IF (thermal noise dominated) is then given by

$$NF_{SSB} \approx \frac{2S_{M3a,out} + 4S_{M1a,out} + S_{Rs,out} + S_{Yneg} + S_{Rload,out}}{0.5S_{Rs,out}} \tag{14}$$
$$= 2\frac{\left[\left(\frac{i_{th3a}}{g_{m3}}\right)^2 + 4\times\left(\frac{(g_{ds}^{M_{3a}} + 2G_{neg})i_{th1a}}{g_{m1}g_{m3}}\right)^2 + kTR_s + \left(\frac{i_{th}^{Y_{neg}}}{g_{m3}}\right)^2\right]\Bigg|_{t_1} + \frac{4kTR_{load}}{\left(1-\frac{4\alpha}{3}\right)\left|F^{M_3}|_{t_1}\right|^2}}{kTR_s}$$

where the five terms respectively account for the thermal noise from the transconductor stage M_{3a}/M_{3b}, the thermal noise from the switching stage (M_{1a}/M_{1b} and M_{2a}/M_{2b}), the thermal noise from the input source impedance R_s, the thermal noise from the negative impedance and the thermal noise from the load. Although the extra noise by Y_{neg} increases the thermal noise NF, due to the increased conversion gain (larger $F^{M_3}|_{t_1}$), the input referred noise due to the load R_{Load} is decreased. As a result, the thermal noise increase due to Y_{neg} can be small.

D. Negative impedance for IM3 distortion cancellation

It is shown in [7] that the IM3 of the time-varying mixer can be estimated by one time-invariant IM3 calculation at the maximum of the LO signal. The circuit model shown in Fig. 7 is now used to demonstrate the concept of using negative impedance for IM3 cancellation. When the LO signal reaches its positive maximum at t_1, M_{1a}/M_{1b} are fully on and M_{2a}/M_{2b} are fully off. The IM3 distortion current $i_{IM3}^{M_{1a}}$, $i_{IM3}^{M_{1b}}$, $i_{IM3}^{M_{3a}}$ and $i_{IM3}^{M_{3b}}$ are generated by the voltage swing across the transistor terminals. Given the differential circuit topology we can assume $i_{IM3}^{M_{1a}} = -i_{IM3}^{M_{1b}} = i_{IM3}^{M_1}$ and $i_{IM3}^{M_{3a}} = -i_{IM3}^{M_{3b}} = i_{IM3}^{M_3}$. For a first-order approximation, only the transconductance of M_1, M_2 and M_3, and the output admittance of M_3 are taken into account, which yields

$$v_{out}^{IM3} = \frac{-2g_m^{M_1}R_L}{g_m^{M_1}+Y_{ds}^{M_3}+2Y_{neg}} i_{IM3}^{M_3} + \frac{-2\left(Y_{ds}^{M_3}+2Y_{neg}\right)R_L}{g_m^{M_1}+Y_{ds}^{M_3}+2Y_{neg}} i_{IM3}^{M_1} \tag{15}$$

$$i_{IM3}^{M_3} = f_{IM3}^{M_3}\left(v_{gs}^{M_{3a}}, v_{ds}^{M_{3a}}\right) = f_{IM3}^{M_3}\left[\frac{v_{in}}{2}, \frac{-g_m^{M_3} v_{in}}{2\left(g_m^{M_1}+Y_{ds}^{M_3}+2Y_{neg}\right)}\right] \tag{16}$$

$$i_{IM3}^{M_1} = f_{IM3}^{M_1}\left(v_{gs}^{M_{1a}}, v_{ds}^{M_{1a}}\right) = f_{IM3}^{M_1}\left[\frac{g_m^{M_3} v_{in}}{2\left(g_m^{M_1}+Y_{ds}^{M_3}+2Y_{neg}\right)}, \frac{-g_m^{M_3}(-1+g_m^{M_1} R_L) v_{in}}{2\left(g_m^{M_1}+Y_{ds}^{M_3}+2Y_{neg}\right)}\right] \tag{17}$$

Equation (16) and (17) describe the fact that via transistor nonlinearity (denoted by the function f_d) the distortion current of a transistor is due to both the voltage swing across its gate-source and to its drain-source voltage swing (assuming the distortion related to the bulk-source voltage swing is insignificant).

For $G_{neg} \in \left[\frac{-g_{ds}^{M_{3a}} - g_m^{M_{1a}}}{2}, \frac{-g_{ds}^{M_{3a}}}{2}\right]$ and $C_{neg} \approx -0.5C_{tail}$,

- Eq. (16-17) show that the gate-source and drain-source voltage swing respectively for M_{1a} and M_{3a} have the same polarity. Thus $i_{IM3}^{M_3}$ and $i_{IM3}^{M_1}$ have the same polarity, given that both M_{1a} and M_{3a} are biased in the saturation region.
- Eq. (15) shows that the gain factor for distortion currents $i_{IM3}^{M_3}$ and $i_{IM3}^{M_1}$ have opposite signs. This enables cancellation of the distortion contributions caused by $i_{IM3}^{M_3}$ and $i_{IM3}^{M_1}$.

Equating (15) to zero gives that for a *complete* IM3 cancellation

$$\begin{cases} G_{neg} = -\frac{g_{ds}^{M_3}}{2} - \frac{g_m^{M_1} i_d^{M_3}}{2 i_d^{M_1}} \\ C_{neg} = -\frac{C_{tail}}{2} \end{cases} \tag{18}$$

Under *partial* IM3 cancelling condition ($G_{neg} \in \left[\frac{-g_{ds}^{M_{3a}} - g_m^{M_{1a}}}{2}, \frac{-g_{ds}^{M_{3a}}}{2}\right]$ and $C_{neg} \approx -0.5C_{tail}$), the distortion current polarity of each transistor within the mixer remains unchanged. For the switching stage (M_{1a}/M_{1b} and M_{2a}/M_{2b}), the negative impedance changes the amplifying factor of their distortion current from negative to positive. This enables the IM3 cancellation between the transconductor stage (M_{3a}/M_{3b}) and the switching stage (M_{1a}/M_{1b} and M_{2a}/M_{2b}). As the IM3 cancellation depends on the scaling and subtraction of distortion currents of the switching stage and g_m stage, we use Monte Carlo simulations to evaluate its sensitivity over device mismatches and process spread; the results are

shown in section IV. A.

E. Simulation verification

To illustrate the validity of the proposed theory of flicker noise and IM3 cancellation, in this section we show some simulation results for the mixer shown in Fig. 3a using an ideal negative resistance and an ideal negative capacitance in parallel to implement Y_{neg}. The bias and dimension condition for this mixer is the same as one (MixerD) that will be discussed in section III. In simulations, for 0.9GHz LO, we sweep the negative resistance while using a capacitance of -80fF.

Both simulated and calculated (using (5)-(8)) DSB NF in Fig. 8 (a) clearly show that either complete or partial cancellation of flicker noise can be achieved by using an ideal Y_{neg}. The sweet spot for *complete* flicker noise cancellation is by nature sensitive to device mismatch and PVT variations, illustrated by the notch around the optimum Y_{neg}=-950. *Partial* flicker noise cancellation is less sensitive to device mismatch and PVT variations: for this example, within $\pm$15% variation of Y_{neg} at the NF notch more than 20dB flicker cancellation is achieved. Due to some circuit analysis simplification in deriving (9), the optimal Y_{neg} for complete flicker noise according to (9) is somewhat different than actual (following from simulations) value. Fig. 8 (b) shows similar results for distortion cancellation, illustrating that IM3 distortion cancellation can be achieved using a properly designed Y_{neg} and illustrating that (15)-(18) provide a good prediction for the actual (simulated) IM3 distortion cancellation.

F. Summary

It can be concluded that a negative impedance ($G_{neg} \in \left[\frac{-g_{ds}^{M_{3a}}-g_m^{M_{1a}}}{2}, \frac{-g_{ds}^{M_{3a}}}{2}\right]$ and $C_{neg} \approx -0.5C_{tail}$) reduces the flicker noise leakage from the switching stage (M_{1a}/M_{1b} and M_{2a}/M_{2b}) by averaging out the flicker noise leakage transfer function. Note that this is very similar to flicker noise

suppression in chopper amplifiers [8]. Using a negative impedance, also the conversion gain is increased while the thermal noise may be slightly degraded. For a perfect symmetric mixer no flicker noise will be introduced by the negative impedance.

Using negative impedance in the specified range also enables partial IM3 cancellation between the transconductor stage (M_{3a}/M_{3b}) and the switching stage (M_{1a}/M_{1b} and M_{2a}/M_{2b}). The exact optimum of Y_{neg} is in general a little different for complete flicker noise cancellation and complete IM3 cancellation. Hence Y_{neg} can be designed for either full flicker noise/partial IM3 cancellation or full IM3/partial flicker noise cancellation.

III. Circuit Implementation

A. Circuit implementation of the negative impedance

To prove this flicker noise/IM3 cancellation concept, the circuit shown in Fig. 9 is implemented in a standard 0.16µm CMOS process. The negative impedance is implemented by the cross-coupled pair M_{4a}/M_{4b} with source degeneration provided by capacitor (C_s) and current source M_{5a}/M_{5b} [9-10]. The pMOS-based negative impedance enables dc current reuse of the negative impedance by the mixer's transconductor stage. As a first-order estimation, the value of the negative impedance --- taking only the transconductance of M_4 and M_5 and the output impedance of M_5 into account --- is:

$$\begin{cases} G_{neg} = -\dfrac{g_m^{M_4}\left[g_{ds}^{M_5}\left(g_{ds}^{M_5}+g_m^{M_4}\right)+\left(C_{ds}^{M_5}+2C_s\right)^2\omega^2\right]}{2\left[\left(g_{ds}^{M_5}+g_m^{M_4}\right)^2+\left(C_{ds}^{M_5}+2C_s\right)^2\omega^2\right]} \\ C_{neg} = -\dfrac{{g_m^{M_4}}^2\left(C_{ds}^{M_5}+2C_s\right)^2\omega}{2\left[\left(g_{ds}^{M_5}+g_m^{M_4}\right)^2+\left(C_{ds}^{M_5}+2C_s\right)^2\omega^2\right]} \end{cases} \quad (19)$$

Assuming $g_m^{M_4} \gg g_{ds}^{M_5}$, and denoting $\dfrac{g_m^{M_4}}{C_{ds}^{M_5}+2C_s} = \omega_t$, then for $\omega \ll \omega_t$ (19) reduces to

$$\begin{cases} G_{neg} \approx -\dfrac{g_m^{M_4}\left(\frac{\omega}{\omega_t}\right)^2}{2\left[1+\left(\frac{\omega}{\omega_t}\right)^2\right]} \approx -\dfrac{g_m^{M_4}}{2} \\ C_{neg} \approx -\dfrac{C_{ds}^{M_5}+2C_s}{2\left[1+\left(\frac{\omega}{\omega_t}\right)^2\right]} \approx -\dfrac{C_{ds}^{M_5}+2C_s}{2} \end{cases} \quad (20)$$

Equation (20) shows that the Y_{neg} for either full flicker noise cancellation or full IM3 cancellation can be obtained by setting a suitable value both for the transconductance of M_4 and for the degeneration capacitance C_s. For minimal chip area, two anti-parallel poly-diffusion capacitors are used for C_s instead of a fringe capacitor.

Equation (20) also shows that the implemented Y_{neg} is frequency dependent: the negative conductance (G_{neg}) has a high-pass characteristic while the negative capacitance (C_{neg}) presents a low-pass behavior. Consequently, using this Y_{neg}-circuit the optimization for either flicker noise cancellation or for IM3 cancellation is frequency-dependent. In order to demonstrate the effect of the frequency-dependency of the Y_{neg} circuit, Fig. 10 shows simulation results for one of the designed mixer circuits in section III: MixerD, which is designed for full IM3 cancellation and partial flicker noise cancellation at 0.9GHz. Design details of MixerD is shown in section III. B.

Fig. 10 (a) shows IIP3 as a function of the LO frequency, swept from 0.1GHz to 2GHz. The IIP3 peak around 0.9GHz shows that Y_{neg} circuit is optimized for this frequency. For higher frequencies, the IM3 cancellation degrades, mainly due to the less negative capacitance provided by the Y_{neg} circuit with increasing frequency. As a result, the phase difference between the distortion currents of the switching stage and of the gm stage then deviates from 180 degrees. For LO frequencies lower than 0.8GHz, the distortion cancellation remain effective since parasitics has less effect. Fig. 10 (b) shows that the Y_{neg} circuit achieves a complete flicker noise cancellation at around 0.2GHz and that only partial flicker noise cancellation is achieved at higher frequencies.

In summary, the G_{neg} and C_{neg} provided by our Y_{neg} circuit is frequency-dependent. As a result, a complete IM3 distortion or a complete flicker noise cancellation provided by the circuit implementation shown in Fig. 8 is narrowband. Tuning the bias of the Y_{neg} circuit and using tunable capacitors for Cs, a tunable negative impedance can be provided by the Y_{neg} circuit for various frequencies which may enable complete IM3 distortion or complete flicker noise cancellation for multiband applications. However, this is not implemented in this paper.

B. Two prototype chips

Our active mixer circuits use load ressitors R_{load}. It is frequently assumed that a poly-silicon resistor has negligible flicker noise [1, 6] which assumption is valid for many conventional circuits. However, in this paper the aim is at very low flicker noise mixers. The work in [11] shows that the traps at the silicon grain boundaries in the poly-silicon cause some flicker noise, resulting in a flicker noise current given by $S_i = \frac{\beta I^2}{WL} \cdot \frac{1}{f}$, where β is a constant including technology-dependent data and temperature, I is the DC current through the resistor, and W and L are the resistor width and length respectively. Simulation results in Fig. 11 show that without mismatch and with metal resistors, the mixer noise output only contains thermal noise (denoted by "Nominal mixer noise with MetalRload"). Including mismatch and with metal resistors, the mixer flicker noise frequency corner is below 1kHz. Using poly resistors, even in the nominal case without any mismatch, the flicker noise of the poly-silicon resistor is dominant compared to the mixer thermal noise unless large silicon area (larger than 2100 um^2) is used. Therefore, in our design a serpentine metal resistor consisting four stacked metal layers (M1-M4) with a total area of 370 um^2 is used to be able to prove our concept properly.

Using the topology shown in Fig. 9 we designed two chips. One (MixerD) is optimized for full

IM3 cancellation and partial flicker noise cancellation using the process's nominal supply voltage ($V_{DD,NOM}$ =1.8V). To show the robustness of the proposed flicker noise cancellation technique under the constraint of low supply voltage, a second chip (MixerNF) is optimized for full flicker noise cancellation and partial IM3 cancellation using $0.67\times V_{DD,NOM}$ (1.2V). The main design parameters of both circuits are listed in Table I. Since flicker noise is mainly a problem for narrowband system, the two mixer chips are designed for 0.9GHz. Two off-chip baluns are used to generate the differential RF input and differential clock, respectively. The external differential clock signal and an on-chip LO buffer provides the LO for mixer.

C. Comparison with other techniques

Due to the similar topology appearance, our mixer in Fig. 9 is compared with previous techniques of flicker noise reduction. In [1] the cross-coupled pair M_{4a}/M_{4b} shown in Fig. 12a provides a dynamic current into the transconductor stage at the LO zero-crossings (at $\frac{T_{LO}}{2}$). As a result, at $\frac{T_{LO}}{2}$ the current through the switching pair and the transconductance of the switching pair is reduced. This enables a smaller $v_{fl,out}^{M_{1a}}\Big|_{\frac{T_{LO}}{2}}$ in (5) and consequently yields flicker noise reduction. The cross-coupled pair M_{4a}/M_{4b} turns on only around $\frac{T_{LO}}{2}$ and remains off during the remainder of the LO period, which requires a high LO voltage swing and low R_{load} (50 ohm in [1]). To tune out the parasitic capacitance of the cross-coupled pair M_{4a}/M_{4b}, an inductor is added to the cross-coupled pair M_{4a}/M_{4b} as shown in Fig. 12b in [2]. Although these dynamic bleeding techniques [1-2] and our mixer all use the cross-coupled pair M_{4a}/M_{4b}, there are a number of fundamental differences:

- The cross-coupled pair M_{4a}/M_{4b} in the dynamic bleeding technique only operates around $\frac{T_{LO}}{2}$, while in our mixer the negative impedance is operational during the total LO period. As a result, our mixer only needs normal LO voltage swing, while high LO voltage swing is required in the

dynamic bleeding technique, which may impose linearity degradation due to the switching pair (see [7]).

- The cross-coupled pair M_{4a}/M_{4b} in the dynamic bleeding technique is designed as a DC current injector rather than a negative resistor. Flicker noise leakage due to the finite transconductor output resistance is not addressed. The source degenerated capacitance together with the cross-coupled pair M_{4a}/M_{4b} in this paper are designed as a negative impedance, which fully addresses the flicker noise leakage.

Based on the analysis in section II, in fact the mixer in Fig.12b can be made to act in the same way as our mixer if the cross-coupled pair M_{4a}/M_{4b} is designed to operate during the whole LO period: the cross-coupled pair together with the inductor in [2] is equivalent to the negative impedance proposed in our work. However, full flicker noise cancelling was not done in [2].

IV. SIMULATION AND MEASUREMENT

The microphotograhps of two demonstrator mixer chips (MixerD and MixerNF) are shown in Fig. 13. The active area of the LO buffer and mixer with decap is $0.0156mm^2$ for MixerD, of which 8.2% is occupied by the Y_{neg} circuit. In MixerNF the Y_{neg} circuit consumes 7.1% of the total active area ($0.014mm^2$). The packaged chips were measured on PCB boards for 0.9GHz LO and 0.92GHz RF. The noise is measured by an Agilent E5500 noise measurement set-up. For noise at IF<1MHz a SRS preamplifer is used to connect the mixer output with the noise set-up; for noise at IF>1MHz, a LeCroy AP033 active probe was used connecting the mixer output with the noise measurement set-up.

A. Mixer with full-IM3/partial-flicker-noise cancellation

For the mixer optimized for full IM3 cancellation and partial flicker noise cancellation (MixerD), the bias current of Y_{neg} (I_{Yneg} shown in Fig. 9) is swept within $\pm$45% variation of the optimal value to

demonstrate the robustness against process spread. The measured and simulated results are shown in Fig.14 as a function of the bias current normalized to the optimal value (NI_{Yneg}). At the optimal bias value (NI_{yneg}=1), a measured improvement of 10dB for IIP3, 5dB for conversion gain, 9dB for DSB NF@1kHz, and 1dB for input P_{1dB} are achieved compared to the same mixer without Y_{neg}. The DSB NF@10MHz degrades by 0.1dB. The mixer DC current increases from 9.2mA to 10.7mA due to the biasing of the Y_{neg} circuitry, while the LO buffer current (16mA) stays unchanged. Within ±45% variation of I_{Yneg}, >5dB gain improvement, >6dB NF@1kHz reduction, <0.2dB thermal NF degradation, no input P_{1dB} degradation are achieved. Fig. 14b shows the flicker NF reduction at a very low frequency (1 kHz), where the flicker noise is dominant and the thermal noise can be neglected. Fig.15 shows the measured fundamental and IM3 output at the optimal bias value (NI_{Yneg}=1). Due to higher-order nonlinearity distortion introduced by Y_{neg}, the IM3 curve start to show 5th order behavior for Pin >-18dBm. The measured mixer DSB NF is shown in Fig. 16. The spikes are from the equipment power supply and the measurement setup. Although Y_{neg} introduces 5dB thermal noise to the mixer, 5dB more gain also provided by Y_{neg} lowers the input-referred noise of the R_{load} by 5dB and results in overall less than 0.1dB degradation in the thermal noise figure. The flicker noise corner frequency decreases from 100kHz to 20kHz.

Simulated and measured effects of mismatch and process spread on NF and IIP3 of MixerD are shown in Fig. 17. The results of a 200-time Monte Carlo simulation using a realistic production variation model for device mismatches and process spread, in Fig. 17a, show a mean DSB NF@1kHz of 19.2dB (nominally 19dB) which is about 7dB lower than the mixer without Y_{neg}, while the measurements of ten dies from one wafer show +7dB NF reduction at 1kHz in Fig. 17b. Note that such a high NF is not the result a badly designed mixer but is due to the very low frequency (1kHz),

where the flicker noise is significant. In comparison, the measured NF@1kHz of the low-flicker-noise mixer in [2] is 29dB. In Fig. 17c a 200-time Monte Carlo simulation shows a mean IIP3 of 10.8dBm (nominally 12dBm) which is 9dB higher than the mixer without Y_{neg}, whereas more than 6dB IIP3 improvement is measured in ten dies from one wafer as shown in Fig. 17d. For the temperature range [-40°C to 80°C] in the nominal corner, simulations show >6.7dB flicker NF reduction in Fig. 18a; the IM3 cancellation becomes less effective as the temperature increases as shown in Fig. 18b. We did not implement a control loop to adjust the negative impedance over temperature; the realized chips aim to prove the principle of flicker noise and distortion cancellation.

B. Mixer with full-flicker-noise / partial-IM3 cancellation

For the mixer optimized for full flicker noise cancellation (MixerNF), Fig.19 shows the measured and simulated results as a function of the bias current for Y_{neg} normalized to the optimal value (NI_{Yneg}). When Y_{neg} is not enabled, MixerNF has about 5dB less gain compared with MixerD. There is less voltage swing across the transistors' terminals resulting less distortion and hence higher IIP3. At the optimal bias value (NI_{yneg}=1) a measured improvement of 8dB for DSB NF@1kHz, 1.4dB for conversion gain, 0.1dB for the DSB NF@5MHz and 2.5dB for input P_{1dB} are achieved compared to the same mixer without Y_{neg}. The mixer DC current increases by 4% due to the biasing of the Y_{neg} circuitry, while the LO buffer current (4.8mA) stays unchanged. The difference between the measured and simulated IIP3 shown in Fig. 19d may be due to the fact that this mixer is operated at low supply voltage ($0.67\times V_{DD,NOM}$), where the headroom for the Y_{neg} circuit is insufficient to provide a robust IM3 cancellation. Full flicker noise cancellation at the optimal bias value (NI_{yneg}=1) shown in Fig. 19(a) suggested by simulation is not found in measurement, probably due to external low-frequency noise contributed by the measurement set-up and due to the LO phase noise leakage resulting from

mismatches in the mixer. However, Fig. 19a shows that more than 10dB improvement for the flicker NF can be achieved for very broad bias range (for NI_{Yneg}>1.75). The robustness of this flicker noise cancellation under low supply voltage is estimated for NI_{Yneg}=2 in MixerNF. Fig. 20a shows the results of a 200-time Monte Carlo with mismatch and process spread, indicating a mean DSB@1kHz of 21.9dB (nominally 20dB) which is 15dB lower than in the mixer without Y_{neg}; measurements on ten dies shows more than 11dB flicker NF reduction, see Fig. 20b. For the temperature range [-40°C to 80°C] in the nominal corner, simulations shows more than 14dB flicker NF reduction, see Fig. 21. The measured mixer noise output is shown in Fig. 22 (for Y_{neg} biased at NI_{yneg}=2). The flicker corner frequency decreases from 200kHz to 20kHz; the rolling-off behavior for IF>5MHz is due to the IF filter in the measurement setup.

C. Benchmarking

The mixer with full-IM3/partial-flicker noise cancellation (MixerD) presented in this paper is compared with previous works on flicker noise reduction [1-4] in Table II. Since the flicker NF value depends on a few factors such as circuit bias and technology-related flicker noise corner, our technique is compared with previous works in term of the value of flicker noise reduction. It shows that the presented technique provides very good flicker NF reduction, while at the same time it achieves the largest improvement in IIP3 and gain without using on-chip inductors or high supply voltages or increasing the LO power. In conclusion, this flicker noise/IM3 cancellation provides solutions for reducing flicker noise and improving linearity of CMOS active mixers.

V. CONCLUSION

A new technique providing simultaneous cancellation of flicker noise and IM3 distortion for active mixers is presented without using on-chip inductors or high supply voltages or increasing the

LO power. By using a negative impedance (Y_{neg}), the flicker noise leakage from the switching pairs is minimized. Meanwhile the negative impedance enables IM3 distortion cancellation between the switching pairs and the transconductor stage, which yields overall IM3 improvement. The techniques also improve the conversion gain while it has little effect on the thermal noise. For the demonstrator mixer chip optimized for full-IM3/partial-flicker-noise cancellation, 9dB flicker noise suppression, 10dB improvement for IIP3, 5dB improvement for conversion gain and 1dB improvement for input P_{1dB} are achieved. The Y_{neg} circuit increases the thermal NF by 0.1dB, power consumption by 16% and active area by 8%. Under mismatch and process spread, a 200-time Monte Carlo simulation shows 7dB reduction in mean NF@1kHz and 9dB increase in mean IIP3. A ten-sample measurement shows over 7dB reduction in NF@1kHz and more than 6dB increase in IIP3. Simulations indicate that the flicker noise cancellation is not very sensitive to temperature variation [-40^{o}C to 80^{o}C], while the IM3 cancellation degrades as the temperature increases. For the demonstrator mixer chip optimized for full-flicker-noise/partial-IM3 cancellation under low supply voltage ($0.67\times V_{DD,NOM}$), more than 10dB flicker noise suppression is measured within $\pm$200% variation of the negative impedance bias current. The ten-sample measurement shows over 11dB flicker NF reduction, and the simulation shows more than 14dB flicker NF reduction for the temperature range [-40^{o}C to 80^{o}C].

Acknowledgements:

We thank NXP Semiconductors for chip fabrication, and G. van der Weide, M. C. M. Soer and H. de Vries for their help.

APPENDIX

The real part of (6) is given by

$$Re\left(v_{fl,out}^{M_{1a}}\Big|_{t_1}\right)=\frac{-g_m^{M_{1a}}R_L\left[G^{M_3}\left(g_m^{M_{1a}}+G^{M_3}\right)+\left(\omega_{LO}C^{M_3}\right)^2\right]v_{fl,in}^{M_{1a}}}{\left(g_m^{M_{1a}}+G^{M_3}\right)^2+\left(\omega_{LO}C^{M_3}\right)^2} \quad \text{(A1)}$$

where $G^{M_3}=g_{ds}^{M_{3a}}+2G_{neg}$ and $C^{M_3}=C_{tail}+2C_{neg}$.

When $$\begin{cases} G_{neg}>\frac{1}{4}\left(-2g_{ds}^{M_{3a}}-g_m^{M_{1a}}-\sqrt{{g_m^{M_{1a}}}^2-(2\omega_{LO}C^{M_3})^2}\right) \\ G_{neg}<\frac{1}{4}\left(-2g_{ds}^{M_{3a}}-g_m^{M_{1a}}+\sqrt{{g_m^{M_{1a}}}^2-(2\omega_{LO}C^{M_3})^2}\right) \end{cases} \quad \text{(A2)}$$

the real part of (6) is positive. For $C_{neg}\approx -0.5C_{tail}$, $C^{M_3}\approx 0$ and (A2) can be simplified to

$$\frac{-g_{ds}^{M_{3a}}-g_m^{M_{1a}}}{2}<G_{neg}<\frac{-g_{ds}^{M_{3a}}}{2} \quad \text{(A3)}$$

Therefore, for $G_{neg}\in\left[\frac{-g_{ds}^{M_{3a}}-g_m^{M_{1a}}}{2},\frac{-g_{ds}^{M_{3a}}}{2}\right]$ the real part of (6) is positive.

REFERENCES

[1] H. Darabi and J. Chiu, "A noise cancellation technique in active RF-CMOS mixers," *IEEE J. Solid-State Circuits,* vol. 40, pp. 2628-2632, Dec. 2005.

[2] J. Yoon, H. Kim, C. Park, J. Yang, H. Song, S. Lee and B. Kim, "A new RF CMOS Gilbert mixer with improved noise figure and linearity," *IEEE Trans. Microwave Theory and Techniques,* vol. 56, pp. 626-631, Mar. 2008.

[3] R. S. Pullela, T. Sowlati and D. Rozenblit, "Low flicker-Noise quadrature mixer topology," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* San Francisco, CA, 2006, pp. 1870 - 1879.

[4] J. Park, C. H. Lee, B.-S Kim and J. Laskar, "Design and analysis of low flicker-noise CMOS mixers for direct-conversion receivers", *IEEE Trans. Microwave Theory and Techniques,* vol. 54, pp. 4372-4380, Dec. 2006.

[5] B. Razavi, "Design considerations for future RF circuits", *Proc. IEEE ISCAS*, May 2008.

[6] H. Darabi and A. A. Abidi, "Noise in RF-CMOS mixers: a simple physical model," *IEEE J. Solid-State Circuits,* vol. 35, pp. 15-25, Jan. 2000.

[7] W. Cheng, A. J. Annema, J. A. Croon and B. Nauta, "Noise and nonlinearity modeling of active mixers for fast and accurate estimation", *IEEE Trans. Circuits and Systems I,* vol. 58, pp. 276-289, Feb. 2011.

[8] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1615, Nov. 1996.

[9] C. Tilhac, S. Razafimandimby, A. Cathelin, S. Bila, V. Madrangeas and D. Belot, "A Tunable bandpass BAE-filter architecture using negative capacitance circuitry," *IEEE Radio Frequency integrated Circuits (RFIC)Symposium,* pp.605 – 608, 2008.

[10] J. C. Zhan, K. Maurice, J. Duster and K. T. Kornegay, "Analysis and design of negative impedance LC oscillators using bipolar transistors," *IEEE Trans. Circuits and Systems I,* vol. 50, pp. 1461-1464, Nov. 2003.

[11] R. Brederlow, W. Weber, C. Dahl, D. Schmitt-Landsiedel and R. Thewes, "Low-frequency noise of integrated poly-silicon resistors," *IEEE Trans. Electron Devices,* vol. 48,nl.6, pp. 1180-1187, Nov. 2001.

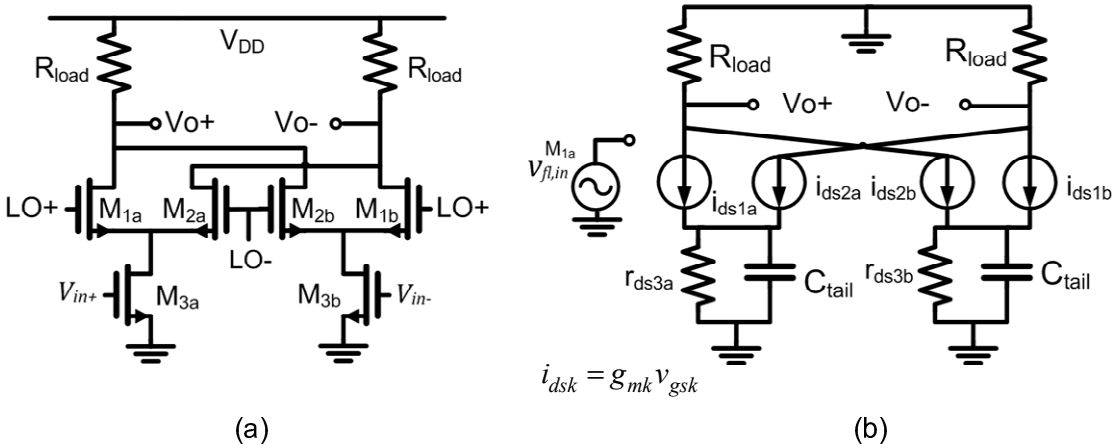

Fig. 1. (a) Schematic and (b) time-varying noise model of the double-balanced Gilbert mixer.

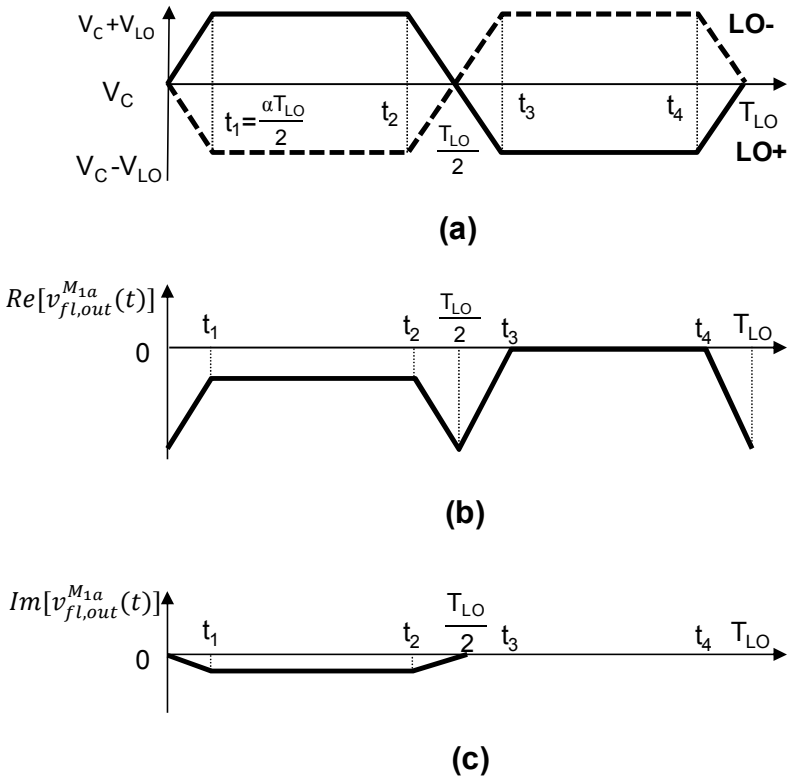

Fig. 2. (a) Waveform of the LO signal, (b) and (c): approximation of the real and imaginary part of $v_{fl,out}^{M_{1a}}(t)$ respectively.

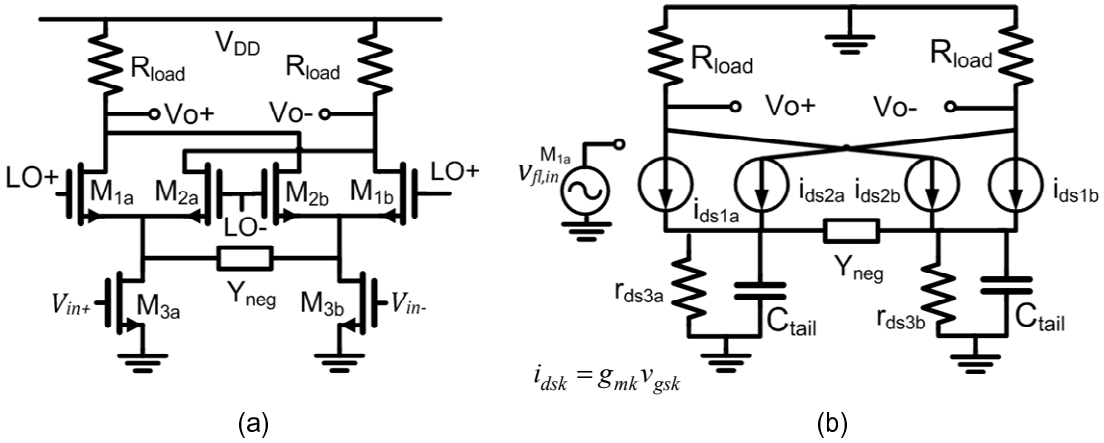

Fig. 3. (a) Schematic and (b) time-varying noise model for the mixer with a negative impedance for flicker noise cancellation.

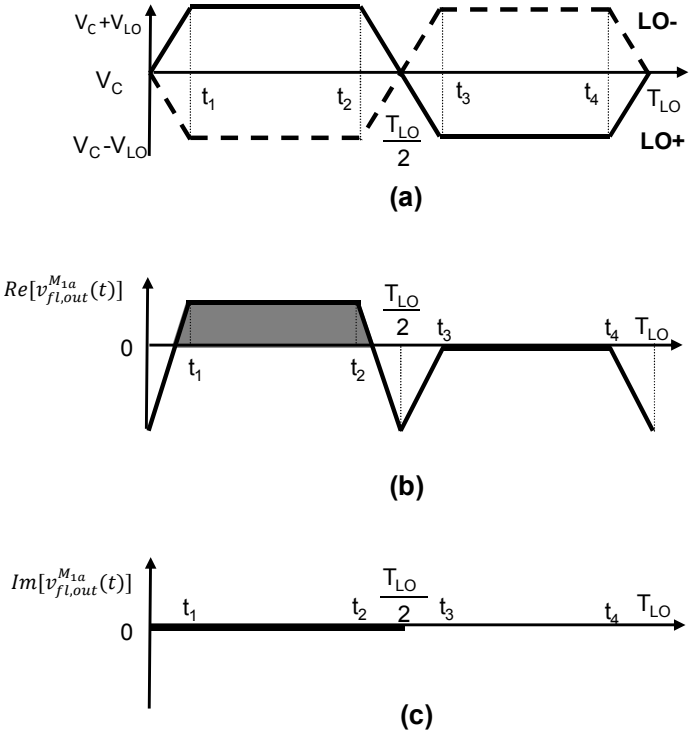

Fig. 4. (a) Waveform of the LO signal. (b) and (c): approximation of the real respectively imaginary part of $v_{fl,out}^{M_{1a}}(t)$ using a negative impedance for flicker noise cancellation.

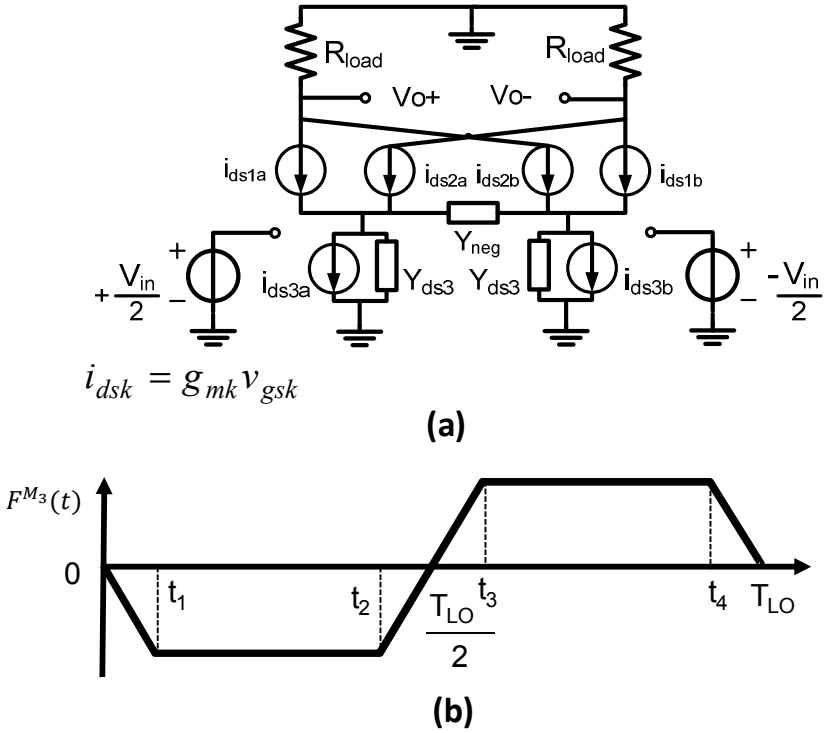

Fig. 5. (a) Time-varying linear model for calculating the voltage gain of the mixer with a negative impedance for flicker noise cancellation and (b) the approximation for the instantaneous voltage gain $F^{M_3}(t)$.

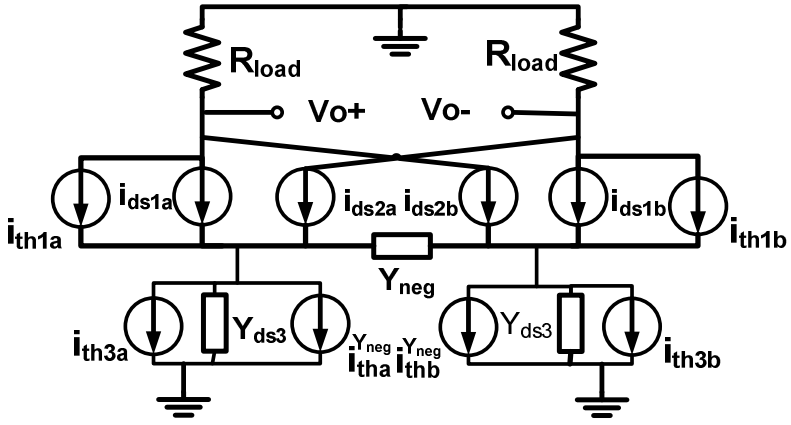

Fig. 6. Time-varying noise model for calculating the thermal noise of the mixer with a negative impedance.

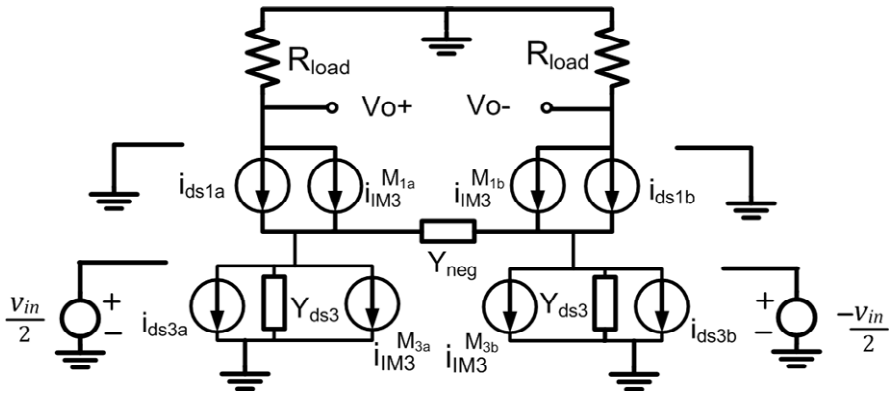

Fig. 7. Circuit model for the mixer distortion analysis.

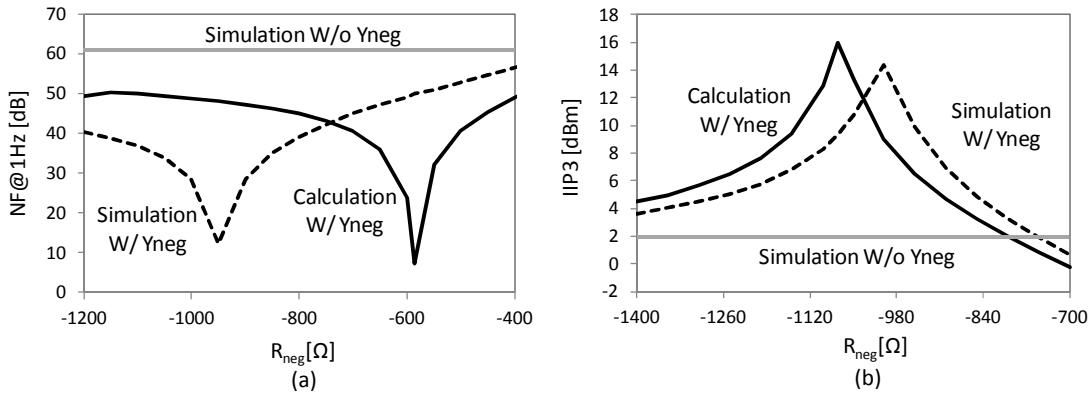

Fig. 8. Simulated and calculated (a) NF at 1Hz and (b) IIP3 as a function of the negative resistance for the mixer shown in Fig. 3(a) at an LO of 0.9GHz.

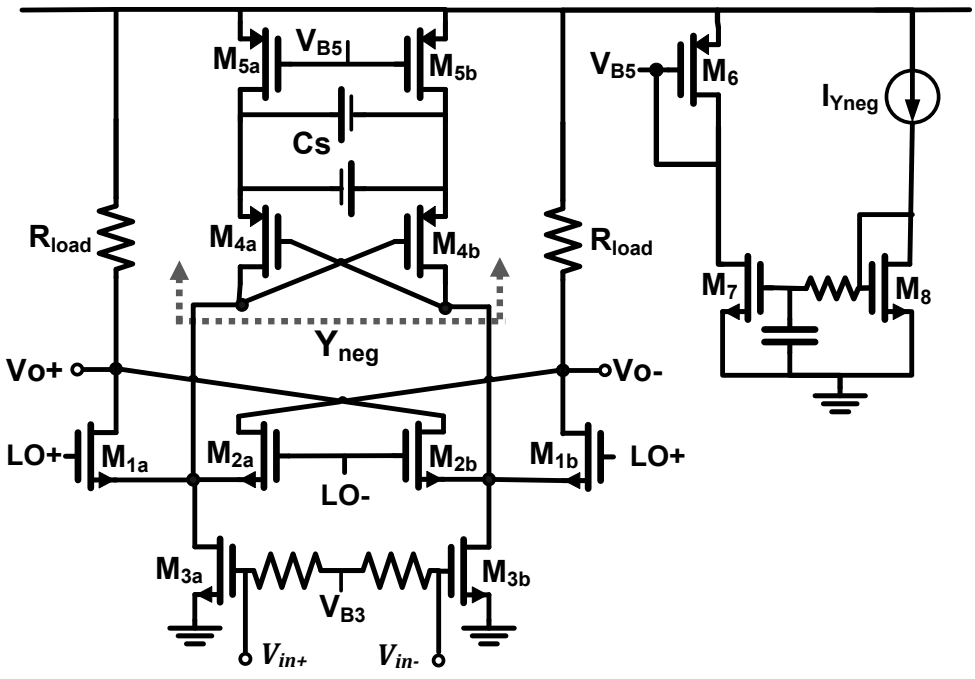

Fig. 9. The schematic of the mixer with a negative impedance Y_{neg}.

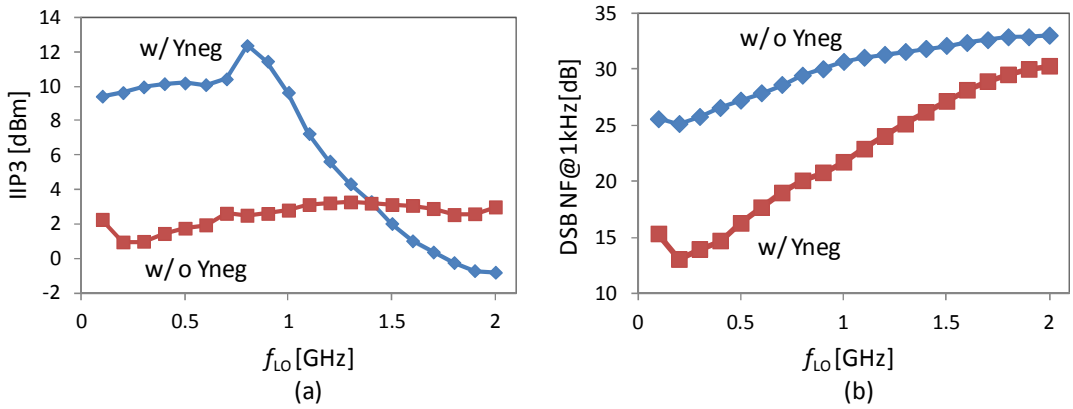

Fig. 10. The simulated (a) IIP3 and (b) DSB NF at 1kHz as a function of LO frequency for MixerD with and without using the negative impedance. MixerD is designed for full IM3 cancellation and partial flicker noise cancellation at 0.9GHz LO.

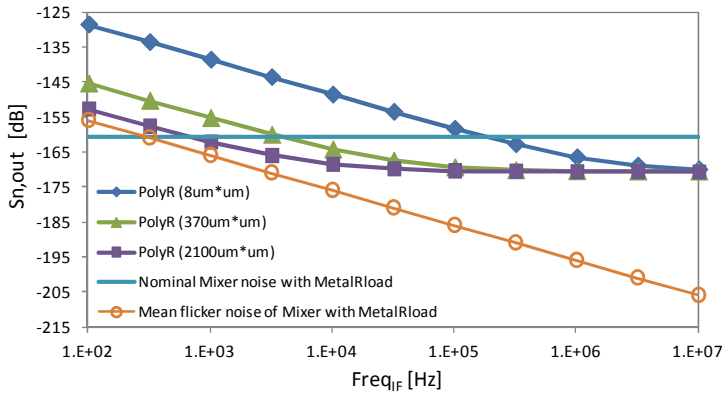

Fig. 11. The simulated output noise of the mixer using poly-silicon resistor and metal resistor as R_{load}.

Table I: Main design parameters for two prototype chips (MixerD and MixerNF)

Chip name	W/L [μm] (M_1/ M_2)	W/L [μm] (M_3)	W/L [μm] (M_4)	W/L[μm] (M_5)	R_{load} [Ω]	C_s [pF]	V_{dd} [V]
MixerD	100/0.16	80/0.16	80/0.16	104/0.16	250	1.2	1.8
MixerNF	108/0.16	72/0.16	68/0.18	68/0.18	250	0.8	1.2

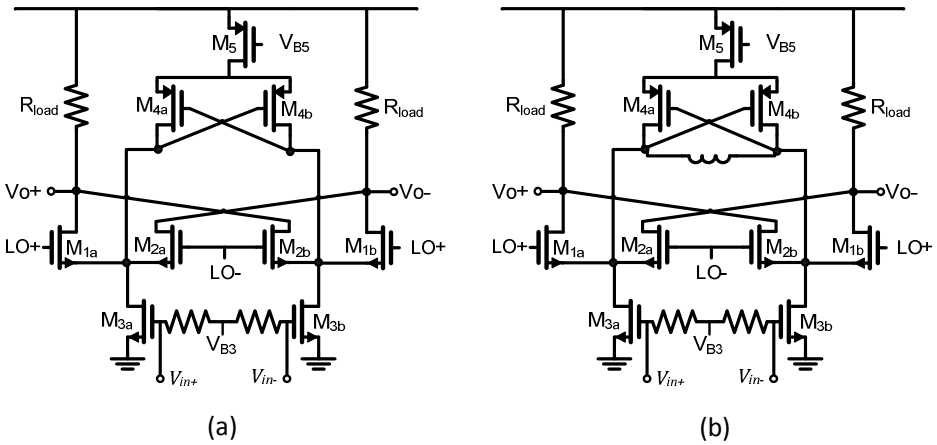

Fig. 12 Two mixers for flicker noise reduction. a) Dynamic bleeding [1], b) Dynamic bleeding with a inductor [2].

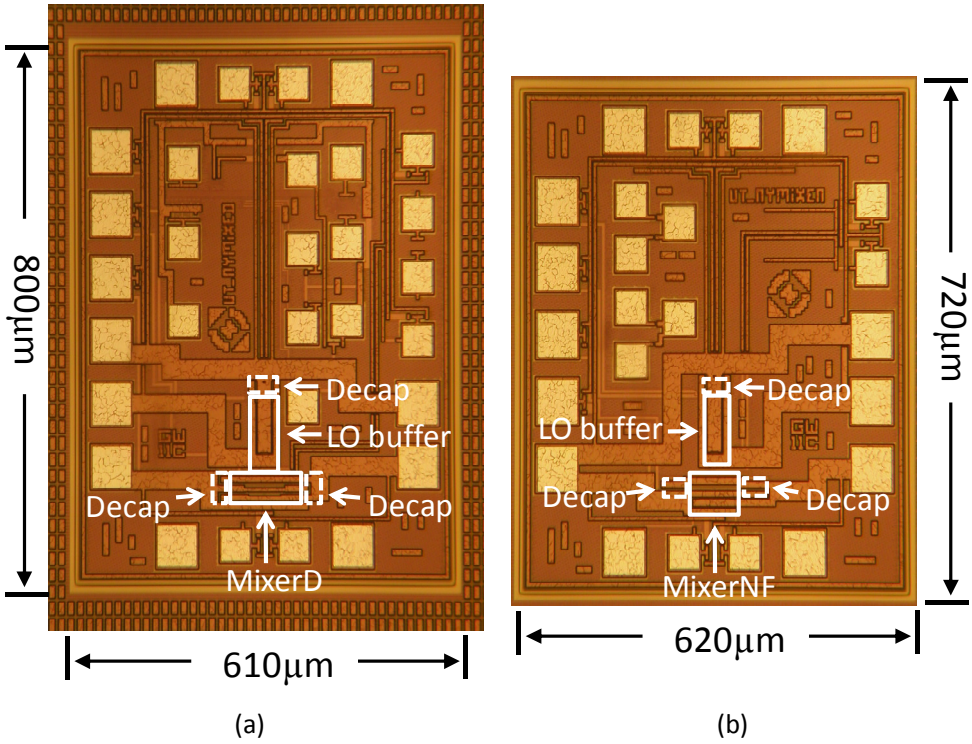

Fig. 13. Chip photo of (a) MixerD and (b) MixerNF.

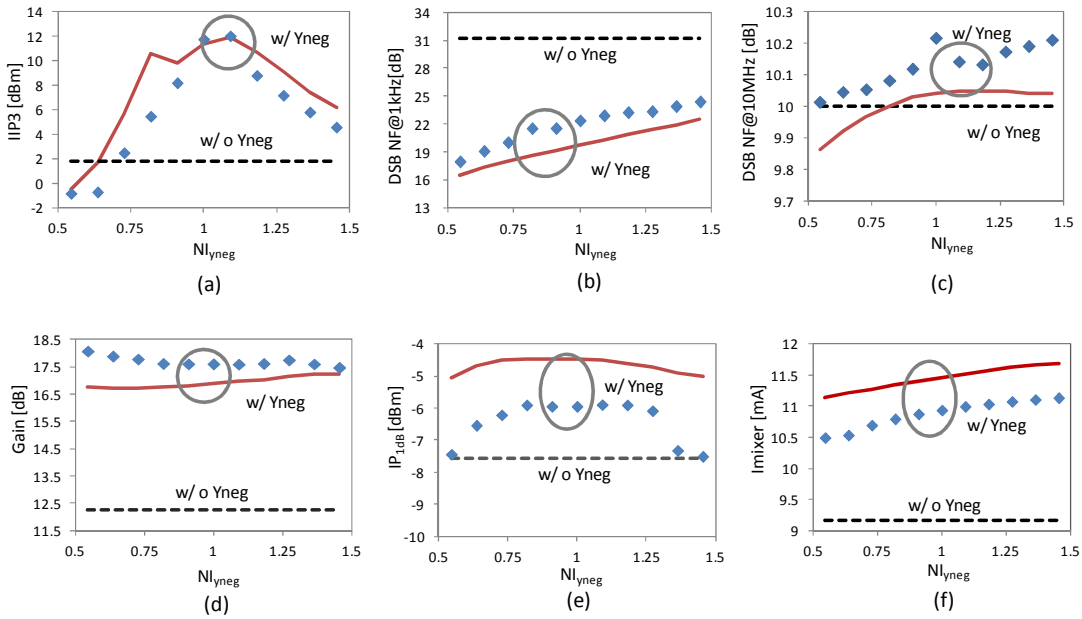

Fig. 14. IIP3, NF, conversion gain, input P_{1dB} and dc current taken by the mixer as a function of the normalized bias current of Y_{neg} for MixerD. Solid line for simulated results and symbol for measured results of the mixer with Y_{neg}. Dashed line for measured results of the mixer without Y_{neg}.

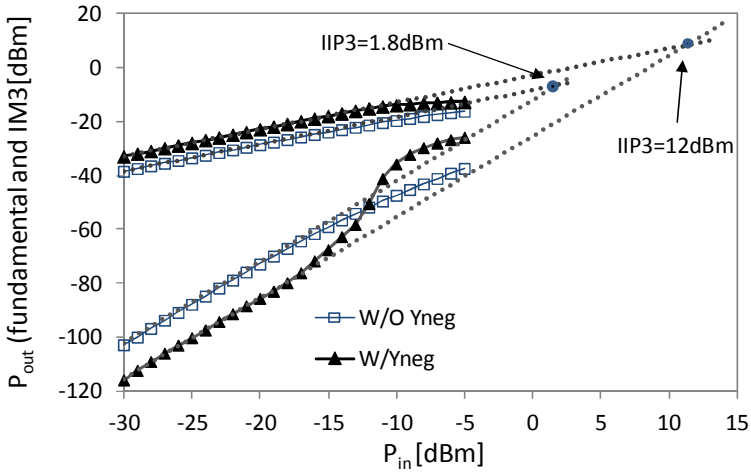

Fig. 15. Measured fundamental and IM3 output vs input power P_{in} for MixerD.

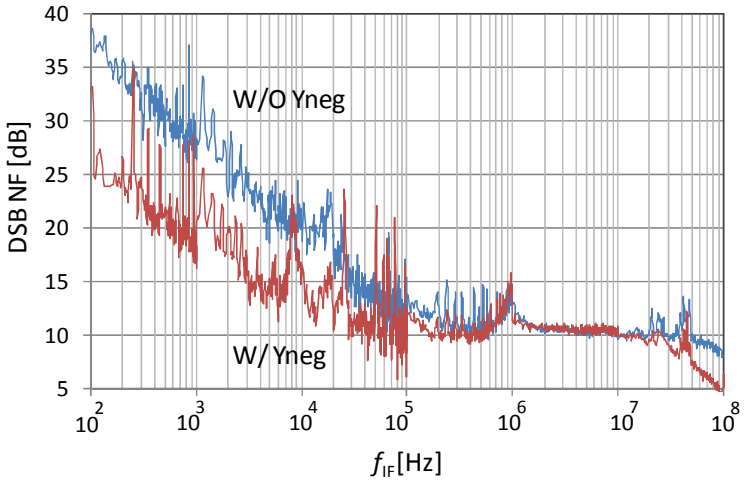

Fig. 16. Measured DSB NF for mixer (MixerD) with and without using Y_{neg}.

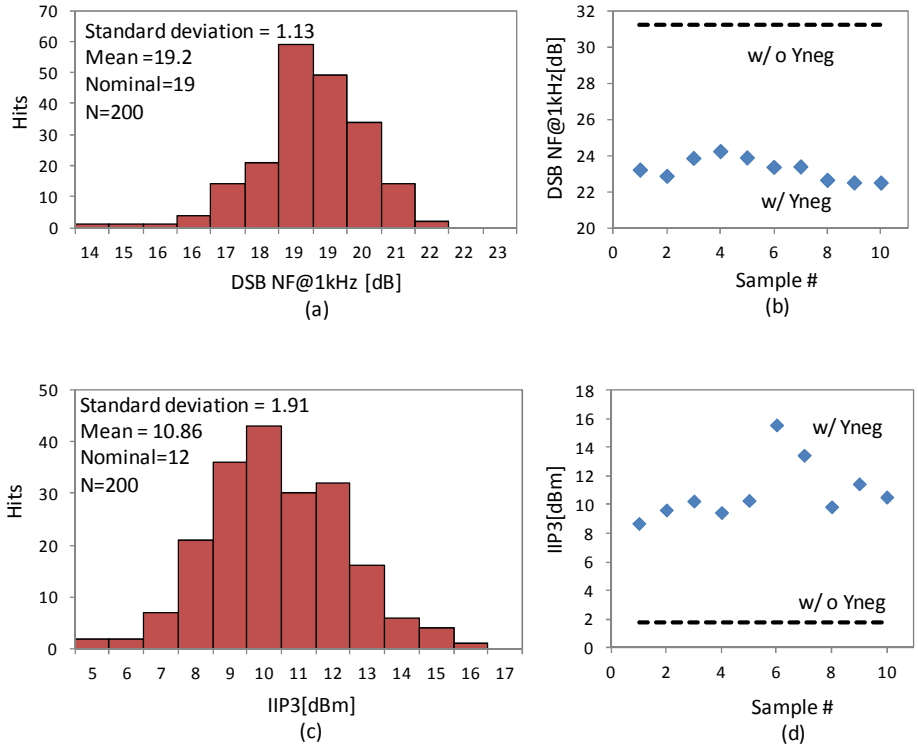

Fig. 17. Effect of mismatches and process spread on NF and IIP3 of MixerD with Y_{neg} (NI_{Yneg}=1). (a) 200-time Monte Carlo simulation results of DSB NF@1kHz (b) measured DSB NF@1kHz of ten dies, (c) 200-time Monte Carlo simulation results of IIP3, (d) measured IIP3 of ten dies. Symbol for measured results of the mixer with Y_{neg}. Dashed line for measured results of one mixer sample without Y_{neg}.

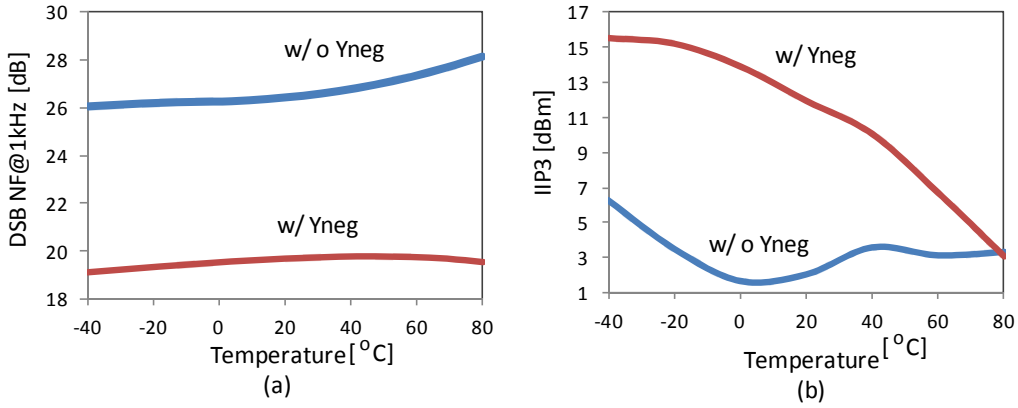

Fig. 18. Simulated NF and IIP3 for mixer (MixerD) with and without using Y_{neg} as a function of temperature.

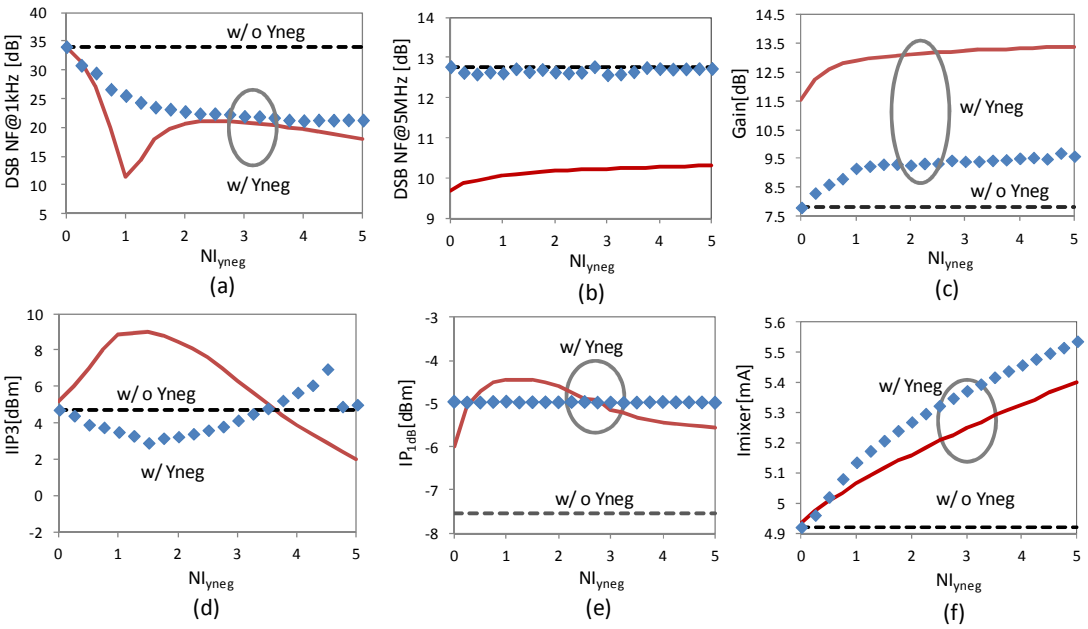

Fig. 19. NF, IIP3,conversion gain, input P_{1dB} and dc current taken by the mixer as a function of the normalized bias current of Y_{neg} for MixerNF. Solid line for simulated results and symbol for measured results of the mixer with Y_{neg}. Dashed line for measured results of the mixer without Y_{neg}.

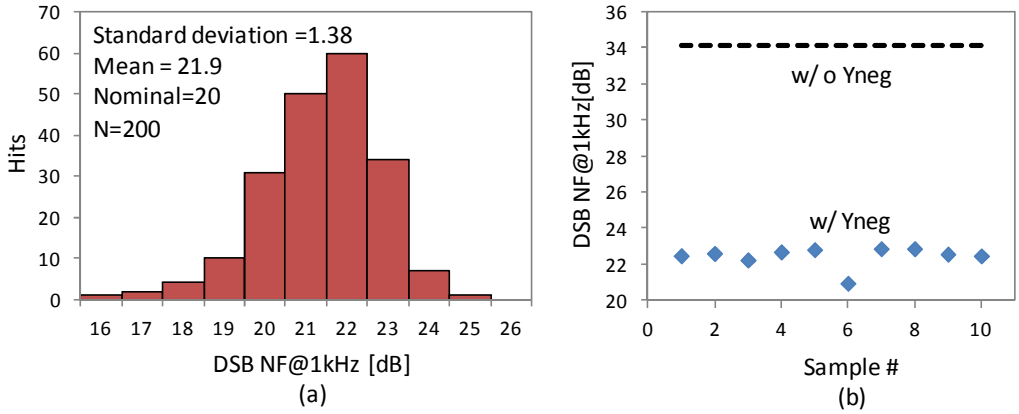

Fig. 20. (a) 200-time Monte Carlo simulation results of DSB NF@1kHz for MixerNF (NI_{yneg}=2). (b) Measured DSB NF@1kHz for MixerNF (NI_{yneg}=2) of ten dies.

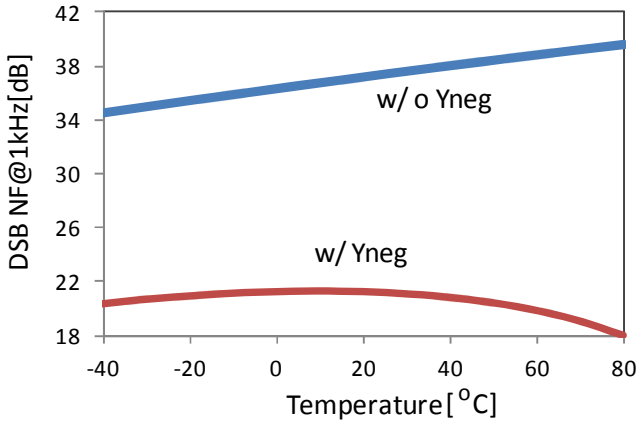

Fig. 21. Simulated NF for mixer (MixerNF) with and without using Y_{neg} as a function of temperature.

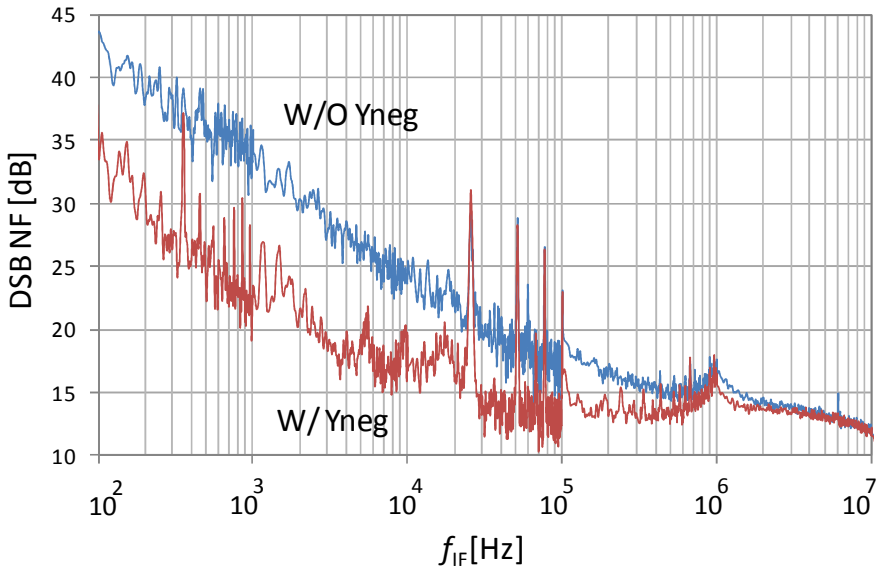

Fig. 22. Measured DSB NF for mixer with and with using Y_{neg} for MixerNF (NI_{yneg}=2).

Table II. Comparison of techniques for flicker noise reduction in CMOS active mixers.

		Darabi[1]	Yoon[2]	Park[4]	Pullela[3]	This work
CMOS		0.13μm	0.13μm	0.18μm	0.13μm	0.16μm
V_{DD} [V]		1.2	1.5	1.8	2.7	1.8
Freq [GHz]		2	2.4	5.2	1.96	0.9
Inductor Number		0	1	2	0	0
Flicker NF reduction [dB]		7@10kHz	7.5@10kHz	7@10kHz	9.5@10kHz	9@1kHz
Flicker NF @10kHz [dB]	w/o cancelling	21.8	37	27	18	20
	w/ cancelling	14	29	20	8.5	13
Gain Improvement [dB]		0.5	1.3	6	2	5
Gain [dB]	w/o cancelling	0	10.1	9.3	5	12.3
	w/ cancelling	0.5	11.4	16.2	7	17.6
Thermal NF changes∗ [dB]		0	0	0	-2	+0.1
Thermal NF @10MHz [dB]	w/o cancelling	12	7.5#	10	8.5	10
	w/ cancelling	12	7.5#	10	6.5	10.1
IIP3 improvement [dB]		0	1.6	0	1	10
IIP3 [dBm]	w/o cancelling	10.5	3.8	-4	1	1.8
	w/ cancelling	10.5	4.4	-5	2	11.8
Bias current increases		0%	0%	0%	N/A	16%
Bias current [mA]	w/o cancelling	2	6	3.9	3	9.2
	w/ cancelling	2	6	3.9	3	10.9

∗ "+" for NF increases and "–" for NF decreases.