Tuning a racetrack ring resonator by an integrated dielectric MEMS cantilever

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Abstract: The principle, fabrication and characterization of a dielectric MEMS cantilever located a few 100 nm above a racetrack ring resonator are presented. After fabrication of the resonators on silicon-on-insulator (SOI) wafers in a foundry process, the cantilevers were integrated by surface micromachining techniques. Off-state deflections of the cantilevers have been optimized to appropriately position them near the evanescent field of the resonator. Using electrostatic actuation, moving the cantilevers into this evanescent field, the propagation properties of the ring waveguide are modulated. We demonstrate 122 pm tuning of the resonance wavelength of the optical ring resonator (in the optical C-band) without change of the optical quality factor, on application of 9 V to a 40 µm long cantilever. This compact integrated device can be used for tuning/switching a specific wavelength, with very little energy for operation and negligible cross talk with surrounding devices.

OCIS codes: (070.5753) Resonators; (130.3120) Integrated optics devices; (130.4815) Optical switching devices; (060.4080) Modulation; (130.7408) Wavelength filtering devices; (220.4610) Optical fabrication; (230.4685) Optical microelectromechanical devices.

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#148205 - $15.00 USD Received 26 May 2011; revised 20 Jul 2011; accepted 20 Jul 2011; published 4 Aug 2011

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1. Introduction

Microring resonators have been attracting attention in recent years due to their compactness, high quality factor, ease of fabrication, and potential for dense integration. They are highly promising building blocks in the field of integrated optical systems, having a wide range of applications including lasers [1], optical switches [2], tunable wavelength filters [3], add/drop multiplexers [4] and biosensors [5]. Tuning of a microring resonator makes it possible to use it as an active element, which can have ample applications in future optical communication networks. Furthermore, tuning allows for compensation of small fabrication-induced variations of geometrical parameters, changes in material properties by temperature variations and so on. One of the tuning methods is to change the refractive index of the materials of the ring resonator and thereby the ring's resonance wavelength. The resonator can be tuned by a variety of means e.g thermo-optic, electro-optic, plasma dispersion, or (electro-) mechano-optic [6–8]. Among these methods, opto-mechanical tuning by electrostatic actuation has the characteristics of potentially providing a broad wavelength tuning range and requiring very little energy for operation and this technique has been studied more extensively in this paper.

In general both the real and imaginary parts of the effective index of a guided mode in a dielectric waveguide will be affected by the presence of an object –such as a cantilever– in its evanescent field. If the waveguide is part of a ring resonator, a change of the real part of the effective index causes a shift of the optical resonance wavelength, whereas a change of the imaginary part translates into a change of the optical quality factor.

Micromechanically-actuated wavelength-selective on/off-switching of a silicon-nitride microring resonator has been demonstrated before, by moving an aluminum membrane into and out of the evanescent field of a ring waveguide, using a 2 kHz, 0-30 V square-wave driving signal [2]. Since the lossy aluminum affects mainly the imaginary part of the effective index, this device can only be used as an on/off switch but cannot be used for wavelength tuning. In a different approach, 27 nm tuning at 1565 nm (or 1.7% wavelength tuning) of a silicon-nitride ring resonator has been demonstrated by perturbing the evanescent field with an external silica fiber probe [3]. Obviously, the drawback of this approach is the lack of monolithic integration.

#148205 - $15.00 USD Received 26 May 2011; revised 20 Jul 2011; accepted 20 Jul 2011; published 4 Aug 2011

Therefore, the quest of the current study is to fabricate, characterize, and demonstrate the feasibility of tuning or switching of optical signals using a silicon racetrack ring resonator integrated with a movable dielectric MEMS cantilever. On application of a voltage between the cantilever and the substrate, the former is pulled into the evanescent field. This increases the effective index of the resonator waveguide, resulting in a shift of the resonance wavelength. This CMOS-compatible device is designed for operation in the optical communications C-band (1530-1565 nm), and the waveguides of the ring resonator are designed to be single mode for TE-polarized light at a wavelength of 1550 nm.

The organization of this paper is as follows. The next section gives a brief description of the basic principle of the device. Section 3 discusses the fabrication technology for integrating dielectric cantilevers with optical racetrack ring resonators. The mechanical and optical characterization of the MEMS integrated device is presented in section 4. Then, a discussion about the fabrication issues and the performance of the device is given in section 5. Finally section 6 provides a summary and conclusions of the paper. Throughout this paper, off-state of the device refers to the situation in which there is no electrical signal, i.e. the cantilever is in the upper position, which in turn is an optical state in which the resonator is virtually unperturbed by the cantilever.

2. Basic principle

Figure 1 shows a schematic illustration of the integrated device, with (A) top view and (B), (C) different cross-sectional views. The modal field of an optical waveguide has an exponentially decaying evanescent field, which typically extends only a few hundred nanometers into the (air) cladding. The cantilever (length between 40 and 100 μm and 10 μm in width) is a bimorph consisting of an upper layer acting as the electrode and a lower layer acting as the dielectric. In the off-state, as shown in Fig. 1C, the thermal- and deposition-induced stresses during fabrication make it to bend upward [8,9]; the stress is optimized such that the tip of the bimorph is hardly affecting the modal propagation properties, i.e., the waveguide is unperturbed. On application of a voltage between the top electrode and the substrate, the cantilever is pulled towards the resonator and the air is partially replaced by the dielectric material of higher refractive index. This changes the modal propagation and hence tunes the resonator. The needed deflection of the bimorph is designed to be less than 500 nm to reduce the voltage required to pull the cantilever into the evanescent field. Figure 2 shows a close-up of Fig. 1C.

#148205 - $15.00 USD Received 26 May 2011; revised 20 Jul 2011; accepted 20 Jul 2011; published 4 Aug 2011

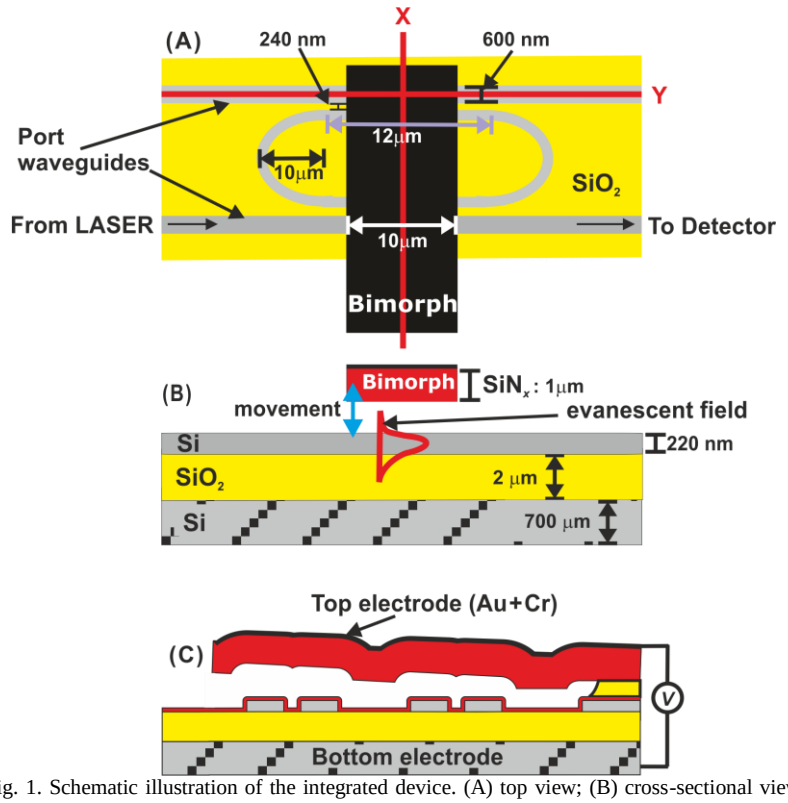

Fig. 1. Schematic illustration of the integrated device. (A) top view; (B) cross-sectional view through Y; and (C) cross-sectional view through X.

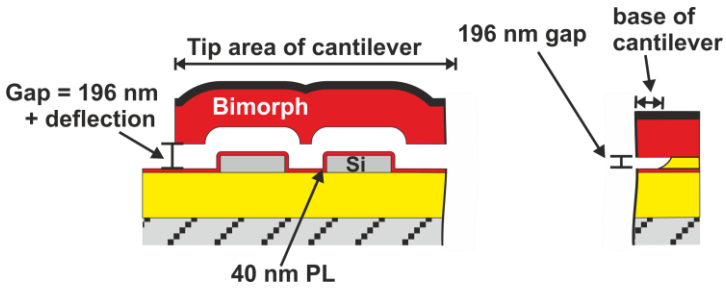

Fig. 2. Close-up of Fig. 1C.

3. Fabrication

3.1 Optical device fabrication

Racetrack ring resonators were designed with a bend radius of 10 μm and a straight section length of 12 μm [7,10]. As shown in Fig. 1A, the gap between the port (or access) waveguide and the straight section of the ring is 240 nm. The length of the access waveguides is 6000 μm with gratings at both end to couple light vertically [11]. The width of the ring- and its access-waveguides is 600 nm. However, 2200 μm away from the centre of the ring, in both directions, the width of the waveguides increases gradually and reaches 10 μm at the location of the grating couplers. The resonators and waveguides have been fabricated on a 200 mm SOI wafer using a 193 nm deep-UV lithography process by the silicon photonics platform ePIXfab [12]. The thickness of the silicon device layer is 220 nm and that of the handle wafer is 700 μm. The ring resonators were formed by patterning and etching the Si device layer and

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stopping on the 2 µm thick buried oxide layer, which serves as the bottom cladding of the waveguides.

3.2 MEMS integration

Figure 3 shows the fabrication flow for wafer-scale integration of bimorph cantilevers with racetrack ring resonators [13]. It is a two-mask process using positive photoresist for the UV lithography. (a) Starting with an SOI wafer, in which the optical resonators have been previously fabricated [12], (b) 40 nm low-stress silicon-rich nitride (SiN_x) is deposited at 850°C using low-pressure chemical vapour deposition (LPCVD) [14]. It serves as a protective layer (PL) for the underlying oxide cladding layer and the waveguides. This SiN_x layer is removed from the backside of the wafer by reactive ion etching (RIE) to later on have access to the bottom electrode. Next, a 200 nm LPCVD tetraethyl orthosilicate (TEOS) oxide sacrificial layer (SL) is deposited conformally, at 700°C. The thickness is chosen such that the formation of etch residues, known as stringers (see section 5.1.3) can be reduced or even prevented [13]. Then 1.1 µm LPCVD SiN_x, which will later be structured into the MEMS cantilevers, is deposited. On the front side of the wafer, 50 nm gold is sputtered as the top electrode using 8 nm chromium as adhesive. (c) Subsequently, the first resist mask (OiR 907-17, Fujifilm) is used to pattern the metal layers; Au is etched in gold etch solution at 30°C (KI = 132 g, I_2 = 18 g, DI = 1200 ml, in which 600 ml glycerin is added to reduce the excessive undercut), and Cr is wet etched in chromium etchant (MERCK 111547.2500). (d) The second resist mask (OiR 908-35, Fujifilm) is used for patterning the SiN_x into the cantilevers by RIE [15] (Elektrotech PF340 at 10°C, 75 W, 10 mTorr, 25 sccm CHF_3 and 5 sccm O_2). The resist is first plasma etched for 1 minute (TEPLA 300E, 200 sccm O_2, 500 W, 1.2 mbar) to remove the fluorocarbon contamination produced by RIE [16] which, if remaining, might hamper the subsequent 20 minutes HNO_3 (99%) resist stripping. (e) Finally, sacrificial layer etching (SLE), using buffered hydrofluric acid (BHF, NH_4F:HF = 7:1) followed by freeze drying [17], is applied to release the cantilevers. The SLE is divided into three steps in which the second one consists of an ultrasonic cleaning step as described in [13] to remove the SiN_x stringers. Scanning electron microscopic (SEM) images of a successfully integrated device is shown in Fig. 4.

#148205 - $15.00 USD Received 26 May 2011; revised 20 Jul 2011; accepted 20 Jul 2011; published 4 Aug 2011

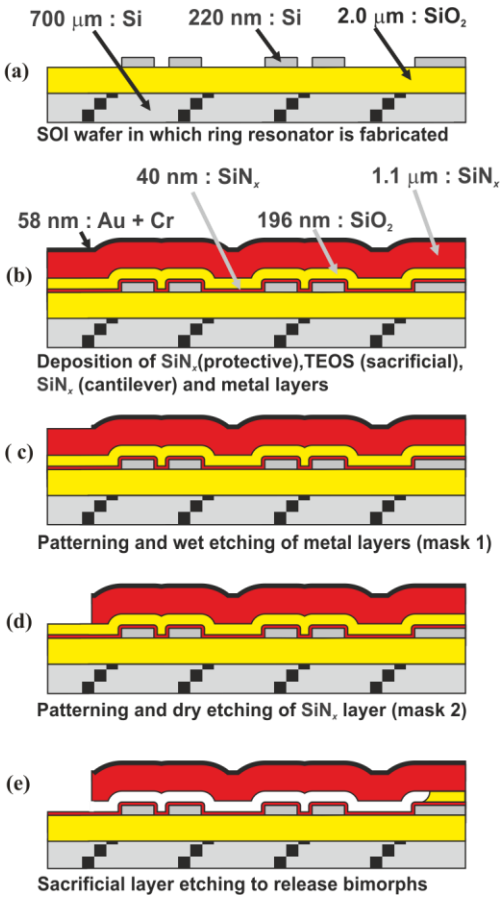

Fig. 3. Fabrication flow of a silicon racetrack resonator with a tuning cantilever.

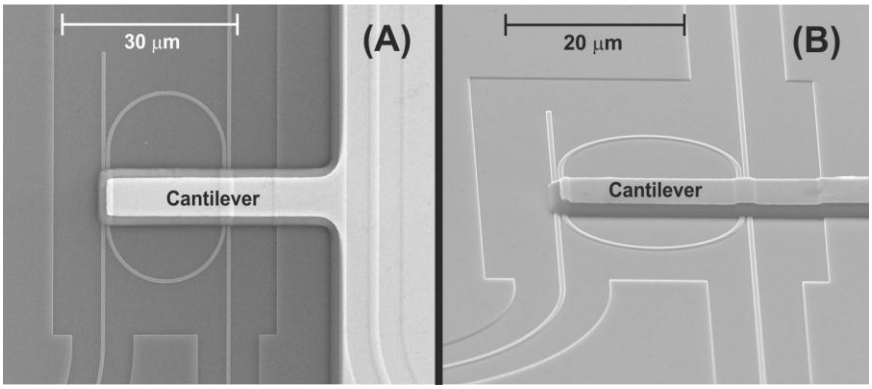

Fig. 4. SEM image of a 40 μm long cantilever successfully integrated with the racetrack ring resonator showing (A) top view and (B) oblique view.

4. Characterization

4.1 Static mechanical measurements on off-state deflection and pull-in voltage

The integrated cantilevers were statically characterized in order to analyze their mechanical performance. Thickness and uniformity of each deposited layer is measured during fabrication using ellipsometry and under-etch during the SLE is measured using optical microscope

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(OM). Off-state deflections and static pull-in measurements of cantilevers of various effective lengths were carried out at room temperature by white light interference microscopy (WLIM, Polytec MSA400).

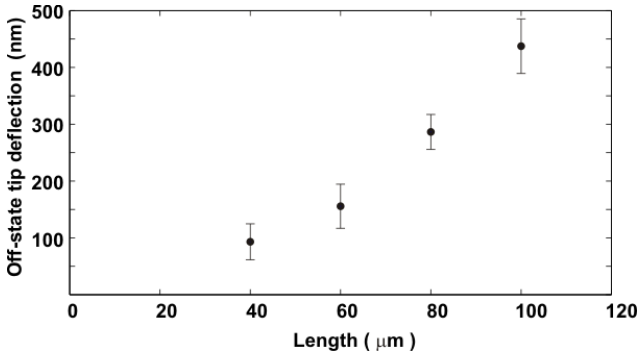

Fig. 5. Off-state tip deflections of cantilevers of various lengths, measured by WLIM.

Figure 5 shows the measured off-state tip deflections (the vertical distance between the tip and the base) of the cantilevers of different lengths (corresponding to the mask design). The standard deviation error bars in the observed deflection are calculated by measuring seven cantilevers of each length across the wafer. The variation in the observed deflection is due to the non-uniformity of the deposited layers and will be discussed in section 5.1.1. Clearly, the deflection increases with the length of the beam, which is caused by the stresses in the bimorph cantilever resulting in a circular shaped curvature. For the same reason, the air-gap between the cantilever and the ring resonator varies along its length. At the base, for all bimorphs, it is 196 nm, which is the thickness of the sacrificial layer. At the tip of the bimorph it is given by adding the off-state tip deflection to 196 nm. Thus a 40 μm long cantilever has approximately 290 nm (196 + 94) air-gap at its tip (Fig. 5 and Fig. 6). As the micro-ring resonators are fabricated by etching the silicon device layer down to the SiO_2 cladding, the resulting stepped geometry is transferred into the subsequently conformally deposited layers. The hills and valleys observed in Fig. 6 are due to the fact that the cantilever is deposited on top of the micro-ring resonator (also observed in Fig. 2 and Fig. 4)

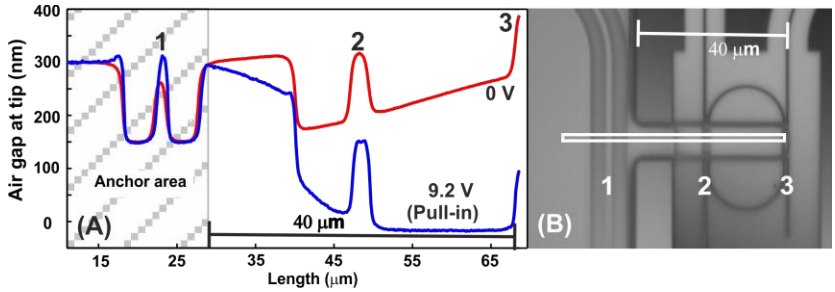

Fig. 6. (A) Static deflection of a 40 μm long cantilever at the off-state (0 V) and at pull-in (9.2 V), measured by WLIM. And (B) OM image of the integrated device which was measured, where the rectangular square represents the WLI scanning area.

A well-known instability in operating electrostatic MEMS is the 'pull-in' phenomenon. The pull-in voltage is defined as the voltage beyond which the increasing restoring spring force can no longer keep up with the even faster increasing electrostatic attractive force [18] and at this voltage the cantilever collapses onto the substrate thereby possibly destroying it for further use. Hence it is important to determine the pull-in voltage to estimate the stable range of operation of the cantilever. Figure 7 shows a static pull-in measurement by WLIM for a 60 μm long cantilever, which has a pull-in instability point at a DC voltage of 4.8-4.9 V. Pull-in voltages for cantilevers of different design lengths have been measured as well (Fig. 8). The

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error bars in the measurements are found by determining the observed pull-in voltage of three cantilevers of each length across the wafer. As the length of the cantilever increases, the pull-in voltage decreases. More details can be found in section 5.1.4.

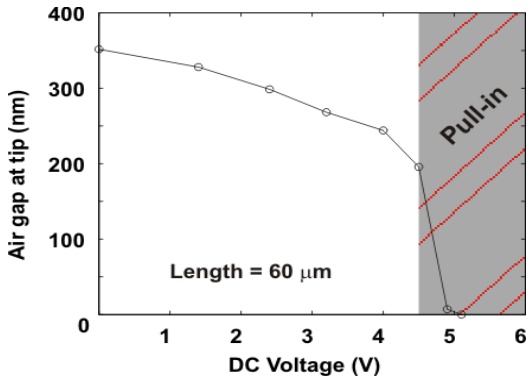

Fig. 7. Static tip deflection as a function of applied actuation voltage for a cantilever of 60 μm length.

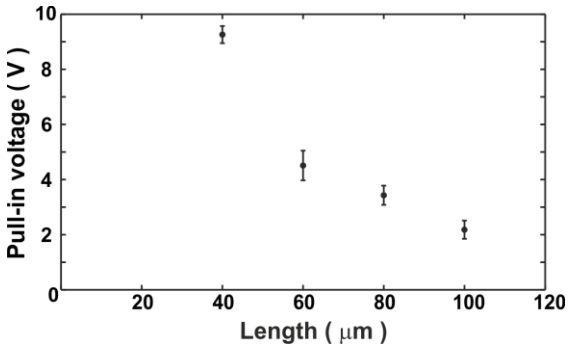

Fig. 8. Measured static pull-in voltage as a function of the length of the cantilever.

4.2 Optical measurements

MEMS integrated racetrack ring resonators were optically characterized to assess their performance. Figure 9 shows the measurement set up used for optical modulation. Infrared light from a tunable laser (input power of 1 mW) is coupled through integrated grating couplers [7,10,11], to the input waveguide, using a polarization maintaining fiber (PMF). The transmitted light from the 'through' and the 'drop' port waveguides is recollected by second and third gratings, and guided to the photodetector (Agilent 8164B and 81634B) through a single mode fiber (SMF). All the measurements are performed with a resolution of 5 pm. A typical response measured in the 'through' and 'drop' ports, after the cantilever integration, is shown in Fig. 10A. The racetrack resonator has a measured free spectral range of 6.6 nm (= 1558.1-1551.5). Figure 10B shows the various ports of the ring resonator and for dimensions of the device see Fig. 1.

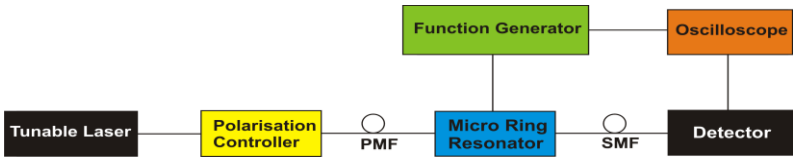

Fig. 9. Schematic representation of the optical modulation measurement set up.

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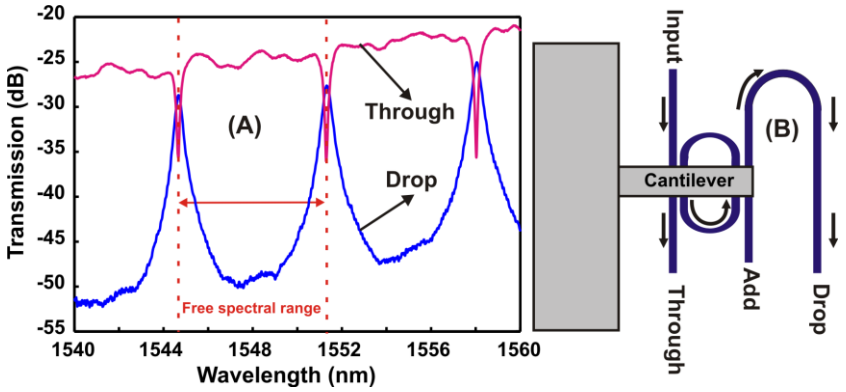

Fig. 10. (A) Through and drop response of the fabricated racetrack ring resonator after cantilever integration. (B) schematic of the ports of the ring resonator (for dimensions see Fig. 1).

Results of the tuning experiments on the cantilever-integrated ring resonator are shown in Fig. 11. The spectrum shows a 20 dB drop of transmission at a resonance wavelength of 1546.32 nm. Resonance wavelength tuning of 122 pm and a modulation depth of 18 dB are measured with a 40 μm long cantilever operated up at 9 V. During the stable range of operation of the cantilever, the quality factor of the resonance remains unchanged, indicating that the cantilever does not introduce any losses to the resonator. However, at pull-in (9.2 V, Fig. 6), the cantilever touches the waveguide and a moderate reduction in the quality factor of the ring resonator (from 8000 to 5000) as well as a considerable change (5 nm) in the resonance wavelength is observed. The latter observation might give this device the ability to switch optical signals in an effective way; an elaboration on this is given in section 5.2, as long as stiction does not occur.

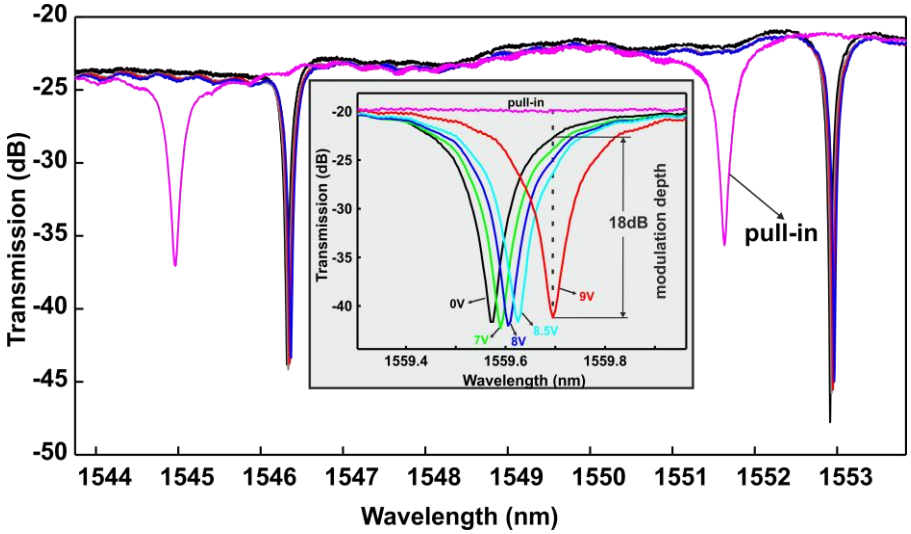

Fig. 11. Resonance wavelength shifting due to mechanical tuning, by a 40 μm long cantilever, for the device shown in Fig. 4. The inset shows a 122 pm tuning at 1559.57 nm.

5. Discussion

The first part of this section provides a detailed discussion on the fabrication issues regarding the materials selection, tapered gap, stringer formation and removal, pull-in behavior, protrusions on the cantilever and cantilever length. The second part discusses the mechano-optical performance of the integrated device.

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5.1 Fabrication issues

5.1.1 Materials selection

Conformal layers with high wafer uniformity (e.g. thickness, intrinsic stress, refractive index) are essential for successful device fabrication with high yield [13]. Therefore, the composition and thickness of each layer was chosen carefully. Table 1 gives the measured variation in thickness across the wafer and the refractive index for various conformal layers used for the fabrication. By virtue of its high uniformity (compared to plasma enhanced chemical vapour deposition (PECVD) methods), LPCVD TEOS oxide was chosen as the SL. Furthermore, it is important to protect the thermal oxide lower cladding layer (i.e. the 2 µm buried oxide) during SLE. If unprotected, it will be attacked by BHF which will result in under-cutting the waveguides, thereby destroying the devices [13]. The PL was selected to be SiN_x because of its high resistance (etch rate 0.5 nm/min) to the BHF etchant used for SLE of TEOS oxide (180 nm/min). During the subsequent SiN_x deposition at 850°C, the TEOS oxide SL is annealed which reduces the etch rate to an estimated value of 150 nm/min. The required SL etch time of a cantilever of 10 µm wide (5000/150 ~33 min) defines the minimum thickness of the PL to be approximately 17 nm (33x0.5). However, an overetching of 19 minutes is performed to ensure that the SiO_2 beneath the cantilever is completely removed. Including this extra time and a safety time to counteract delays caused by layer non-uniformity, a PL thickness of 40 nm is selected. Gold is chosen as the top electrode by virtue of its relatively low residual stress, which in turn reduces the upward bending of the cantilever. But it needs an additional layer to promote sufficient adhesion with the nitride underneath. The SLE step in BHF excludes to select metals like titanium, tantalum, aluminum etc as either the top electrode or as the adhesive layer. A reasonable candidate is Cr, although this material is known to have large built-in stress. Therefore, it has to be as thin as possible. It is found that a combined thickness of 58 nm (50 nm Au and 8 nm Cr) gives an acceptable off-state deflection.

Table 1. Measured thickness variation across the wafer and the refractive index of different conformal layers

Layer (function)	*Thickness (nm)*	*Standard 3σ deviation (nm)*	*Measured refractive index (n) at 633 nm*
SiN_x (Protective)	*40*	*2*	*2.20*
TEOS (Sacrificial)	*196*	*2*	*1.45*
SiN_x (Cantilever)	*1097*	*50*	*2.25*

5.1.2 Tapered gap

After SLE, the thickness of the remaining PL in the freely accessible areas is approximately 14 nm (40 - 52 x 0.5). However, the PL underneath the cantilever will have a tapered profile as the SL is covering the PL during part of the SLE time [19]. This effect is shown in Fig. 12. Below the centre of the cantilever the PL thickness variation can be as high as 16 nm.

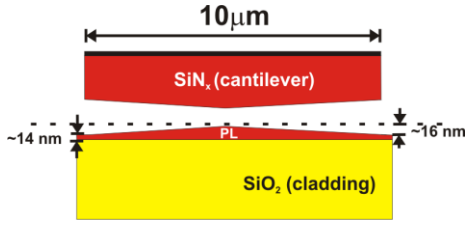

Fig. 12. Variation in the PL and cantilever layer thickness below the cantilever, after the SLE in BHF.

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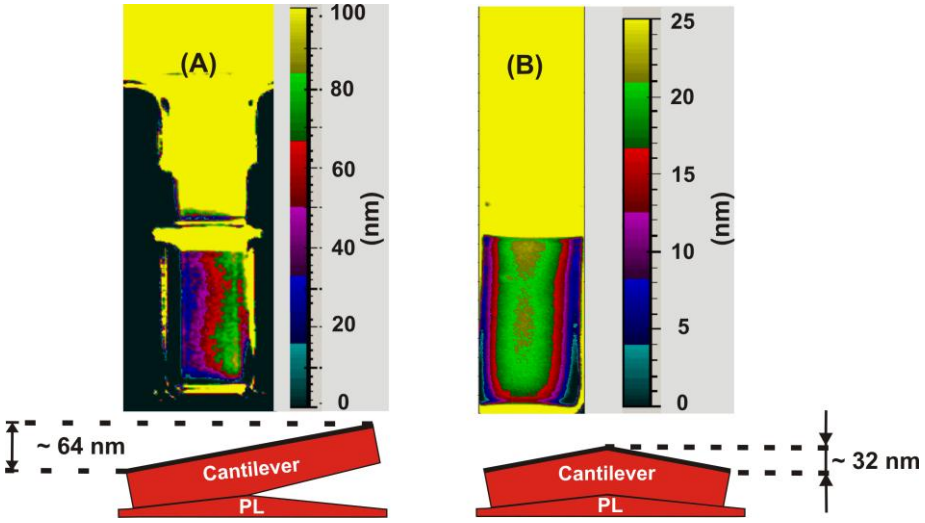

Fig. 13. WLI images showing two different shapes of the beams after pull-in, (A) half sticking: tilts beam tip, (B) full sticking: deforms beam tip.

In addition to the PL underneath the cantilever, the bottom side of the cantilever itself will have a tapered profile as well. Due to this, at pull-in, the cantilever can either stick completely or partially (half) at the substrate. Half sticking will force the cantilever to tilt either to the left or the right (Fig. 13A), whereas full sticking will deform the beam as shown in Fig. 13B. One way to prevent stiction might be by introducing holes into the cantilever as shown in Fig. 14. The additional holes will have at least two positive effects. First, they will reduce the time needed for the SLE and, thus, relax the thickness requirements of the SL and PL. Second, they will cause a saw tooth etch profile under the cantilever, that will prevent intimate contact between the surfaces.

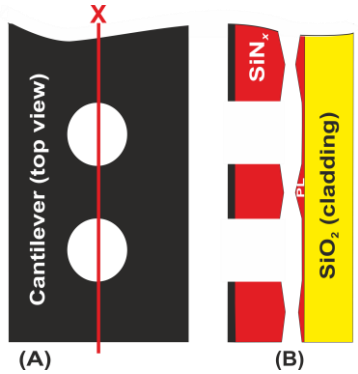

Fig. 14. (A) top view and (B) cross-sectional view in X-direction (defined in Fig. 1) of (part of) a cantilever having etch holes which will create a saw toothed etch profile underneath.

5.1.3 Stringer formation and removal

As the evanescent field of an optical waveguide structure decays exponentially with distance from the waveguide, the vertical air-gap between actuator and waveguide has to be sufficiently small in order to observe any mechano-optical modulation, as experimentally demonstrated in [3]. Since the thickness of the SL defines this gap, it has to be thin (50 – 300 nm). The smallest possible thickness of the SL is mainly related to the etch selectivity of the cantilever SiN_x relative to the SL TEOS oxide in the RIE step (Fig. 3d) and the non-uniformity during the etching of both layers and their thickness. The etch rate of TEOS oxide (as deposited) in RIE is 35 nm/min and that of SiN_x is 55 nm/min, i.e. an approximate

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selectivity of SiN_x:TEOS = 1.6:1. This selectivity is critical if the etch rate non-uniformity of the layers is high.

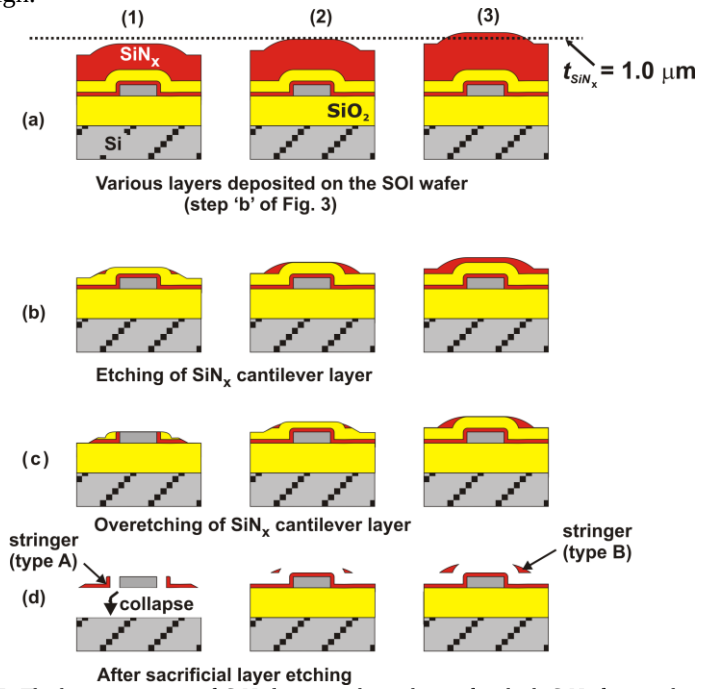

Fig. 15. Thickness variation of SiN_x layer on the etching of a thick SiN_x from a thin TEOS layer for (1) t_{SiNx} = 0.95 μm, (2) t_{SiNx} = 1.0 μm and (3) t_{SiNx} = 1.05 μm.

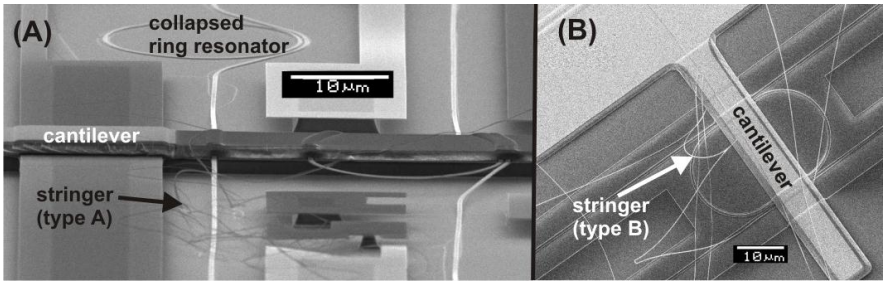

Fig. 16. SEM images showing (A) the ring resonator and access waveguides collapsed by overetching of the SL and PL layer during the RIE of the SiN_x cantilever layer and (B) stringer type B distributed all over the wafer.

Figure 15 shows the effect of the selective etching of a non-uniform SiN_x layer on top of a thin TEOS oxide layer. The measured '3σ' for the cantilever device layer (SiN_x) is 50 nm (Table 1). Due to this, at some points of the wafer, the SiN_x thickness is less than the designed value (Fig. 15(1)) whereas on other points it is above the designed value (Fig. 15(3)). This means that RIE overetching has to be done to completely remove 1.1 μm SiN_x from all over the wafer, which is mostly dictated by the wish to prevent so-called 'stringers' due to etch residue at surface steps [13]. These stringers are observed as "satellite" nanostructures along the silicon waveguides (in Fig. 15d and Fig. 16). The poor RIE selectivity limits the overetching to be less than 5 minutes for a SL thickness (t_{SL}) of 196 nm (196/35 ~5.5). If a longer overetching time is used, the PL layer is under attack which finally results in destroying the ring resonator and its access waveguides (Fig. 15(1)c). The collapse of waveguide structures is schematically presented in Fig. 15-1d and a SEM image of it is shown in Fig. 16A. Furthermore, the SiN_x cantilever layer has to be chosen sufficiently thick to

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prevent optical loss caused by the electrode. And so, the absolute non-uniformity is quite big (± 50 nm), which is causing an etch delay across the wafer of several minutes. Considering the aforementioned selectivity and non-uniformity of the SiN_x layer, the SL thickness is selected to be approximately 200 nm. By carefully checking the thickness and non-uniformity of both layers with dummy wafers and by analyzing the loading effect, we could successfully etch through a 1.1 µm SiN_x layer on top of a 196 nm SL. However, in this case the stringers were not completely removed by sufficient overetching (Fig. 16(B), but SiN_x (cantilever) etching has been stopped when it has reached the planar TEOS-SiN_x (cantilever) interface, all over the wafer. The stringers that remained due to etch delay caused by layer non-uniformities, were successfully removed by an ultrasonic cleaning technique as described in [13].

5.1.4 Pull-in behavior

It is well known that the pull-in instability limits the travelling range of a parallel plate actuator to one third of its gap [20]. A more detailed analysis [21] shows that for a straight, initially stress-free cantilever, this instability point is not at one third of the gap, but rather at 0.44 of the effective gap, (g_{eff}). Although the cantilevers in this study are not straight and have built-in stress, we assume that the instability point is close to 0.44 g_{eff}. The effective gap is the combination of the air gap and the effective dielectric gaps where the latter can be found from dividing the thickness of each dielectric layer by its relative permittivity (ε_r). Figure 17 shows the various parameters considered for the effective gap calculation for a 40 µm long cantilever, which is given by,

$$g_{eff} = \frac{2000}{3.9} + \frac{40}{7.5} + 196 + 94 + \frac{1100}{7.5} \approx 955nm$$

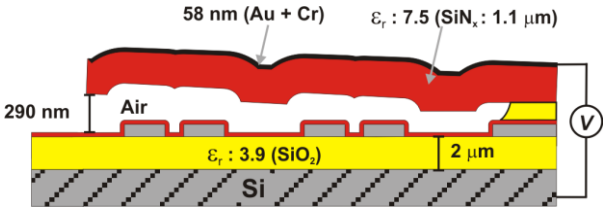

Fig. 17. Various parameters considered in the effective gap calculation for a 40 µm long cantilever.

As the air gap (290 nm) is less than 0.44 of the effective gap (420 nm), the pull-in instability should not have been observed in this device. However, the device clearly shows pull-in behaviour. Possible reasons for this low pull-in voltage could be the presence of the semiconducting silicon device layer inside the (effective) gap as well as charge accumulation in the SiO_2 cladding layer.

A large off-state deflection will make the beam stay far away from the evanescent field, which considering optical performance is good, but it also requires a higher voltage to pull it towards the substrate, which might be limited by the pull-in instability point, as discussed in the previous paragraph. A lower operating voltage can be achieved by increasing the length of the cantilever even though the off-state deflection increases with the length too. Furthermore, the length of the beam cannot be increased beyond a critical length as it can result in stiction during the release process or during operation due to various adhesion forces [21]. Moreover increasing the length decreases the resonance frequency of the cantilever [8], thus reducing its maximum speed of operation.

5.1.5 Protrusions on the cantilever

Conformal layer deposition results in the formation of protrusions (“ridges”) on the cantilever that penetrate into the gap between the ring resonator and the port waveguides. Figure 18 shows a ridge protruding into the gap between the ring and the waveguide in the cantilever off-state. The ridges are observed for all cantilevers across the wafer. Although the sharpness

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of the ridges can be reduced by an increase in SL thickness, this in turn will increase the air gap between the cantilever and the micro-ring resonator thereby reducing the modulation depth. Since the coupling between the ring and the straight waveguide is strongly affected by the variation in distance between them [22], the effect of these ridges on the coupling strength is a topic which needs further investigation.

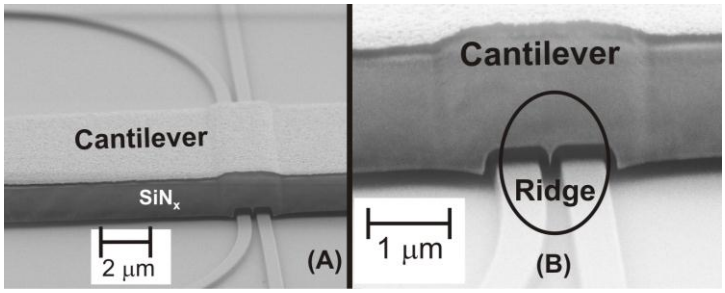

Fig. 18. (A) SEM image showing the released cantilever in the off-state with its pin (B) protruding into the gap between a port waveguide and a straight resonator waveguide section.

5.1.6 Cantilever length

As a last fabrication issue, the actual length of the fabricated cantilever is increased from the designed length of the mask due to the undercut at the bond pads caused by the SLE [8]. The undercut, which was measured with an optical microscope to be 5.5 μm, will result in an increase of the effective cantilever length with associated lower resonance frequency and pull-in voltage.

5.2 Optical performance

The optical loss in the device is another parameter which has to be analyzed. For this, the transmission in a straight waveguide (length = 6 mm and width = 600 nm) and a ring resonator on the same chip, before and after the MEMS integration are measured (Fig. 19). It is observed that after post processing the transmission decreased in the targeted wavelength range of 1530-1565 nm. This could be due to the red shift of the transmission spectrum of the grating couplers [11] due to the added high-index PL (Fig. 19). In any case the 20-25 dB losses observed in Fig. 10 and Fig. 11 are not inherent to the ring resonator, but are the overall loss by the system, which includes and is dominated by coupling and propagation losses. This also means that, when a silicon based light emitting system is directly integrated with a potential future all-optic communication system, the loss introduced by the ring resonator is negligibly small (< 3 dB [7]).

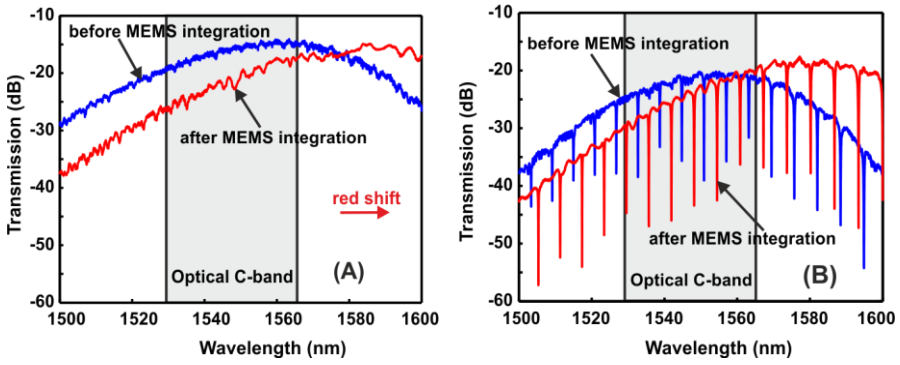

Fig. 19. Transmission measured in (A) straight waveguide and (B) ring resonator, before and after the MEMS integration.

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Even though higher tunability is achieved in thermo-optical modulators (4.3 nm at 1546 nm [6]), the increased power consumption makes them impractical for wavelength routing where many ring resonators need to be cascaded. Electro-optical modulators based on carrier injection [23] require less power for tuning, but the devices suffer increased optical losses as the conductivity is increased. From Fig. 11 it is evident that mechano-optical modulation enables a significant shift in the resonance frequency without introducing optical losses, i.e. only a voltage change from 8.5 to 9 V is enough for realizing a wavelength shift of 70 pm. The tunability range depends on the distance between the cantilever and the ring resonator. A higher tuning range can be achieved by increasing the stable range of operation of the cantilever. The ring resonator described in this paper has a quality factor of ~8000 and a full width at half maximum of ~195 pm. Within its free spectral range of 6.6 nm, at least 16 dense wavelength division multiplexed (DWDM) channels of 0.4 nm (50 GHz) channel spacing can be realized. With the present results the device can be used as an on/off switch for a specific channel and by eliminating the stiction of the cantilever at pull-in, maximum tuning of few nanometers is feasible.

6. Conclusions

A technology for integrating cantilevers with silicon integrated optical devices using surface micromachining techniques has been reported. MEMS integrated racetrack ring resonators have been fabricated successfully on SOI wafers and their mechanical and optical characterization has been carried out. These electrostatically actuated integrated devices have been fabricated on wafer scale with CMOS compatible technology. Reversible resonance wavelength tuning of 122 pm with a modulation depth of 18 dB is demonstrated for an integrated device. Maximum tuning can be larger (> 5 nm) when allowing pull-in and avoiding stiction by proper measures such as anti-stiction bumps or coatings.

Acknowledgments

The authors would like to acknowledge R. Sanders and A. Hollink for their advice on measurements. This project is funded by the NanoNed programme of the Dutch Ministry of Economic Affairs.

#148205 - $15.00 USD Received 26 May 2011; revised 20 Jul 2011; accepted 20 Jul 2011; published 4 Aug 2011