Structural Testing of the HYPRES Niobium Process

Arun A. Joseph, Javier Sese, Jaap Flokstra, and Hans G. Kerkhoff

***Abstract*—The HYPRES 3.0 μm Niobium (Nb) process has proven to be capable of realizing complex Low Temperature Superconductor (LTS) Rapid Single Flux Quantum (RSFQ) circuits. In such a mature fabrication process, the importance of the detection of random defects is crucial as they contribute to the majority of the defects occurring while processing the chips. The global low yield in SCE is due to the fact that little is known about the defects and fault mechanisms occurring in Nb technology. This is, however, of crucial importance in realizing the required complex systems with yields required for commercial production. For this purpose, a structural testing approach has been applied to the HYPRES Nb process. As a result, we have developed test structures for the detection of random defects in the process. Test chips were realized in the process and measurements were carried out. Test results on the processed chips leading to defect statistics in the HYPRES Nb Process are presented in this paper.**

***Index Terms*—LTS devices, RSFQ circuit testing, structural testing, superconductor electronics.**

I. Introduction

THE HYPRES Nb process is the best available commercial superconductor foundry. Many complex devices have been realized in the process [1]–[3]. Yet, the yield levels are much lower than in the semiconductor industry. Although extended research is going on in making advanced process by increasing critical current density of the process, very little or no information is available in the literature for achieving high yield for this superconductor process.

In semiconductor microelectronics, special test structures have been developed and realized along with the functional integrated circuits (ICs). The information gathered using these test structures is used for yield analysis and defect-based testing [4]. In this way, the semiconductor industry has developed methodologies and techniques to achieve high yields.

The type of defects that can occur in an IC manufacturing process flow can be divided into two categories: design failures and manufacturing defects. We will only consider manufacturing defects, which can be further classified into two subclasses:

1. Gross manufacturing defects
2. Local (random) defects

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Defects that affect a large area, even a complete wafer, are called gross manufacturing defects. Random defects are important because they contribute to the majority of the defects in a mature process. The effective detection and avoidance of these defects in a manufacturing process is essential for the quality of the devices developed in that technology. Information about these defects in a process is gathered by using specially designed test modules called Process Control Monitors (PCM).

We have studied the types of defects that can occur in the HYPRES process. In this paper, the structural defects that can occur in the HYPRES Nb tri-layer $(\mathrm{Al/AlO_x/Nb})$ based technology and its experimental results on test structures (on PCMs) are discussed resulting in the most probable defects in the process.

The organization of the paper is as follows. The next section describes the HYPRES Nb process. In Section III, a methodology used for the identification of the defect locations in HYPRES process is presented along with associated test structures. The experimental setup for the analysis is presented in Section IV. The implementation of the test-chip and measurement results from associated structures are presented in Section V. The paper concludes with a realistic ranking of the probable defects in the HYPRES process.

II. HYPRES Nb Process

Knowledge of the Superconductor Electronics (SCE) fabrication process under study is essential for a clear understanding of the defects and fault mechanisms. The investigations were undertaken in the 3.0 μm proven process from HYPRES NY, USA [5]. The standard critical current density, $\mathrm{J_c}$, of the process under investigation is 1 $\mathrm{kA/cm^2}$ for the design of Rapid Single Flux Quantum (RSFQ) circuits. The minimum feature-size in the process is 3.0 μm with junction capacitances of 0.05 $\mathrm{pF/\mu m^2}$. The cross-section of the process is given in Fig. 1.

The process features four Nb metal layers labeled M0 (100 nm), M1 (135 nm), M2 (300 nm) and M3 (600 nm). The layer R3 (350 nm) provides a low-resistance circuit elements as well as contact for chip bonding. M0 is the primary ground plane deposited on an oxidized silicon wafer. M3 can be used as a second ground plane to design more stable circuits if required or as a wiring layer. M1 and M2 are used as wiring layers and when a Josephson Junction (JJ) is defined, they will act as its two contact electrodes.

To reduce the probability of pinholes in the isolation layers leading to inter-layer shorts, the isolation is carried out in two separate $\mathrm{SiO_2}$ depositions. The layers M0 and M1 are separated by I0 (150 nm), while M1 and R2 from M2 by I1B (200 / 100 nm), and I2 (500 nm) separates M2 and M3. The I1A layer defines a JJ, which is a tri-layer consisting of 3 sandwich layers:

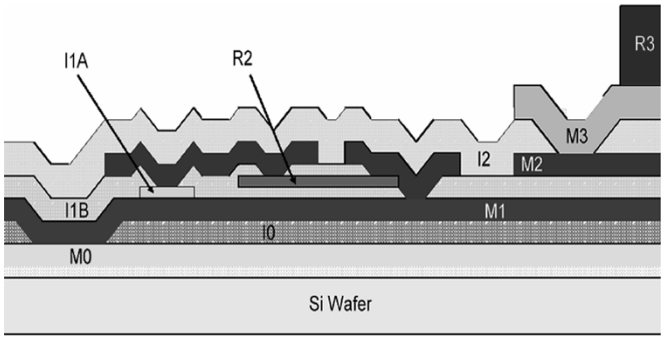

Fig. 1. Cross section of the HYPRES Nb process.

two Nb layers acting as the electrodes with the Al_2O_3 in-between (135/11/45 nm). A tri-layer is formed this way so as to minimize the formation of pinholes in the thin barrier.

As mentioned in [6], the types of defects that can occur in an SCE fabrication process are:

1. Junction defects,
2. Metal layer defects,
3. Resistor layer defects, and
4. Isolation layer defects.

Junction defects are of two types—an open and short junction. Metal-layer defects also cause intra-layer shorts and opens as well as inter-layer shorts. Resistor-to-metal shorts and high contact resistance result in problems associated with the resistor layer. Isolation defects cause inter-layer shorts and problematic via holes. In a mature process, the interconnect causes the majority of the random defects.

III. Defect-Prone Locations and Structures in the HYPRES Process

We now describe our investigation to find the defect-prone locations in the HYPRES process as well as the structures developed for the detection of the defects in the process. Identification of the defect-prone locations is based on the process information from the previous section.

A study of the design rules [5] for the process was the first step in this investigation. This study revealed possible 31 locations in which a defect can occur due to the topography of that particular location. This information was used for the second step. Two cells libraries designed in the process were used in this stage for the investigation. The first one was a cell library from HYPRES and the second one from Chalmers.

The predicted locations based on the design rules were cross checked with the cell libraries. About 25 locations in the HYPRES cells as well as 20 locations in the Chalmers cells showed the predicted defect types. Hence, the probability of the occurrence of the predicted defects had to be determined using structures capable of detecting these defects. Our earlier work on the JeSEF Nb process had resulted in structures capable of detecting a single defect at a time [6]. Some of the structures were translated for the HYPRES process.

New structures were also developed, as the HYPRES process is more mature one than the JeSEF process. The investigation was extended to all possible interconnects. An example of a structure is given in Fig. 2. The figure shows a comb-meander

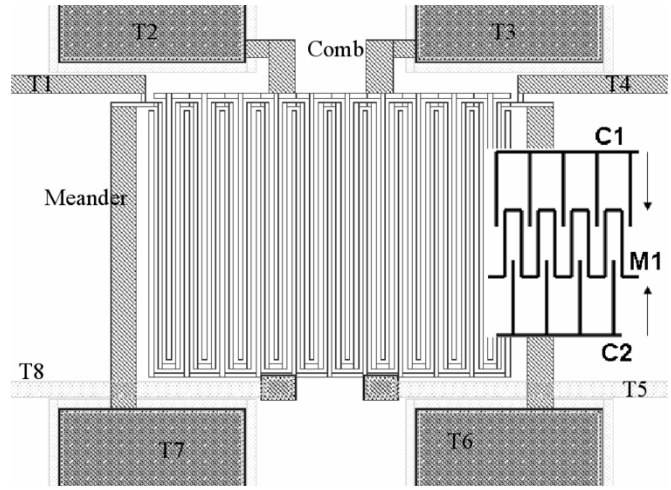

Fig. 2. Example of a test structure developed for the HYPRES process. The structure designed to detect an intra-layer short in the M1 layer. The pads are 100 μm in width.

structure designed to detect the intra-layer short in a layer (here the M1 layer). This structure is an interleave of a meander (M1) with two comb structures (C1 and C2) as shown in the inset [7]. T1, T7 and T4, T6 are the two ends of the meander and the combs are connected to T2, T3 and T5, T8 respectively. The double connection is to facilitate four-point measurements on the structure. The continuity of the meander is first measured by four-point technique on T1, T4 and T6, T7 as the current and voltage pair. Then a short is detected if the measurement between any of the T1/T7 with T2/T3 or T5/T8 results in a measurable resistance. More details on the other types of structures used are presented in [6].

IV. Experimental Setup

All room temperature measurements are being performed on an Electroglass X2001 semi-automatic probe station. This measurement set-up is positioned in a light-tight box. The X2001 probe station has a 6″ hot-chuck and a temperature controller Temptronic TP315 is available in the set-up. The TP315 has a temperature range of 0°C–200°C with resolution of 0.1°C. A "2 × 10" pin probe card is used for measurements. It is first manually positioned to the reference structure of the first chip to be tested on the wafer. After positioning, a program called Integrated Circuit Measurement System (ICMS) controls the automatic measurement [8]. ICMS controls the positioning of the probe on the die as well as the type of test to be performed depending on the test-structure.

The electrical measurements are performed by an HP4141B Modular DC Source/Monitor and an HP3456A 6(1/2) digit Digital Voltmeter. In combination with an HP4084B Switching Matrix Controller, the corresponding structure to be tested is selected. ICMS determines how the connections are made to different test structures via the switching matrix connected to the probe card. The four-point measurement schemes of the test structures were implemented in ICMS. Measurements were carried out by injecting a fixed current to the structures. Depending on the sheet resistance of the material (Nb) and length of the wire, the expected resistance value is calculated. Based on the

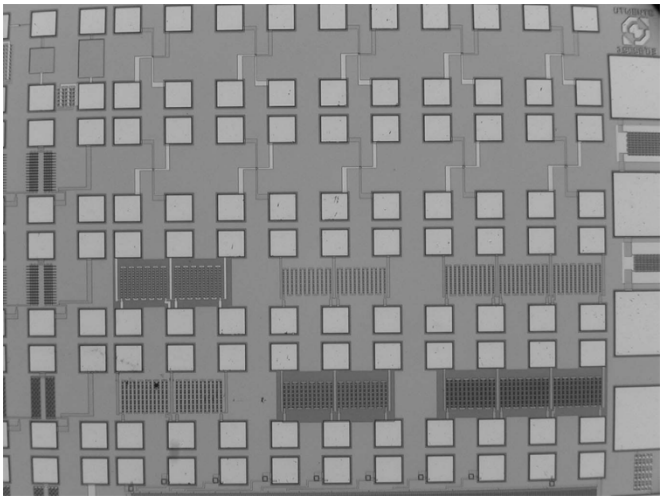

Fig. 3. Micro-photograph of part of the test chip designed for the HYPRES Nb process. The small pads are made of squares with 100 μm edge.

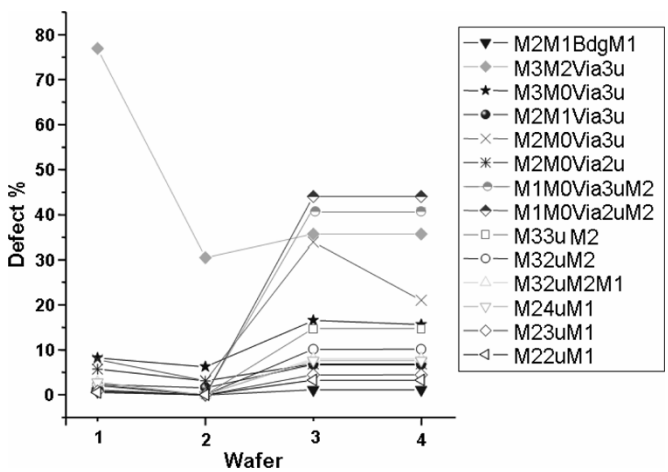

Fig. 4. Part of the measurement results from the test chip designed for the HYPRES Nb process.

symmetry of the structures, each measurement results in the same resistance with an allowed parametric deviation. A large deviation of the measured value from the expected value shows the presence of a defect.

V. Measurement and Data Analysis

The raw test data produced by the tester is sorted using a Unix shell script and is further analyzed using MATLAB [9]. The shell script separates data from the raw output file and groups them into similar defect categories. The MATLAB m-files for data analysis handle the data and perform statistical tests to identify the detected defects. The data is also graphically analyzed using the Origin Graphics package [10] for data analysis.

Three test chips were placed in each wafer and the test chip is as shown in the micro photograph in Fig. 3. There are 100 sets of structures in each chip exclusively for room temperature measurement. They were divided into 5 columns of 20 set of structures as can be seen in Fig. 3. The test time required by the prober to complete the data acquisition from a test chip is about 80 minutes. The room temperature tests were carried out at 298 K using the temperature controller module in the experimental set-up.

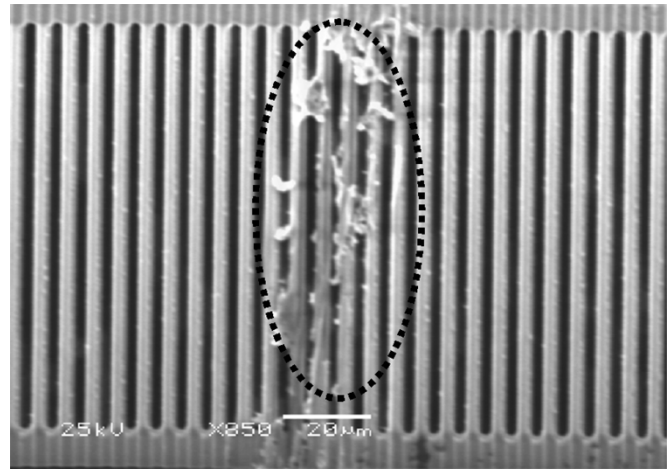

Fig. 5. One of the detected defects in a test chip designed for the HYPRES Nb process. Here the defect is an M3-M2 interlayer short.

TABLE I
Ranking of the Probable Defects in the HYPRES Nb Process

No.	Nature of the defect	Defect %
1.	M3 crack over a 3μ M3M1 via	66.115
2.	M3 crack over a 2μ M3M1 via	56.635
3.	M3 crack over a 3μ M3M2 via	54.750
4.	M3 crack over a 2μ M3M2 via	47.213
5.	M3 crack over a 3μ M3M0 via	38.015
6.	M3 crack over a 2μ M3M0 via	27.292
7.	Crack in 4μ M3 over an M2 edge	26.438
8.	Crack in 3μ M3 over an M2 edge	24.563
9.	Crack in 2μ M3 over an M2M1 edge	23.938
10.	Crack in 2μ M3 over an M2 edge	23.500
11.	Short between M3 & M2 over M2 edge	22.000
12.	Short between M3 & M2 over M2M1 edge	21.711
13.	M2 crack over a 2μ M1M0 via	13.250
14.	M2 crack over a 3μ M1M0 via	13.000
15.	M2 crack over a 3μ M2M0 via	12.438
16.	M2 crack over a 2μ M2M0 via	5.625
17.	M1 crack over a 3.5μ M1M0 via	4.875
18.	Crack in 4μ M2 over an M1 edge	4.750
19.	M2 crack over a 3μ M2M1via	3.688
20.	Crack in 3μ M2 over an M1 edge	3.250
21.	M1 crack over a 2.5μ M1M0 via	2.208
22.	Crack in 2μ M2 over an M1 edge	1.792
23.	M2 crack over a 2μ M2M1 via	1.774
24.	Short between M2 & M1 over M1 edge	0.431
25.	Short between M2 & R2 over R2 edge	0.078

Test chips from eight wafers were received from HYPRES. This represents a production span of five months for the foundry. It has to be noted that these wafers are released in the months immediately after the renovations in the HYPRES foundry. Some of the high percentage of the defects could be due to this or might have influenced the process. Twenty-three chips were tested at room temperature, from the eight wafers.

All of the predicted defects had been detected in at least one of the test chips. A part of the summary of the statistical result is graphically presented in Fig. 4. The x-axis represents the wafer number and the y-axis the percentage of the detected defects in various structures. The average value of the defect percentage

per wafer for each structure was used for the data points. As seen in Fig. 4, some of the structures are heavily affected. These defects, the ones in the M3-M2, the M3-M1 and the M3-M0 vias, are being affected by an error in one of the top layers (R3), the Pd-Au top layer which is being used for bonding as well as low-value resistances. This was caused due to the remnants of the under etched R3 over the M3 layer creating additional conductive paths since there is no isolation layer present between the two layers.

An example of the detected defect is presented in Fig. 5. Here an interlayer short between the M3 and M2 layers has occurred at the M2 edge. The ranking of the probable defects in the process is presented in Table I. The first column gives the rank of the defects presented in the second column, and the third column shows the percentage of defect for the particular structure. The number of units analyzed ranges from 1500 to 5100 for various structures. Due to the less number of test chips per wafer, detailed information like defect density per wafer requires further measurement and analysis. More information on the conducted experiments and results are available in [11].

VI. Conclusion

We have conducted an investigation on the HYPRES process which is being widely used for the realization of SCE circuits. The presented study revealed the probable defects in the process. A test chip was developed using structural testing approach for the process. Measurements from the processed chips show that the predicted defects are realistic. As per the measurement results, the major problem seems to be with the step-coverage of interconnect vias. A ranking of defects was prepared on the basis of the measurement results. This information will be useful for inductive fault analysis while developing an automatic test-pattern generation (ATPG) approach for SCE circuits developed in this process. The details of further study on ATPG and defect behavior of SCE circuits are subject for a future paper.

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