The Charge Plasma P-N Diode

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***Abstract*—A simulation study on a new rectifier concept is presented. This device basically consists of two gates with different workfunctions on top of a thin intrinsic or lowly doped silicon body. The workfunctions and layer thicknesses are chosen such that an electron plasma is formed on one side of the silicon body and a hole plasma on the other, i.e., a charge plasma p-n diode is formed in which no doping is required. Simulation results reveal a good rectifying behavior for well-chosen gate workfunctions and device dimensions. This concept could be applied for other semiconductor devices and materials as well in which doping is an issue.**

***Index Terms*—Charge plasma (CP), current, MOS devices, semiconductor device modeling, simulation.**

I. Introduction

IN SEVERAL R&D roups, ultrathin SOI devices and ultranarrow FinFETs are actively investigated. Rectifying junctions are essential in just about every electronic component, including thin-layer devices. For fabricating p-n junctions with nanodimensions, the key issue is doping control: doping fluctuation (see, e.g., [1] and [2]), doping activation (see, e.g., [3]), and obtaining steep doping profiles yielding a low temperature budget.

Another route which is being explored is the Schottky-based devices in SOI [4]. In these devices, abrupt source and drain junctions are formed between the metallic contact and the silicon body.

An alternative approach of employing metals or silicides in devices is schematically illustrated with the rectifier, recently proposed [5], as shown in Fig. 1, i.e., the charge plasma p-n diode (CP diode). Here, two separate metallic gates are placed on top of a thin silicon body. The gates are isolated from the top of the body by a dielectric layer, and each forms a contact at both sides of the silicon body.

There are two essential features in this concept. First, the workfunctions of the gates should be different from that of silicon, in which $\phi_{m,C} < \chi_{\text{Si}} + (E_G/2)$ and $\phi_{m,A} > \chi_{\text{Si}} + (E_G/2)$ are the workfunctions of the cathode and the anode, respectively. Other parameters are the elementary charge (q), the electron affinity of bulk silicon $(\chi_{\text{Si}} = 4.17$ eV), and the bandgap of bulk silicon (E_G). For the best rectifying behavior, the difference between both workfunctions should be at least $\sim$0.5 eV. Second, the thickness of the silicon body should be less than the Debye length, i.e., $L_D = \sqrt{((\varepsilon_{\text{Si}} \cdot u_T)/(q \cdot N))}$ (ε_{Si} is the dielectric constant of silicon, u_T is the thermal voltage, and N is the carrier concentration in the body). For this situation, the charge underneath both gates in the silicon is primarily determined by charge carriers, and the depletion charge can be neglected irrespective of the doping concentration in the silicon layer. This is also illustrated in Fig. 2, showing simulated (1-D) vertical charge carrier distributions formed by employing an n-type metal contact on two different (p-type doped) SOI layer thicknesses. Both systems are at thermal equilibrium. For the 1-μm-thick SOI layer, the depletion charge is clearly present [Fig. 2(a)]. However, for a 15-nm-thick SOI layer, the

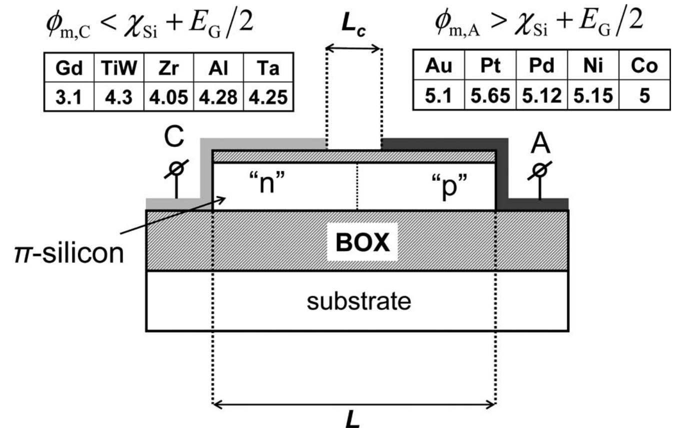

Fig. 1. Schematic cross section of the CP p-n diode. The electrodes C and A denote the cathode and anode, respectively, that consist of a metal, each with a different workfunction. Some practical metals with workfunction data [12] are shown above in a table at the left-hand and right-hand sides for the cathode and anode, respectively. All other parameters indicated in the figure are explained in the text. This device concept could also be made in (silicon) nanowires of Fins in which the influence of the metal workfunctions becomes more important. Note that by shrinking the device length L to the nanometer scale, the device becomes a tunnel diode strongly affected by the metal workfunctions.

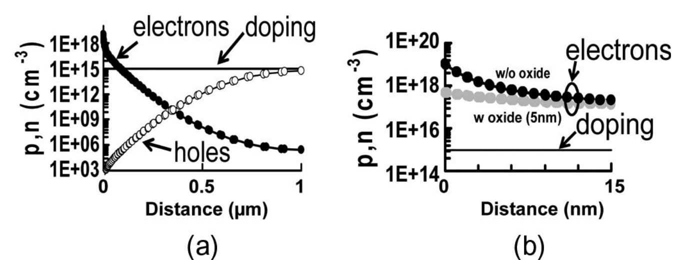

Fig. 2. Semi-classical simulations of 1-D vertical charge carrier distributions underneath an n-type metal contact ($\phi_{m,C} = 4.2$ eV) for two different SOI layer thicknesses: (a) 1 μm and (b) 15 nm. For (b), the distributions are shown for both a pure metal–silicon junction (black symbols) and that for a gate with an oxide thickness of 5 nm (gray symbols). For the p-type doping concentration in the silicon, $N_A = 10^{15}$ cm^{-3} was taken.

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electron concentration dominates the charge in the silicon body [Fig. 2(b)]. Hence, the layer conductivity is determined by the metal adjacent to the layer. By employing a thin insulating layer between the metal and the silicon, and therefore forming a gate, the electron concentration reduces but has a more uniform distribution compared to a pure metal–semiconductor junction.

As shown in Fig. 1, at thermal equilibrium due to the low value of $\phi_{m,C}$, an electron plasma is formed at the cathode of the diode. Likewise, at the anode, a hole plasma is formed due to the high $\phi_{m,A}$, and therefore, a CP diode is formed. The current is strongly controlled by the gates.

This letter discusses simulation results performed on the CP diode, revealing good rectifying behavior and a low series resistance. The results are compared to simulation results obtained from conventional uniformly doped p-n junction diodes, with the same device geometry (and, hence, in SOI). Although important for this comparison, reverse recovery and charge trapping are not part of this letter and are points for future studies. These issues could yield results to the detriment of the CP diode. Moreover, quantum confinement ($t_{\mathrm{Si}} < 15$ nm) and self-heating are important for ultrathin SOI layers, but we expect that these do not affect the general conclusions drawn here.

Note that in the carbon nanotube (CNT) field, some groups use an additional gate to dope the CNT [6]. Quite recently, various metals have been employed to form a rectifier in a CNT [7]. We believe that this CP concept could be applied for other ultrathin layer semiconductor materials and devices as well in which doping is an issue, such as amorphous silicon or polymers for TFTs, ultrathin silicon-based tunnel transistors, or even ZnO.

II. Results

Simulations have been performed with the ATLAS device simulation tool [8] applying the Boltzmann approximation with Philips' unified mobility model [9], doping-induced bandgap narrowing model [10], and the recombination model described in [11], all with default silicon parameters.

In this letter, the following device parameters have been used (see Fig. 1). The buried-oxide layer is 50 nm thick, the total device length (L) is 1 μm, the distance between the electrodes (L_c) is 0.10 μm, and the gate oxide layer thickness is 5 nm. Furthermore, a 20-nm-thick intrinsic silicon layer has been considered, and the cathode contact workfunction is $\phi_{m,C} = 4.17$ eV. The anode workfunction $\phi_{m,A}$ has been varied between 4.9 and 5.6 eV. Moreover, for both contacts, ideal interfaces have been assumed. In practice, metals such as aluminum for the cathode and, e.g., platinum or nickel for the anode could be adopted [12].

In Fig. 3, the lateral charge carrier distributions for three different forward biases (0, 0.5, and 1.0 V) are shown, with $\phi_{m,A} = 5.1$ eV. At low bias, the p-n product near the junction equals $p \cdot n = n_i^2 \cdot \exp(V_D/u_T)$, with n_i being the intrinsic carrier concentration, as can be seen at the intersections (or electrical junctions) of the hole and electron concentrations at 0 and 0.5 V. At the metal contacts, the majority charge carrier concentration increases due to the Schottky effect.

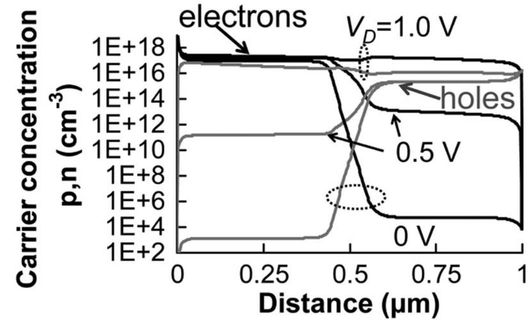

Fig. 3. Simulated 1-D charge carrier distributions in the CP p-n diode as a function of the horizontal direction for different biases: $V_D = 0$, 0.5, and 1.0 V. The silicon thickness $t_{\mathrm{Si}} = 20$ nm, the total device length $L = 1$ μm, gate oxide thickness is 5 nm, the cathode workfunction $\phi_{m,C} = 4.17$ eV, and the anode workfunction $\phi_{m,A} = 5.1$ eV.

For a low bias, the current is determined by diffusion. When the forward bias in the diffusion regime is increased, the electron concentration increases in the cathode region, shifting the electrical junction toward the anode region. For yet higher forward voltages (e.g., 1.0 V), the charge carrier concentrations increase drastically because of the high-injection effects, which can be made less significant by increasing $\phi_{m,A}$ and decreasing $\phi_{m,C}$. These high-injection effects are strongly affected by the gate potentials and, hence, also the polarity of the electrodes.

At low bias, the band diagram shows the same behavior as the conventional p-n junction (not shown in this letter). The built-in potential is about 0.70 V, and the applied voltage is concentrated near the electrical junction. However, at thermal equilibrium, the potential shows a linear curve indicating that there is no charge in the center of the device. This is, of course, due to the intrinsic silicon body. This was also observed for a device formed by a fully depleted doped region in a thin silicon body with a thickness below the Debye length. The lateral electric field is determined by the (limited) distance between the electrodes (L_c). For a reduced L_c, a less linear behavior in the potential can be obtained, although this is a technological challenge. A way to avoid this could be employing another terminal on top of both terminals that is isolated with a dielectric layer and connected to one of the terminals having the same workfunction. For the current drive, however, L_c is not a critical parameter.

Fig. 4 shows simulated Gummel plots for the CP diode for various $\phi_{m,A}$ and those of the conventional uniformly doped p-n diode counterparts having the same device geometry. For the latter, the doping concentrations are chosen to match the diffusion currents to those of the CP diodes. As can be seen, the currents of the CP diodes are strongly dependent on the workfunctions. All devices clearly exhibit rectifying behavior. Due to high-injection effects, the lowly doped symmetrical p-n junctions show lower maximum current levels than the CP devices having the same low-injection current densities. Uniformly doped asymmetrical p-n junctions show more or less the same results compared to the (asymmetrical) CP diodes. For both types of devices, high-injection effects are less important because of the high charge carrier concentration on one side of the junction.

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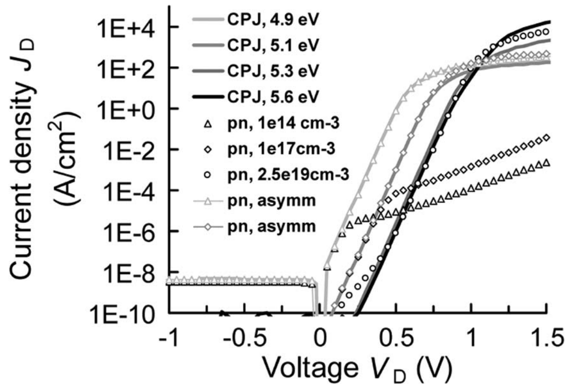

Fig. 4. Simulated current density data J_D of the CP p-n diode (drawn lines), the conventional uniformly doped p-n junction diode having the same device geometry (symbols) versus the diode voltage $V_D(T = 300\text{ K})$. In these data, the workfunction of the anode $\phi_{m,A}$ in the CP p-n diode has been varied between 4.9 and 5.6 eV, and the doping concentration in the conventional p-n junction diode has been assumed to be 10^{14}, 10^{17}, and $2.5 \cdot 10^{19}$ cm^{-3}. In the conventional asymmetrical p-n junction diode, these doping concentrations have been divided into halves on one side of the junction, and at the other side of the junction, a doping concentration of 10^{19} cm^{-3} has been taken. All other device parameters are the same as indicated in the caption of Fig. 3.

III. Conclusion

In this letter, a new device concept, the CP diode, has been investigated with the aid of device simulations. Simulation results reveal a good rectifying behavior depending on the workfunction of the gates and device dimensions. This concept could be applied for other semiconductor devices and materials in which doping is an issue. Topics such as reverse recovery and charge trapping remain points for future research.

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