

TESTABILITY ENHANCEMENT OF A BASIC SET OF CMOS CELLS

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SUMMARY

Testing should be evaluated as the ability of the test patterns to cover realistic faults, and high quality IC products demand high quality testing. We use a test strategy based on physical design for testability (to discover both open and short faults, which are difficult or even impossible to detect). Consequentially, layout level design for testability (LLDFT) rules have been developed, which prevent the faults, or at least reduce the chance of their appearing. The main purpose of this work is to apply a practical set of LLDFT rules to the library cells designed by the Centre Nacional de Microelectrònica (CNM) and obtain a highly testable cell library. The main results of the application of the LLDFT rules (area overheads and performance degradation) are summarized and the results are significant since IC design is highly repetitive; a small effort to improve cell layout can bring about great improvement in design.

KEY WORDS Layout-level design for testability Realistic fault

INTRODUCTION

Because of the continuous evolution and the improvement of CMOS technology, there is still an increase in the demand for reliability in integrated circuits. To achieve this level of reliability there are two aspects that must be approached: the quality of the production process and the test strategy.¹ The second aspect (the test strategy), for realizing highly reliable products, is our main objective. Our aim is to show that physical design for testability can be used to improve the quality of the layout in order to improve testability, yield and reliability.

During the manufacture of an IC, disturbances in the process and contaminants (dust particles, . . .) may cause incorrect behaviour. These defects can affect multiple integrated circuits on the same wafer (global defects) or a small area on a single IC (local defects or spot defects).

The following types of defects have been reported as main causes of CMOS IC failure: bridging, open drain or source, open gate, transmission gate opens, gate oxide shorts, parasitic transistor leakage and punch-through defects, etc.²

The stuck-at fault is the main fault model used in automatic test pattern generation (ATPG) and fault simulation but the single stuck-at model is insufficient for describing faults that may occur during the manufacture of CMOS circuits, and in consequence, testing based on the stuck-at fault model cannot achieve zero defects in CMOS ICs.³

For this reason, it has been necessary to introduce realistic fault models: opens (stuck-opens, floating gates . . .) and shorts (stuck-ons, gate oxide shorts, bridgings, floating gates . . .)⁴ which depend on the technology and on the circuit layout. As realistic faults we refer to those originated by likely physical defects induced during IC manufacturing. Analysis of realistic physical failures in digital circuits is necessary to gain an understanding of the effects of faults on the functional behavior of the circuits, to derive efficient test sets, and to redesign circuits for improved testability.

Once the testability problem has been identified, we must search for ways to redesign the circuit with minimal overheads. Optimal redesigning seeks to decrease test generation/application costs as well to increase fault coverage and diagnosticability.

Therefore, in order to enhance the testability of the CMOS cell library designed at the Centre Nacional de Microelectrònica⁵ we have redesigned it using basic layout-level design for testability (LLDFT) rules^{6,7} to prevent some realistic faults (opens and shorts) from occurring.

The main advantage in applying these rules in a cell-based design process is that a new design for each cell has to be made only once, and this work should be oriented by a test engineer. Because our objective is to enhance the testability, we can devote more time to this task and we obtain a more compact and developed design. Otherwise, if these rules are applied in every new design, the whole circuit will

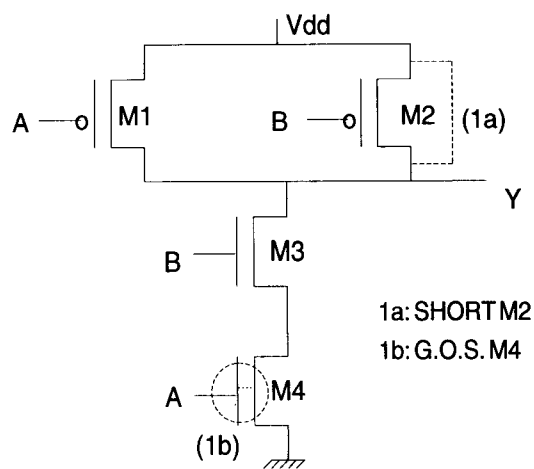


Figure 1. NAND gate with short fault in transistor M2 and gate oxide short in transistor M4

need to be redesigned and this may give rise to area overheads and an increase in design time (because it takes less time to apply these rules to a cell library than directly to a full-custom design).

The short faults (including some floating gates) are very likely to appear and are detectable by means of $IDDq$ measurements, which are assumed to be a good test technique in their detection.^{8,9} For example, in Figure 1 we can see a NAND gate with two kind of faults: a short in transistor M2 and a gate oxide short in transistor M4.

In Figure 2 we can see the simulation results of the NAND without defects.

The result of simulation with a short in transistor M2 appears in Figure 3(b) and the result with a gate oxide short in transistor M4 is shown in Figure 3(c). In both cases a great amount of quiescent power supply current ($IDDq$) is noticeable in comparison with the result of simulation without any defects (see Figure 3(a)).

Current testing is an adequate technique for this kind of fault. For this reason we would propose a test methodology based on the incorporation of BIC (built-in current) sensors in a cell-based design strategy. In the BIC testing technique current sensors will be applied to monitor the amount of quiescent current in the power lines.¹⁰

Otherwise, the open faults are difficult to detect and mean an increase in the test pattern generation cost (i.e. robust sequences, minimum test sequence composed of two vectors, . . .³) in comparison with classical ATPG cost for stuck-at faults, and it is better to avoid them. To review the problem, consider a stuck-open in one branch of a two-input CMOS NAND gate shown in Figure 4. For fault detection a two-pattern test sequence $\langle V1, V2 \rangle$ is required. The $V1$ initializing pattern is used to set the output of the faulty gate to the opposite value to be charged to when the actual $V2$ test pattern is applied. Table I shows the valid two-pattern test sequences for detecting a stuck-open fault in one of the branches of the two-input NAND gate in Figure 4.

For this reason, we present the main results obtained applying basic LLDFT rules to design out some open faults and to make the remaining opens easier to detect.

We work with these LLDFT rules and we analyse which rules are best to apply to cells of the CNM library (with CNM technology) and we obtain the consequences of their application. Because we work with a cell library (of limited height) we only modify the width parameter when we apply some rules. Therefore, when the electrical behaviour is worse, it may be possible to know directly which transistor width has to be changed to achieve the expected electrical behavior.

In short, our objective is make guidelines for the designer in order to enhance the testability of his designs (our rules are layout-oriented). With these

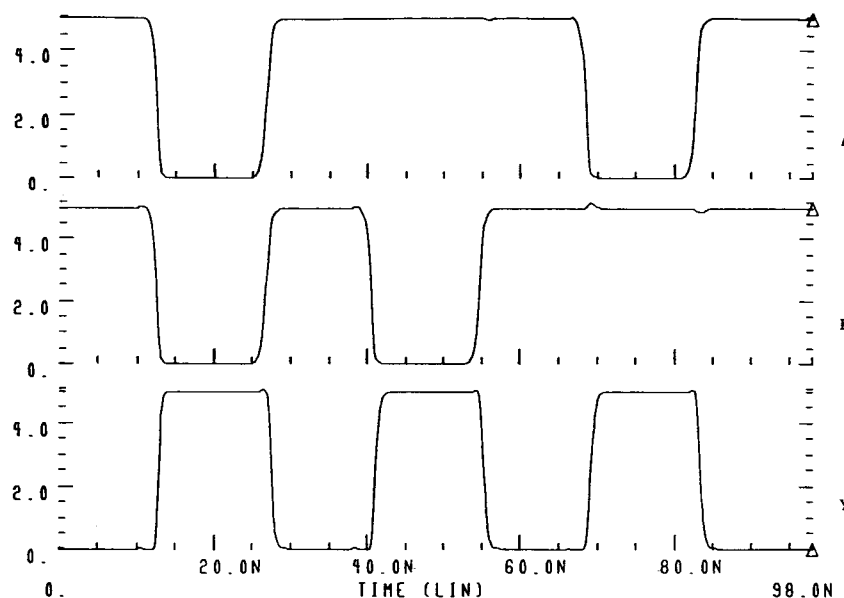


Figure 2. Simulation results of the NAND gate without defects

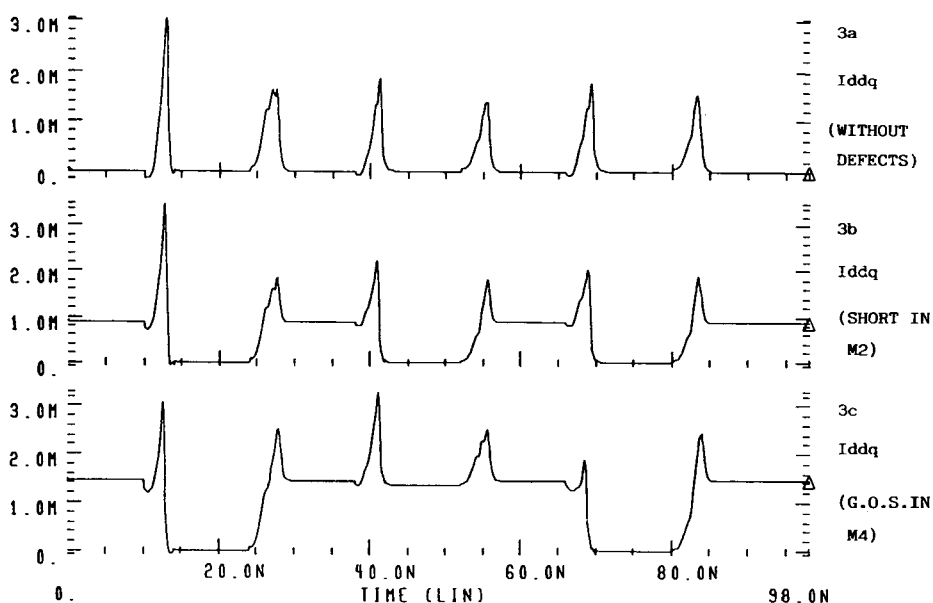


Figure 3. (a) IDDq of the NAND gate without any defects, (b) IDDq of the NAND gate with a short in transistor M2, (c) IDDq of the NAND gate with a gate oxide short in transistor M4

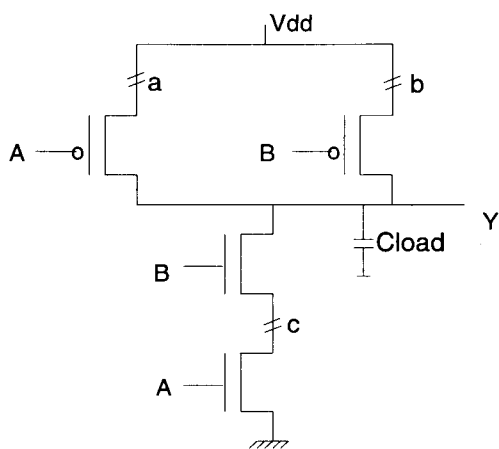


Figure 4. Stuck-open faults (a, b, or c) in one branch of a two-input CMOS NAND gate

Table I. Two-pattern test sequences to detect a stuck-open fault in one of the branches of the two-input NAND gate

Branch	INIT (T1)		TEST (T2)	
	A	B	A	B
a	1	1	0	1
b	1	1	1	0
c	0	-	1	1
	-	0	1	1

guidelines, our purpose is to exploit all ATPG that use stuck-at fault models. We can use them to evaluate testability problems and to enhance IC quality, yield and the reliability of final products.

PREVIOUS WORK

In previous work by Galiay *et al.*¹¹ a set of layout rules for MOS circuits was presented based on LLDFT. Since that work, different approaches have appeared on how to attach LLDFT and, at present, there are two main groups:

- (a) switch-level techniques,¹²⁻¹⁷ which modify the circuit at transistor level. This technique basically consists of adding transistors. In 1987, Liu and McCluskey¹⁴ added an inverter to avoid stuck-on and stuck-open faults. In 1991, Jayasumana *et al.*¹⁷ added one FET to avoid stuck-open faults (see Figure 5)
- (b) layout level techniques^{6, 7, 18-21} which modify the layout (they do not add any control lines but require the designer to work at a low-level design representation). In 1987 Koeppel¹⁹ presented a set of layout rules to cope with

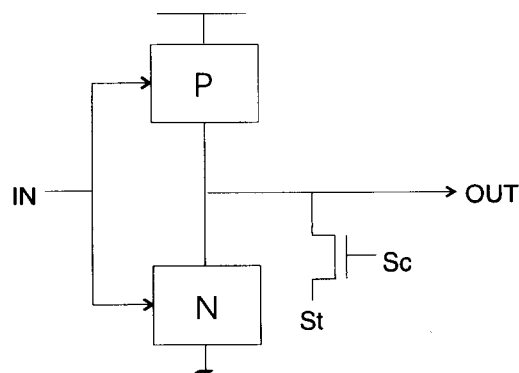


Figure 5. Testable CMOS design using the nMOS transistor proposed by Jayasumana

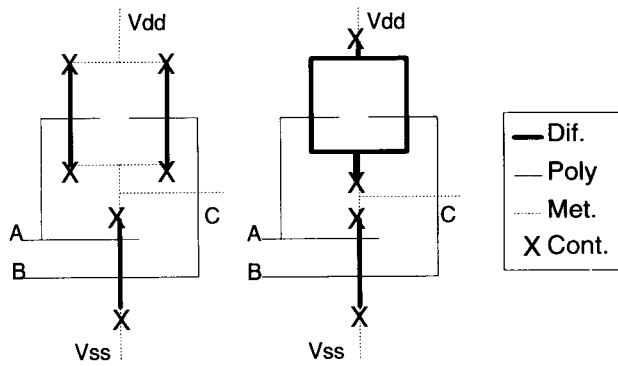


Figure 6. CMOS NAND gate proposed by Koeppe: (a) conventional stick diagram, (b) alternative to avoid an open at the source or drain terminal

stuck-opens (see Figure 6). In the same year, Vierhaus⁷ proposed a set of rules to avoid bridging faults. In 1989, Soden *et al.*²⁰ explained some layout modifications. In 1990, Levitt *et al.*²¹ made a summary and enhanced testability at layout level. In 1991, Teixeira *et al.*⁶ summarized some rules to avoid faults.

In general, all these works show a set of rules that must be applied in a whole design. As a result, the

designer has to know everything related to testability and specifically to LLDFT, to prevent some realistic faults (short and open faults), which means an extra work. For this reason and in order to extend these techniques to the semi-custom design, we have adapted this methodology to cell-based designs starting with the application in a CMOS cell library.

BASIC LLDFT RULES

As our strategy is to modify the layout^{6, 11} in order to reduce the frequency of open faults in each cell of a basic library, we propose a set of rules which may help to avoid open faults or to convert them into easily testable stuck-at faults:

- (a) redundancy of contacts
- (b) application of a ring-shaped or closed loop conductive layer
- (c) duplication of interconnecting layers and inputs (redundant conductive paths)
- (d) placement according to the signal flow
- (e) interconnection of transistor channels with diffusion layers.

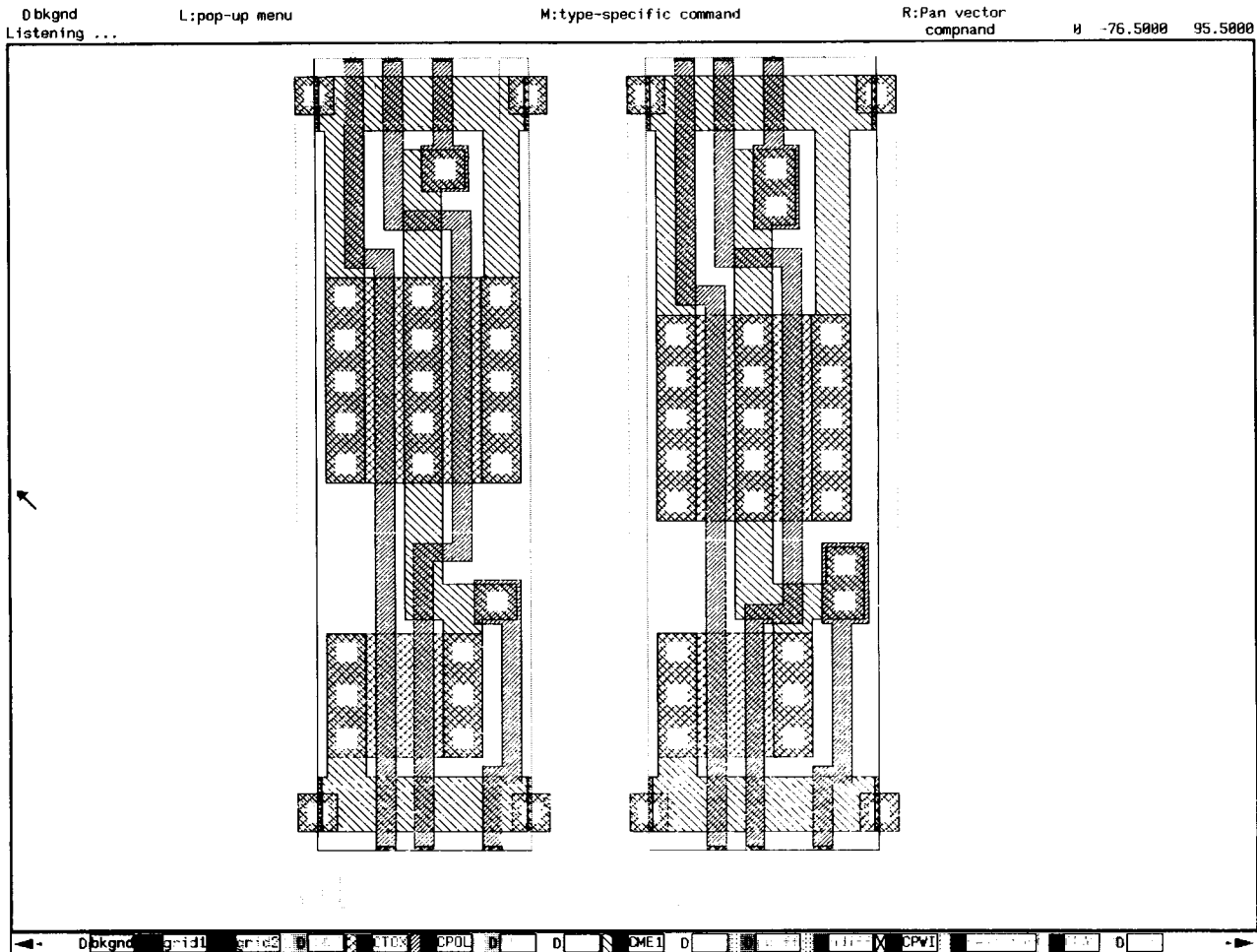


Figure 7. CMOS NAND gate: (a) old layout, (b) redesigned layout with contact duplication

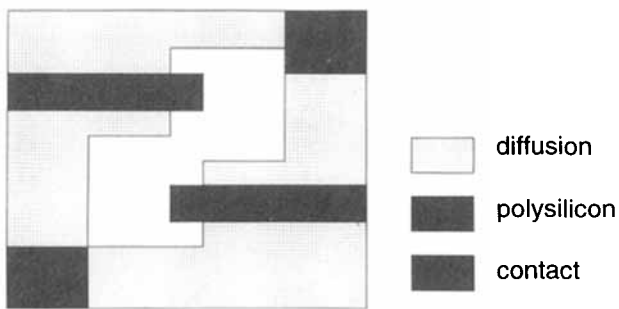


Figure 8. Diffusion ring based on Koeppel

Redundancy of contacts

Since the contacts are elements that have a high probability to produce opens, we can reduce the frequency of this fault in the circuit if we multiply the number of these elements using a stream of contacts instead of isolated ones (Figure 7).

Partial application of a ring-shaped or closed loop conductive layer¹⁹

In order to prevent an open in a source or drain terminal we can avoid all contacts and metal lines and replace the whole parallel structure with a ring-

shaped LOCOS structure. An open fault of the ring-shaped structure itself does not need to be considered. Furthermore, any open fault in the contact between the ring and V_{dd} (V_{ss}) or the gate output will break the whole pull-up (pull-down) path and it will be detected by a stuck-at test pattern set.

An example of a ring based on previous structure is shown in Figure 8.

It is not necessary to maintain the transistor width in the whole ring. Some parts of the ring are simply interconnecting signal lines and may have the minimum line width of the diffusion layer (in order to decrease area and diffusion resistance).

In Figure 9 an example of the application of this rule to an OAI22 cell is shown. In the new OAI22 cell we show a ring of diffusion in the pull-down path.

Duplication of interconnecting layers and inputs (redundant conductive paths)

Whenever possible, it is recommendable to duplicate some layers corresponding to command input lines or interconnections between internal nodes of the transistor networks, in order to reduce the appearance probability of opens in this layer (Figure 10).

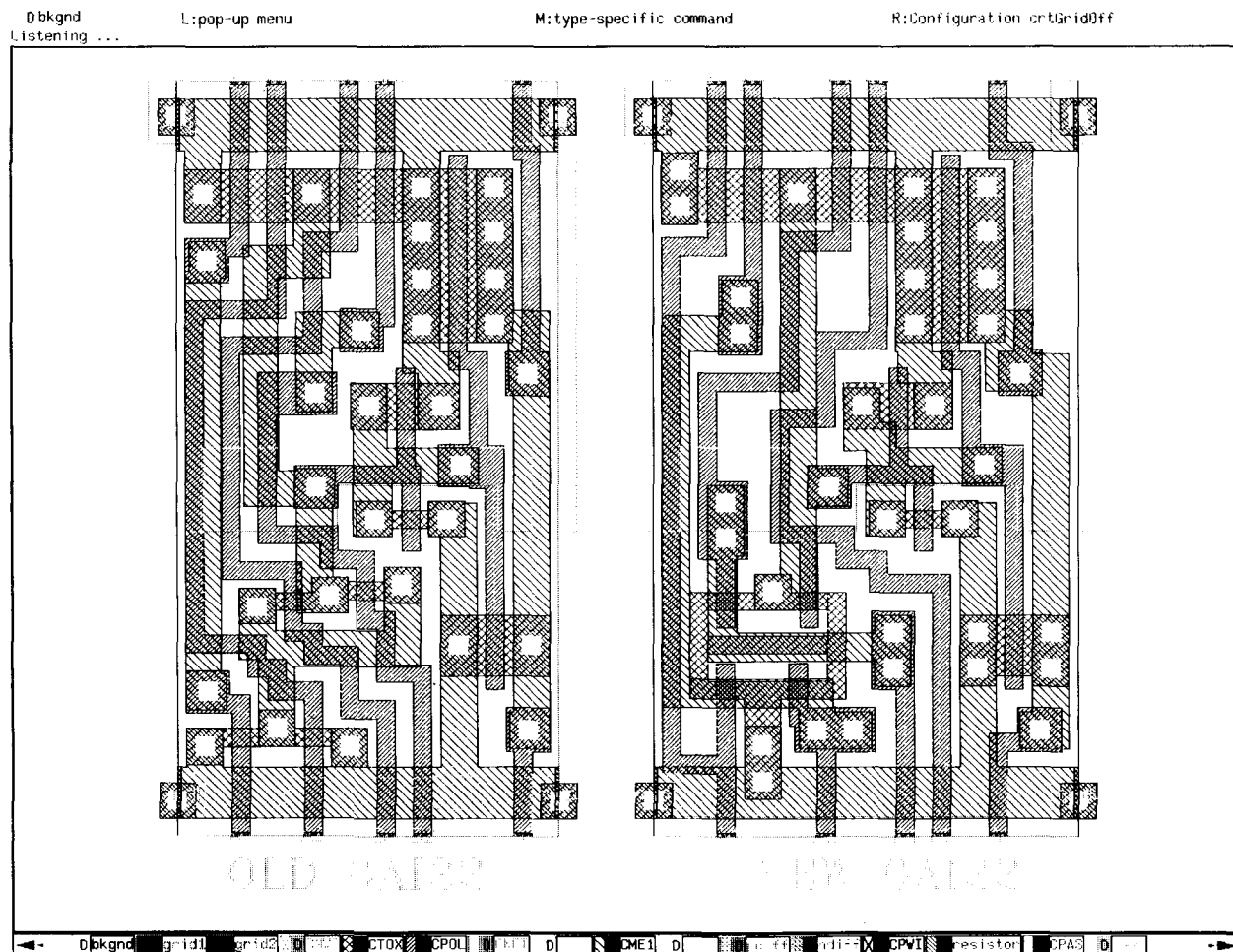


Figure 9. Old OAI22 cell and new cell with a diffusion ring in the pull-down path

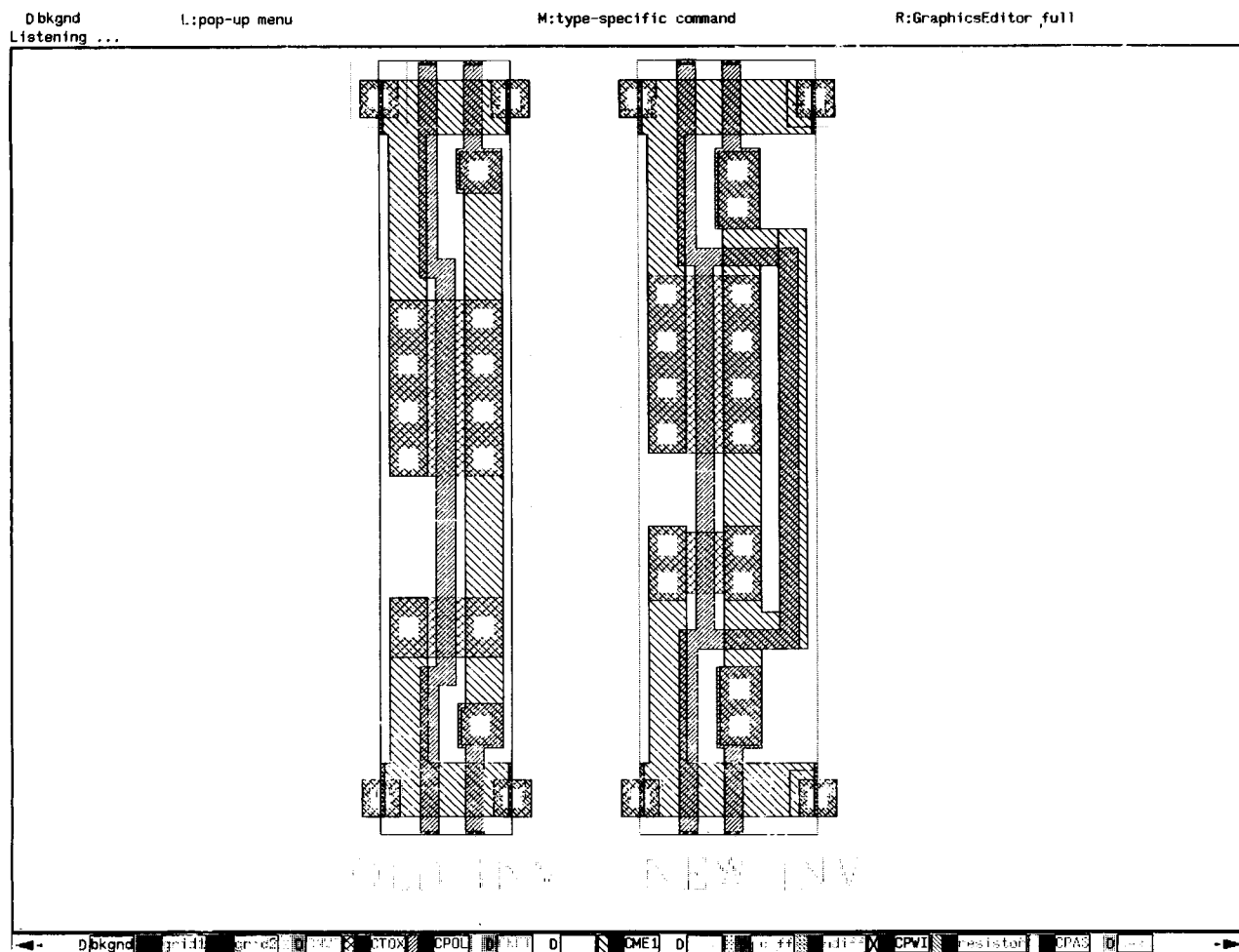


Figure 10. Old INV cell and redesigned cell with duplication of interconnection layers and inputs (redundant conductive paths)

The previous rules are oriented towards avoiding open faults; however other authors have also proposed some LLDFR rules for preventing bridging.^{6, 7, 11}

Usually, to avoid this kind of fault, the spacing between the adjacent conductive layers of the same material has to be increased. Many of these rules convert bridging faults into stuck-at, although some are difficult for a designer to apply (because they take up a lot of area and would deteriorate electrical behaviour).

Placement according to the signal flow

In our work, in some cells (Figure 11) we have applied a basic rule to prevent feedback bridging within a cell ('gates in larger macros should be placed according to the signal flow, in other words, avoid crossovers of input and output lines of a logical element'^{6, 7}).

Interconnection of transistor channels with diffusion layers

Whenever possible, we apply the rule that creates lines in diffusion layer (the diffusion layer has a low probability for open faults¹⁹) and the intercon-

nection of MOS transistor gates is made of polysilicon.

Finally we have applied some rules together in the same cell. In Figure 12 we can see a NOR cell and a redesigned cell. We have applied rule (b) in the pull-down path. Again, it is not necessary to maintain the transistor width in the whole ring. If an open occurs in the common contact it could be detected as a stuck-at fault, and for this reason we have only multiplied the rest (rule (a)). On the other hand we have also duplicated the input gate to avoid an open in this layer (rule (c)).

RESULTS

In general, our aim is to apply the rules explained earlier, to obtain a new library in which physical testability is enhanced, taking into account the design trade-offs: silicon area overheads and performance degradation.

The following paragraphs show the main results obtained by application of LLDFR rules in our library. These results were obtained simulating each rule alone in order to see the different behaviour and area increase. These results enable us to obtain certain conclusions related to the application of these rules. In consequence, we will not always

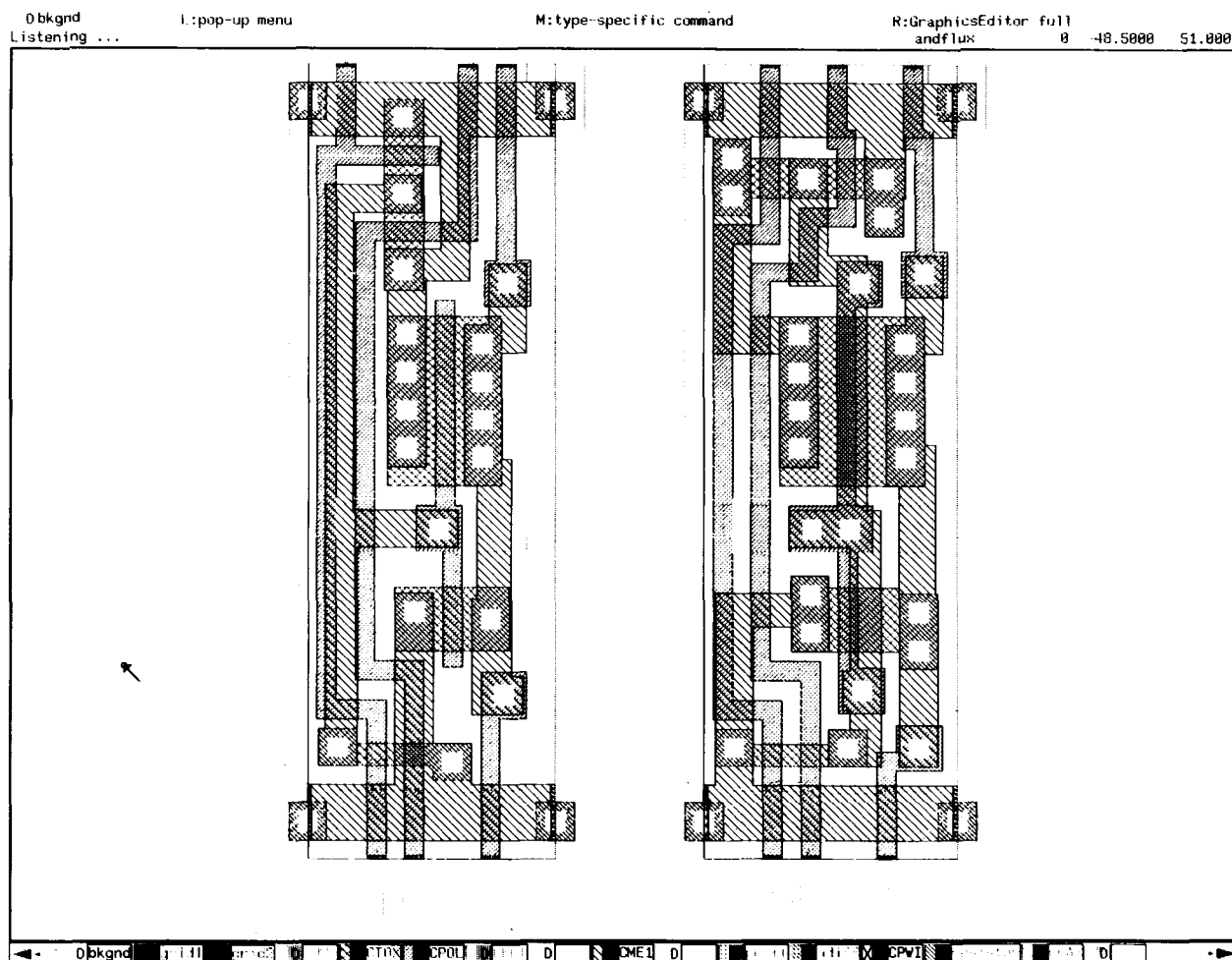


Figure 11. Old AND cell and redesigned cell placing gate according to the signal flow

apply these rules together because it is important to find an equilibrium between the added cost (in area overheads—performance degradation) and the improvement in the faults occurrence.

(a) Redundancy of contacts

Table II shows the results obtained from a set of cells in which the contact was duplicated.

The area and the electrical behaviour variation (rise time, fall time, rise delay and fall delay) of the new cells are presented in comparison with the old results. A positive percentage is an increase in area or time with respect to the old cell, whereas a negative percentage is a better behaviour than that of the old design (for example the new XNOR cell).

In almost every cell, contact duplication causes an equal or slightly different electrical behaviour or area increase. For this reason it would be no problem to apply this rule but first duplicate important contacts (causing faults which are difficult or impossible to detect if an opening occurs) and later, if there is space, duplicate the other contacts.

(b) Partial application of a ring-shaped based on Koeppel¹⁹

We can use a diffusion or polysilicon ring that connects the transistors. We can see in Table III that if the diffusion ring is placed in a pull-up part (with great diffusion resistance) the electrical behaviour is worse than in the pull-down part (with low diffusion resistance). For this reason, the electrical behaviour is better in a NOR gate than in a NAND gate.

(c) Duplication of interconnection layers and inputs

Whenever possible, it is recommendable to duplicate some layers corresponding to input lines or interconnections between internal nodes, in order to reduce the chance of openings occurring. The duplication of lines in general causes an enormous increase in area and worse electrical behaviour (see Table IV) except in the NOR gate.

This kind of rule could only be applied when importance is given to the equilibrium between the added cost (in area of electrical behaviour) and the improvement in fault occurrence.

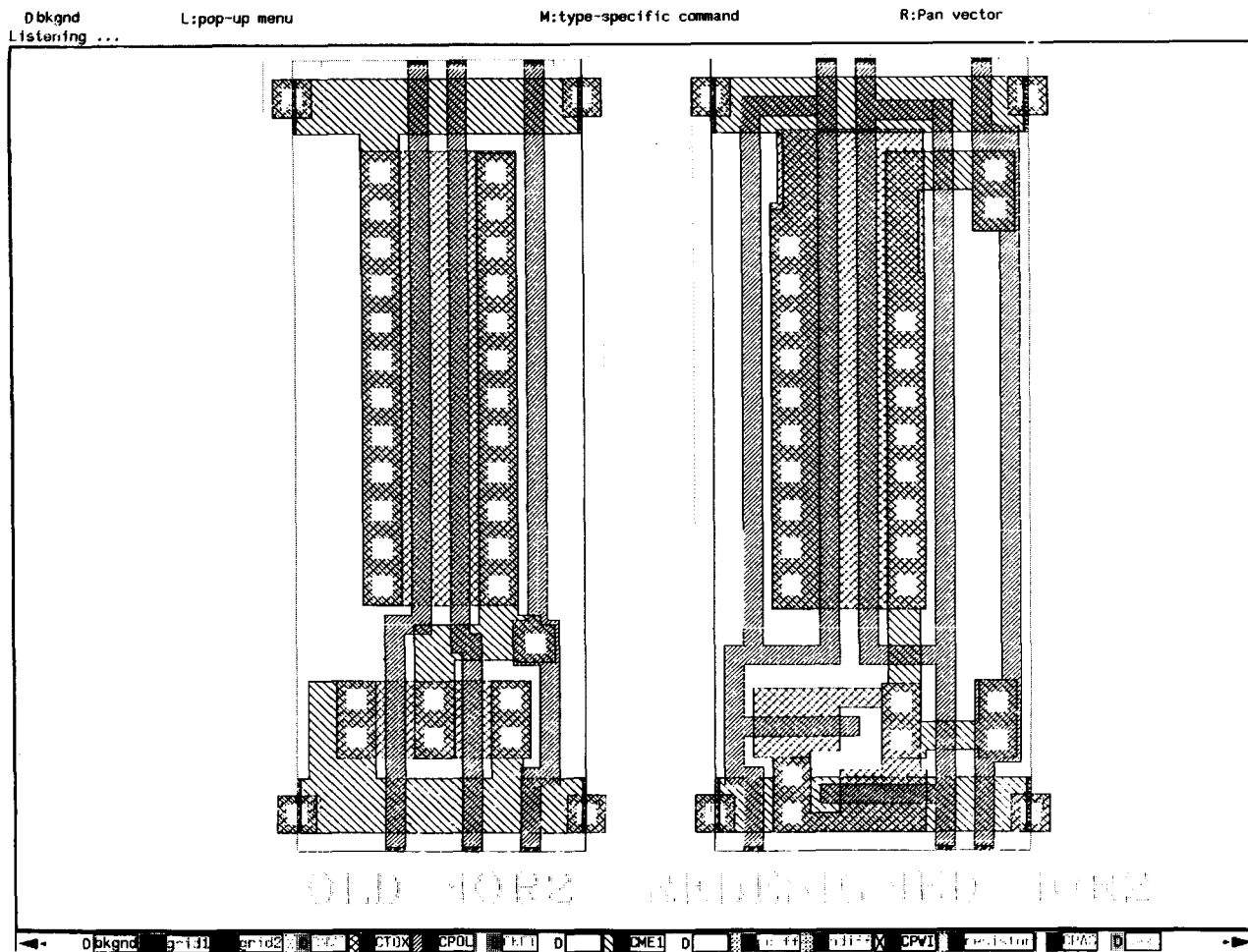


Figure 12. Old NOR cell and a redesigned cell applying rules (a), (b) and (c)

Table II. Results obtained over a set of cells where the contact has been duplicated

Cell	Area, %	Rise time, %	Fall time, %	Delay rise, %	Delay fall, %
INV	0	0.8	0.8	0.6	0.6
NAND	0	0.5	0.6	1	0.7
NOR	0	0.2	0.4	0.2	0.3
AND	0	6.1	5.8	12	11.4
OR	0	5	4.2	4.9	5.7
XNOR	1	-0.2	0.2	0.1	-0.1
AOI21	0	1.5	1.9	3.1	2.3
AOI22	0	1.7	3	8.3	7.2
OAI21	0.4	7	2.2	9.2	5.6

Table III. Results obtained over a set of cells where we use a diffusion or polysilicon ring that connects the transistors

Cell	Area, %	Rise time, %	Fall time, %	Delay rise, %	Delay fall, %
NAND	6.4	44	-8.7	36.7	-6.2
NOR	5.6	0.8	1.8	0.2	-0.3
AND	3.1	4.8	8.8	14.7	15.8
OR	15	4.6	10.5	7.4	8
AOI21	9.9	3.1	-8.9	10.2	6.3
OAI21	2	7.1	2.8	5.1	4.5
OAI22	10	1.3	1.3	3.6	4.8

Table IV. Results obtained over a set of cells where the input-output lines have been duplicated

Cell	Area, %	Rise time, %	Fall time, %	Delay rise, %	Delay fall, %
INV	25	4	4	7	7
NAND	31	3.7	4.5	5.3	4.3
NOR	0	1.5	0.6	1.9	0.8
OR	36.8	1.3	2.3	1.5	-0.1
AND	25.6	10	10	26	21

Table V. Results obtained over a set of cells where we avoid crossovers of input and output lines

Cell	Area, %	Rise time, %	Fall time, %	Delay rise, %	Delay fall, %
AND	0	9.6	7.9	8.5	6.1
OR	0	5.6	4.9	4.2	4.6

(d) Placement according to signal flow

In this case the aim is to prevent feedback bridging within a cell. In other words, to avoid crossovers of input and output lines of a logical element. This causes very poor electrical behaviour in the AND gate (see Table V), but good electrical behaviour in the OR gate. This rule is strongly dependent on layout and it is difficult to establish an optimal criterion for its use.

CONCLUSIONS

By way of conclusion, the basic LLDFT rules can be used to improve layout quality and to enhance testability and reliability.

Are overheads are always less than 10 per cent, except when the layers and inputs have been duplicated (rule (c)). There is degradation in electrical behaviour around the 10 per cent mark, except when rule (b) has been applied to the AND gate (application of the Koeppe ring).

It seems reasonable to use these rules to avoid some opens or to use easier fault models (i.e. classical stuck-at), when the new cells do not vary in more than 10 per cent from the standard cell nominal value.

These results also demonstrate that it is possible to improve circuit testability by improving the physical design. We have focused the results of this work on avoiding open faults; however, it could also be applied to bridging faults.

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