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COMPONENT LIFETIME MODELLING

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SUMMARY

There are two approaches to component lifetime modelling. The first one uses a reliability prediction method as described in the (military) handbooks with the appropriate models and parameters. The advantages are:

(a) It takes into account all possible failure mechanisms.
(b) It is easy to use.

The disadvantages are:

(a) It assumes a constant failure rate which is often not the case (infant mortality).
(b) It contains no designable parameters and therefore it cannot be used for built-in reliability.

The second approach is to model the different degradation mechanisms and to incorporate this into an (existing) circuit simulator. Here we have also advantages and disadvantages which are mostly complementary to those of the first method.

KEY WORDS Lifetime modelling Reliability Simulation Component reliability System reliability Electromigration Hot carriers Handbooks MIL CNET BT Failure rate ESD IC MOS

1. INTRODUCTION

Component lifetime modelling deals with reliability prediction. This prediction is done with the aid of data collection on existing components and subsequent fitting of data with suitable models. The benefits of proper models are that we can do predictions for new components and systems in the development/design phase and so finally achieve a better reliability.

In designing electronic circuits and systems a large effort is made to make sure that the design is right first time, at least as far as simulation can predict. The reason is simple: the large costs of processing designs. The aspects of design here refer to the electrical characteristics under all possible loads the circuit might face. An obvious and necessary extension is to make sure the design is reliable with respect to endurance failures such as material breakdown under prolonged electrical or thermal, mechanical or even chemical stress. Reliability tests are normally carried out after production and translated into failure data in handbooks. However, a growing knowledge becomes available of the physical mechanisms of various breakdown phenomena such as electromigration, ESD, junction breakdown, oxide wear out etc. With this knowledge it must be made possible to predict reliability behaviour at the design phase of circuits and systems. In the last few years several efforts on integrated circuits have been published, which are reviewed by Hu,[1] and progress in modelling with a stronger relation to the 'real' physics will make more accurate simulation possible. In our tutorial we will sketch two approaches. The first is an approach as described in handbooks and which is especially suited for systems with different components. In the second approach one particular degradation mechanism is being modelled and its contribution to the overall component degradation calculated. This approach is especially suited for integrated circuits. We will discuss how both approaches have their advantages and disadvantages.

2. GENERAL PROCEDURE

In this section we will describe the general procedure to be followed in either of the two approaches mentioned above. It contains the following steps:

Data collection

There are two sources of data, field returns or failures in accelerated testing. An important quantity is the failure rate λ which relates the number

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of failures to sample size and time interval by the formula

$$\lambda = \frac{n}{N\Delta t} \quad (1)$$

where n is the observed number of failures in time period Δt and N the sample size or number of systems. In the case of accelerated testing Δt is equal to the test period multiplied by an accelerating factor A.

Models

The purpose of models is twofold: first, they should allow a calculation of the reliability in practical use from data obtained in accelerated testing, or, secondly, the calculation of the reliability of new components or systems from data for existing components and systems. For the calculation in the first case we need proper acceleration factors in our models. For temperature stress the acceleration factor A is usually described by Arrhenius' law:

$$A = A^1 \exp(-E_a/kT) \quad (2)$$

where A^1 is a constant not depending on the temperature T, and E_a is the activation energy of the degradation process. For other stresses other relations have been found and incorporated into models.

We would like to emphasize here that models should contain designable parameters so that they can be used to optimize a new design with respect to reliability. In this way the concept of 'built-in reliability' can be pursued.

Results

Under this heading we will carry out a verification of the models, a confrontation of models with new results, indicate the shortcomings of the existing models and, finally, the ways followed to overcome these shortcomings. It should be noted that we have to deal often with complex systems with many components or with components such as ICs that are complex. Then calculations are only possible with relatively large computers. Therefore, we will pay attention to this area of computer simulation.

3. SYSTEMS APPROACH

In this section we will follow to a large extent the book written by one of the authors.[2] However, we will use the term 'system' instead of 'circuit' for a system with several components in order to avoid confusion with integrated circuits (which are considered here as components).

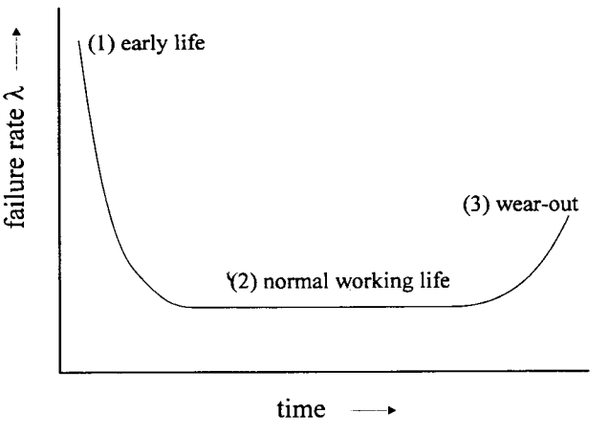

Figure 1. Bathtub curve showing the three most important failure rate phases of a product during its lifetime: (1) early failures (infant mortality), (2) normal operating life and (3) wear-out

3.1. *Data collection*

The failure rate of components in systems in the field is assumed to show a typical bathtub behaviour, as is sketched in Figure 1.

Three regions can be seen; first, the early life regime with a relatively high and in-time decreasing failure rate; secondly, the working life with a constant failure rate; and, thirdly, the increasing failure rate in the wear-out regime.

This is a sketch; how does it look in practice? Figure 2 shows the failure rate in an endurance test on a large number of integrated circuits made in bipolar and MOS technology.[3] All the different failure rate curves were derated to practical use condition via the above-mentioned equation (2) with a value of the activation energy of $E_a = 0{\cdot}7$ eV. Also the curves were normalized to a failure rate of 1 at the 300 h time point. In Figure 2 we may observe a continuously decreasing failure rate which shows signs of becoming constant only after an equivalent operating time as long as 10,000 hours. As indicated above, the second sources of data are the field

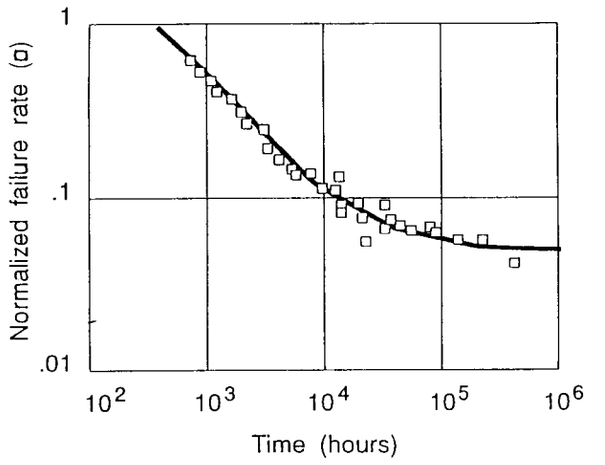

Figure 2. Measured failure rates for a large number of integrated circuits made in bipolar and MOS technology[3]

returns. Figure 3 shows the results of an extensive study[4] at Loughborough University on CMOS circuits failing in systems in the field. The time frame is now as long as 21,000 hours operating time. It can be seen that again the early failure rate is high and decreases to a lower level, but now over a 4000 hour period. It should be noted that the data in Figure 3 are from different sources, systems and environments, which may explain why there is a larger contribution from other mechanisms in the constant failure rate regime, mechanisms such as ESD and overstress. These are certainly absent in the failures in the endurance testing for the data in Figure 2. Of course when we want to calculate the component lifetime, or better its failure rate, then we have to incorporate these and all other mechanisms into a model.

3.2. *Models*

The models used in reliability prediction of components in general and integrated circuits in particular are registered in handbooks, which describe the failure rates for various types of classes (see Figure 4). A well-known handbook is the United States Department of Defense MIL-HDBK-217, the 'Mil Handbook'. In general a failure rate formula looks like

$$\lambda = \pi_a \pi_b \pi_c \qquad (3)$$

where π_a, π_b, etc. represent acceleration factors. It is assumed in all models to be described here that the failure rate is constant. It should be clear from the data in the previous section that this is not correct. This imposes a serious drawback on the models because the high early failure rate may be the dominant reliability hazard in system reliability.

The model for the failure rate in integrated circuits used in the Mil Handbook is given in Table I, together with a description of the parameters, influence factors and the origin of the parameters. Apart from temperature, most parameters used in the model are either related to device structure or to the application of the circuit. Especially the application-related parameters have the form of correction factors with values derived from heuristic data; no physical failure mechanisms are involved. It should be noted that the model does not contain any designable parameter to be used for optimizing the circuit for reliability performance. The quantities C_1 and C_2 in Table I could be considered as such because they are related to the number of bits/gates. However, the number of bits/gates cannot be reduced without completely changing the function of the circuit. Therefore, this model cannot be used for built-in reliability.

The advantages of the model are twofold; first it takes into account all possible failure mechanisms, and secondly, it is easy to use because of its simplicity.

Another handbook with a model for the failure rate is the British Telecom Handbook of Reliability Data[2] (refer to Table II).

A third model to be mentioned here has been published by the French Centre National d'Etudes

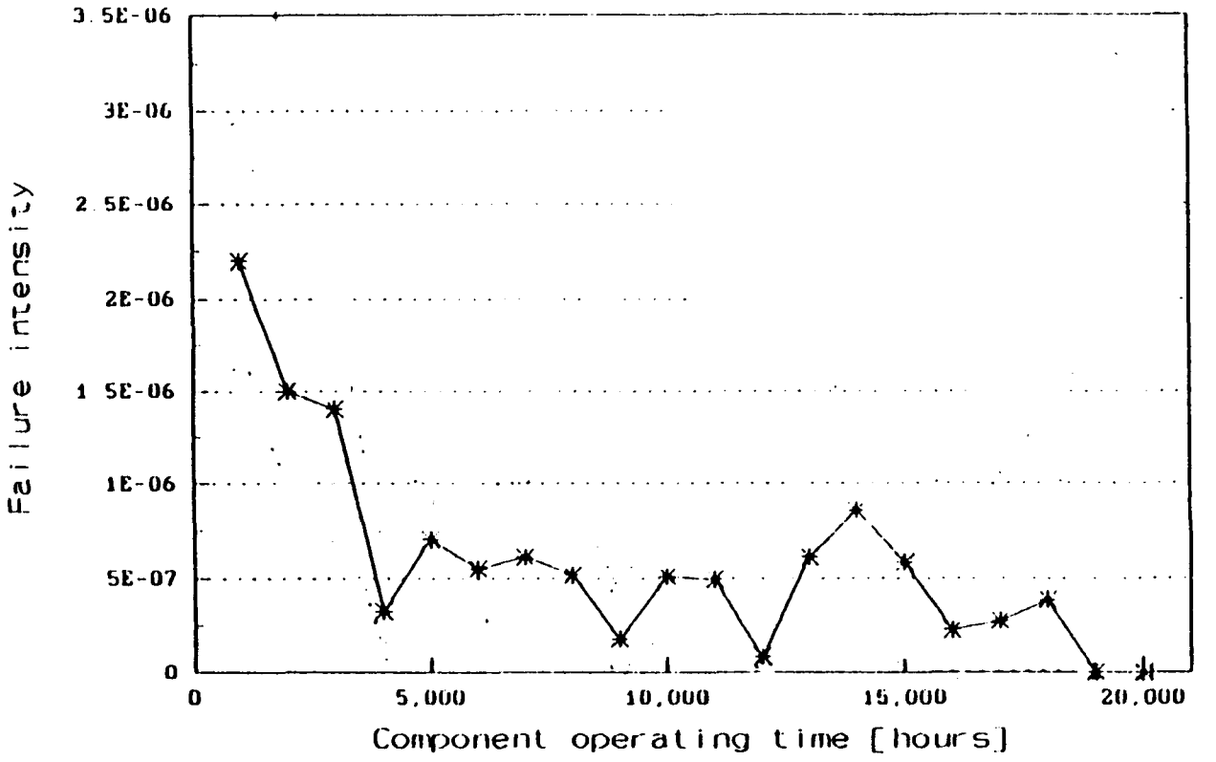

Figure 3. Failure intensity curve for digital MOS ICs with 10^3 to 10^4 gates

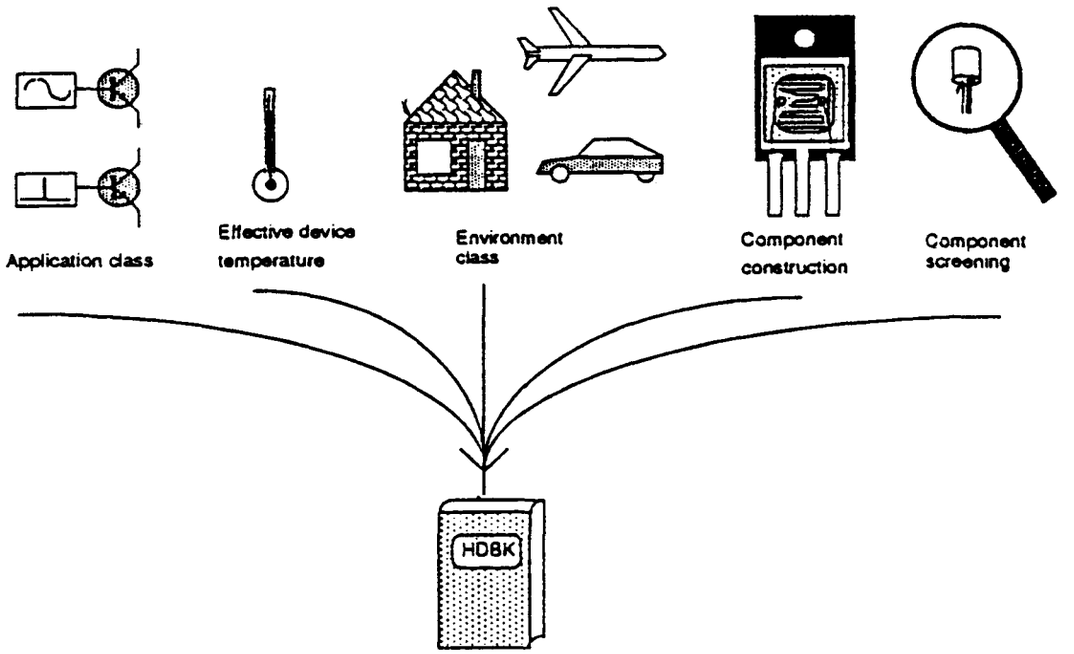

Figure 4. The use of reliability handbooks for several classes of systems

Table I. Failure rate model for integrated circuits according to the MIL-HDBK-217 handbook ($\lambda = \pi_q\pi_l[C_1\pi_t\pi_v\pi_{pt} + (C_1 + C_3)\,\pi_e]$)

Parameter	Description	Influence factors	Source
π_e	Environmental acceleration factor	environment class	heuristic
π_q	Quality acceleration factor	component screening	heuristic
π_t	Thermal acceleration factor	thermal, device structure	Arrhenius, heuristic
π_v	Voltage derating factor. MOS only	application class	heuristic
π_{pt}	Correction factor for programming technique. ROM/PROM only	device structure	heuristic
C_1, C_2	Complexity factor, depending on number of bits/gates	device structure	heuristic, (thermal conductivity package)
C_3	Complexity factor, depending on package	device structure	heuristic (thermal conductivity package)
π_l	Learning factor	device structure, depending on the maturity of the production process of a part	heuristic

des Telecommunications (CNET model, see Table III). The last two models have similar advantages and disadvantages to those mentioned with the Mil Handbook model.

3.3. *Results*

Before drawing conclusions about the models we will compare the reliability prediction figures with figures in practical situations. In Reference 2 failure rate data are given on two similar systems: self oscillating power supplies. The results of measurements (practice) and model calculation according to Mil Handbook (MIL) and British Telecom (HRD-4 (BT) are given in Figure 5. The horizontal axis indicates the different components in the system (D are diodes, R are resistance's, C are capacitors, etc.). It can be observed that the two models predict in general a higher failure rate than observed in practice. Moreover, there are vast differences in the

Table II. Failure rate model for integrated circuits according to the British Telecom Handbook of Reliability Data ($\lambda_p = \lambda_b \pi_t \pi_q \pi_e$)

Parameter	Description	Influence factors	Source
All parts			
π_e	Environmental acceleration factor	environment class	heuristic
π_q	Quality correction factor	component screening	heuristic
Integrated circuits			
λ_b	Base failure rate, depending on number of bits/gates	device structure	heuristic
π_t	Thermal acceleration factor: $Ae^{\frac{-3500}{T_j}} + e^{\frac{-11600}{T_j}}$	thermal, device structure	Arrhenius (two failure mechanisms), heuristic

Table III. Failure rate model for integrated circuits according to the CNET handbook ($\lambda_p = \pi_q[C_1\pi_T\pi_V + (C_2 + \pi_P)\pi_e]\pi_L$)

Parameter	Description	Influence factors	Source
π_q	Quality acceleration factor	component screening	heuristic
π_T	Technology factor	device structure	Arrhenius (two degradation mechanisms)
	$e\left[11606\,\varphi\left\{\frac{1}{T_{r1}} - \frac{1}{T}\right\}\right] + e\left[11606\,\varphi\left\{\frac{1}{T_{r2}} - \frac{1}{T}\right\}\right]$		
π_e	Environmental acceleration factor	environment class	heuristic
π_P	Package factor	device structure	heuristic (thermal conductivity package)
C_1, C_2	Complexity factors, depending on the number of bits/gates	device structure	heuristic

values. This is also valid not only for the absolute failure rate but also for the relative failure rate.[2]

3.4. *Conclusions*

Based on the data in the previous sections we conclude the following on the existing component failure rate models compiled in handbooks and intended for use in the systems approach. All possible failure mechanisms are taken into account:

1. The models are easy to use.
2. They assume a constant failure rate which is not the case.
3. The calculated failure rates show vast differences among the models.
4. No designable parameters are present for use in the concept of 'built-in' reliability.

Concerning the last conclusion we expect that new possibilities will occur for improvement by models based on stressor–susceptility interaction.[2]

4. CIRCUIT APPROACH

In this chapter on the circuit approach for component lifetime modelling we will focus our attention on integrated circuits. This is to some extent justified because the ICs form the dominant components in many electronic systems. Moreover, a separate approach is required because of the complexity of the circuits.

We want to consider separate degradation mechanisms. This means that we have to consider the different elements in the IC such as transistors, metal stripes, dielectric layers, etc., because each element may be vulnerable to particular degradation mechanisms. Moreover, in our approach we will look for models for the degradation mechanisms that contain designable parameters.

4.1. *Data collection*

As we have described in section 2 the data collection consists of field returns and reliability testing.

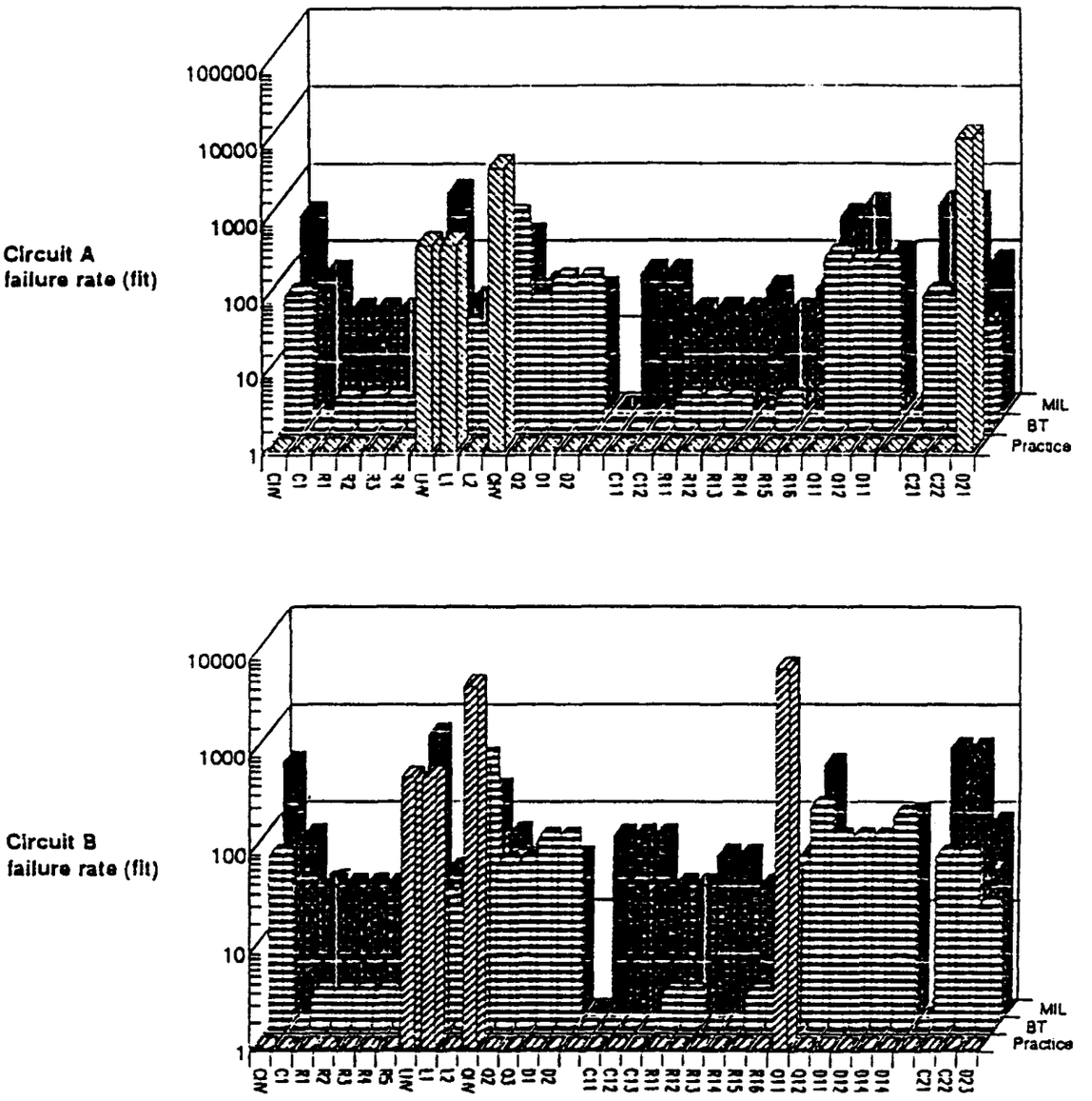

Figure 5. Measurements and model calculations according to the MIL and British Telecom handbooks

In this section we start with an overview of the main groups of reliability tests in integrated circuits. These are the following:

(a) Humidity tests. They are carried out at a high relative humidity, high temperature and usually with bias.
(b) Temperature cycling tests. Components are subjected to alternating temperatures, without bias.
(c) Electrostatic discharge (ESD). A fixed value capacitor is discharged through the component under test.
(d) Endurance testing. This testing is carried out at elevated temperatures and with bias applied to the circuits.

The outcome of these tests is usually a number of failures depending on the actual failure rate and on the number of components. In our first group of tests, namely the humidity tests, the lifetime of the component for all failure modes can be expressed[5] in terms of mean time to failure (MTTF):

$$\mathrm{MTTF} = A(\mathrm{RH})^{-n}\exp\left(E_a/kT\right) \qquad (4)$$

where the last factor is the well-known Arrhenius factor, RH the relative humidity and A a constant related to the composing materials. The quantity n has a value of about 3 according to Peck,[5] but it has no physical background. Moreover, equation (4) does not contain any designable parameter. Therefore, this group of tests is left out of further consideration.

In temperature cycling of plastic encapsulated ICs different failures may occur due to mechanical stresses originating from the difference in thermal expansion coefficients. The modelling of the acceleration factors for calculating lifetime is based on the mechanical properties of the constituting materials.[6, 7] It must be concluded that in recent

years considerable progress has been made in the physical understanding of the acceleration factors, but they do not yet contain on-chip designable parameters.

The opposite is true for the failures in ESD testing. The capacitor discharge can cause damage in the internal circuitry of the IC, but protection circuitry near the bond pads may reduce the sensitivity by deviating the discharge. The protections should have the right dimensions and structures, so many designable parameters are present. However, at the ESREF 91 conference an invited paper has already been given,[8] so this topic is not treated here in detail.

This leaves us with the last group of tests, namely, (electrical) endurance tests. Especially in this endurance testing one observes the bathtub curve for the failure rate (Figure 1) or more specifically the first two regions, as is shown in Figure 2. For the early-life regime we only have Arrhenius law, equation (2), as an acceleration factor. However, one observes a multitude of failures strongly related to contamination and defects. There are hardly any physical models and no designable parameters.[9]

For the wear-out regime a number of mechanisms are known:

(a) oxide breakdown
(b) hot carrier effects
(c) electromigration
(d) contact and via degradation, etc.

For all these degradation mechanisms physical models exist, although they are not complete or still subject to scientific debate.

In oxide breakdown the actual defect density is the important quantity for circuit reliability. The designable parameter related to it is the oxide area, i.e. this should be minimized. However, in any design this area is always minimized. This leaves the oxide breakdown modelling only for failure rate calculation and also for burn-in optimization.[1] For the other wear-out mechanisms, especially hot carrier effects and electromigration, the situation is different.[10] The models have designable parameters that are free to be changed by the designer. Then circuit simulation and design optimization become feasible. Therefore, their degradation models and parameters will be described in the next subsection. The data collection on wear-out mechanisms is also done by measurements on test structures.

4.2. *Models*

In the case of hot carrier effects in MOS circuits the parameter extraction is done in transistors as test structures. Because of the high fields in small transistors charge carriers are accelerated and are able to give damage, creation of interface states and charge trapping. As a consequence the electrical parameters of the transistor start to change, especially transconductance and threshold voltage. These parameter shifts are assumed to follow a time power-law.[11] The shifts have to be determined as a function of the stressors, in this case gate and drain voltage.

The damage by hot carriers is at a maximum when the bulk current I_b is at a maximum, which is for a gate voltage at about half of the drain voltage. For this reason the substrate/bulk current is used to extrapolate to lifetime τ at operating conditions;

$$\tau_{\text{life}} \sim (I_b/I_d)^{-m} \tag{5}$$

The parameter m is thought to be related to the ratio of the $Si-SiO_2$ barrier energy to the energy for impact ionization. It has a value of about 3.

Concerning the spatial dependence it has been found that the transistor lifetime is strongly dependent on the effective channel length. This can therefore be used to optimize the design: a small increase at particular vulnerable transistors may dramatically increase the reliability of the overall circuit with respect to hot carrier degradation.

The other mechanism we want to discuss here is the electromigration. The degradation model in general use is given in Black's formula:

$$\text{MTTF} \sim J^{-n} \exp(-E_a/kT) \tag{6}$$

Besides the Arrhenius factor we see a power-law dependence on current density. The value of n is usually taken as $n = 2$. This dependence on current density gives the possibility to optimize the design: a given current at a particular node in the circuit may result in a lower current density when the metal width at that particular node is increased.

4.3. *Results*

Figure 6 shows the frequency decreasing in a 125-stage CMOS ring oscillator due to hot carrier effects.[1] It can be clearly observed that this particular sensitive ring oscillator shows instabilities that can be nicely modelled and simulated. This means that this can be applied to other circuits and that in this way the hot-carrier-related lifetime can be calculated and subsequently optimized.

Figure 7 gives more results with respect to hot-carrier effects.[12] It shows the lifetime of 1·2 μm n-channel transistors stressed at maximum I_b (curves 1 and 2) and of two 8k8 SRAM batches (curves 3 and 4) as a function of $1/V_{dd}$. This way of plotting is well known in this field. It is based on physical modelling and can be used to extrapolate to use conditions. Between transistors and products a lifetime difference of a factor 50 has been observed.[12] This has been ascribed to the relatively small sensitivity of this product to transistor degradation and to duty cycle effects. It is interesting to note that these experiments were supported by circuit simulation.[12]

For electromigration, many results have been

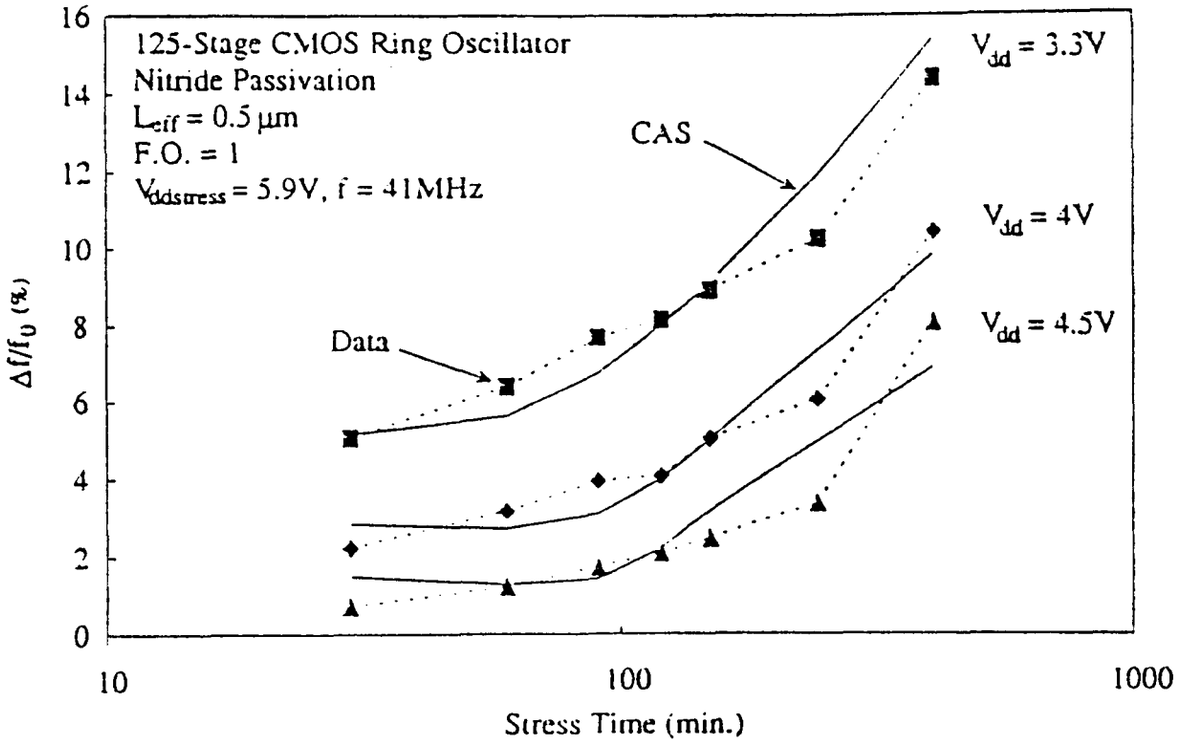

Figure 6. 125-stage CMOS ring oscillator. Measured and (BERT-CAS) simulated frequency decrease at three frequency measuring V_{dd} values[1]

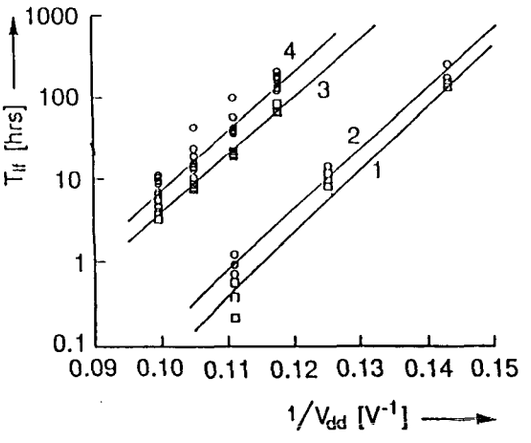

Figure 7. Comparison of hot-carrier lifetime in transistors (curve 1 and 2) and in SRAM products (curve 3 and 4)[12]

obtained on test structures. Also a lot of physical modelling has been carried out. But the application to circuits and circuit simulation is still limited. It is possible that this is related to the fact that the local stressor level (i.e. current density) is difficult to calculate directly from the circuit diagram. One needs the details of the actual lay-out. Hu[1] mentions the highlighting of electromigration trouble spots in a full-adder circuit. Frost and Poole[13] calculated the failure rate of a one-bit counter out of those of the different structure elements, runs (i.e. stripes) contacts, vias and steps. However, this is not yet corroborated by life testing on circuits.

4.4. *Conclusions on the circuit approach*

In the circuit approach the lifetime or the failure rate of the circuit is calculated with the aid of modelling the degradation by one mechanism for separate structure elements. There are no *a priori* assumptions necessary about the constancy of the failure rate, but this is directly calculated with the aid of the knowledge of the physical background of the degradation process. It should be noted, however, that for many degradation processes the physical models are not yet complete. This is even true for electromigration[14] that already has been studied for many years. A disadvantage of the approach is the extensive computer simulation necessary for a complete circuit. A great advantage is that the inherent models contain designable parameters for circuit optimization.

5. FINAL CONCLUSIONS

When we finally compare the two approaches described in the previous sections for the calculation of lifetime or failure rate of components than it can be concluded that

(a) the systems approach is easy to use and it takes into account all failure mechanisms.
(b) the circuit approach is based on physical mod-

elling and contains designable parameters for circuit optimization (built-in reliability).

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Authors' biographies:

Jan F. Verweij was born in Benschop, The Netherlands. He studied solid-state chemistry at the University of Utrecht. In 1967 he joined Philips Research Laboratories, Eindhoven, where he has been involved in research on hot carrier effects, oxide breakdown, high-voltage integrated circuits and non-volatile memory devices. From 1988 until 1991 he headed the Corporate Reliability Center for Integrated Circuits within Philips Components, Eindhoven. He also has some teaching experience. From 1976 until 1985 he was (extra ordinary) professor in Applied Physics at Groningen University, The Netherlands. Currently his teaching subject is reliability of semiconductor devices, and he has a small research group working on the modelling of electrothermal interactions, electrostatic discharge, hot carrier effects and electromigration.

Aarnout Cornelis Brombacher was born in Rotterdam, the Netherlands on 20 September 1961. He obtained a B.Sc., an M.Sc. and a Ph.D. in engineering science at Twente University of technology. Aarnout Brombacher has experience in industrial reliability analysis projects and the development of reliability analysis software, and has authored and co-authored several papers on these subjects. He is now working as head of the Quality Engineering department of Philips Consumer Electronics in Eindhoven. The main task of this department is research on, as well as application of, new methods and techniques for reliability engineering and reliability automation, especially for the early phases of the development process.

Besides his job at Philips, Aarnout Brombacher is also Professor in Mechanical Engineering at the Eindhoven University of Technology.

Meindert Martin Lunenborg was born in The Hague, the Netherlands on 5 May 1968. In 1992 he received the M.Sc. degree in electrical engineering from the University of Twente, Enschede, The Netherlands and he is currently working towards his Ph.D. degree at the same university. His research activities concentrate on MOSFET hot-carrier degradation phenomena and the development of MOS hot-carrier degradation models for circuit reliability simulation.