Gate Current and Oxide Reliability in p^+ Poly MOS Capacitors with Poly-Si and Poly-Ge_{0.3}Si_{0.7} Gate Material

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Abstract—Fowler–Nordheim (FN) tunnel current and oxide reliability of PMOS capacitors with a p^+ polycrystalline silicon (poly-Si) and polycrystalline germanium-silicon (poly-Ge_{0.3}Si_{0.7}) gate on 5.6-nm thick gate oxides have been compared. It is shown that the FN current depends on the gate material and the bias polarity. The tunneling barrier heights, ϕ_B , have been determined from FN-plots. The larger barrier height for negative bias, compared to positive bias, suggests that electron injection takes place from the valence band of the gate. This barrier height for the GeSi gate is 0.4 eV lower than for the Si gate due to the higher valence band edge position. Charge-to-breakdown (Q_{bd}) measurements show improved oxide reliability of the GeSi gate on of PMOS capacitors with 5.6 nm thick gate oxide. We confirm that workfunction engineering in deepsubmicron MOS technologies using poly-GeSi gates is possible without limiting effects of the gate currents and oxide reliability.

Index Terms—Deep-submicron MOS technology, GeSi, Fowler–Nordheim, oxide reliability, valence band tunneling.

I. INTRODUCTION

THE reduction of gate oxide thickness with downscaling CMOS technologies leads to increasing oxide fields. Thus Fowler–Nordheim (FN) induced oxide degradation is an important issue. In deep-submicron CMOS technology p^+ polysilicon gates are usually used for PMOS devices. BF_2^+ doped poly-GeSi gates have been investigated recently because of the possibility to manipulate the workfunction by changing the Ge mole fraction [1], [2] and the compatibility to Si processing. However, little is known about the effects of this novel gate material on the FN tunnel currents and oxide reliability using thin gate oxides.

In this paper we compare BF_2^+ doped poly-GeSi and poly-Si gate material grown on 5.6 nm thick gate oxide. FN currents

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Fig. 1. Current–voltage characteristics for MOS capacitors with a $2 \times 10^{15} \text{ cm}^{-2} BF_2^+$ doped poly-Si and poly-Ge_{0.3}Si_{0.7} gate after an anneal of 30 m at 850 °C.

of p^+ gated MOS capacitors with both positive and negative injection voltages and Q_{bd} results were studied. We show that because of the smaller bandgap of GeSi the onset of conduction takes place at lower absolute values for the gate voltages. For negative gate voltages, the tunneling mechanism is not completely understood and might be the result of valence band tunneling [3]. There are no electrons in the conduction band and substrate hole tunneling is improbable. The tunnel barrier height for gate injection will then be larger than for substrate injection where electrons tunnel from the conduction band. The effect of the Ge presence at the gate/SiO₂ interface has been studied by means of statistical Q_{bd} measurements.

II. EXPERIMENTAL

MOS capacitors were fabricated on n-type Si(100) substrates with a resistivity of $\rho = 10 \Omega\text{-cm}$. Undoped poly-Si or -Ge_{0.3}Si_{0.7} was deposited in an LPCVD system on gate oxide with a thickness of 5.6 nm as determined with ellipsometry. The gate oxide recipe was based on a standard thermal oxide from a 0.25 μm CMOS process [4]. The 200-nm thick gate was implanted with $2.5 \times 10^{15} \text{ cm}^{-2} BF_2^+$ at 20 keV and activated for 30 m at 850 °C in N₂ ambient. For Si and GeSi gates, the gate depletion was acceptable (9 and 8.5%, respectively, determined from C – V measurements at ± 2 V) and negligible

Fig. 2. Schematic overview of oxide breakdown due to valence band tunneling from p^+ poly gates.

Fig. 3. Fowler-Nordheim plot of MOS capacitors with a poly-Si and poly-GeSi at positive and negative gate biases.

fluorine enhanced boron diffusion through the SiO_2 layer was observed.

III. RESULTS AND DISCUSSION

The FN current of p^+ poly MOS capacitors with 5.6 nm gate oxide thickness for Si and GeSi gates is shown in Fig. 1 under positive and negative gate voltages, with illuminated samples. At positive bias, the GeSi gated samples show the onset of conduction 0.15 V earlier than the Si samples because of the difference in flatband voltage, V_{fb} . At negative gate bias the onset of conduction is 0.35 V earlier for poly-GeSi gates. This shift cannot be accounted for by a slightly larger poly-Si gate depletion, but is due to the difference in valence band edge position since injection takes place from the valence band instead of the conduction band as will be shown below [3]. Although the onset of conduction is earlier for poly-GeSi gate material, the used 5.6 nm thick gate oxide provides good isolating properties for (sub) 0.25 μm CMOS technology. In Fig. 2 a schematic picture of the tunneling mechanism is shown indicating that the barrier heights for gate injection will be smaller for a poly-GeSi gate because of the smaller valence band energy. The energy barrier heights, ϕ_B , were determined from FN-characteristics plotting J/E^2 versus $1/E$. To calculate the exact oxide field the flatband voltage and mono-Si voltage

Fig. 4. Weibull distributions of capacitors with a poly-Si or poly- $\text{Ge}_{0.3}\text{Si}_{0.7}$ gate. A constant current density of $J = 5 \text{ mA/cm}^2$ was applied to 50 capacitors with an area of $6.4 \times 10^3 \text{ cm}^2$.

drop were taken into account. The depletion approximation [5] has been used to correct for poly depletion. In Fig. 3 the FN characteristics are shown for both gate materials at positive and negative gate voltages. It is obvious that the curves at negative gate biases are significantly steeper than for positive gate voltages. The energy barrier heights for positive voltages are $\phi_B = 3.1 \text{ eV}$ for poly-Si and poly- $\text{Ge}_{0.3}\text{Si}_{0.7}$ gate material. With this method the barrier height can be determined up to a 0.1 eV accuracy. For negative gate voltages the barrier heights for the two materials are different, $\phi_B = 4.0 \text{ eV}$ for GeSi and $\phi_B = 4.4 \text{ eV}$ for the Si gate. The larger barrier heights for poly-Si gates at negative bias compared to poly- $\text{Ge}_{0.3}\text{Si}_{0.7}$ gates is also observed for gate oxide thickness' in the range of 6.8–10.4 nm. In comparison, NMOS capacitors with As^+ doped gates on 5.6 nm thick gate oxide resulted for both Si and GeSi gates in a measured barrier height of $\phi_B = 3.0 \text{ eV}$ for substrate and gate injection, as was expected since the conduction band edge positions of Si and GeSi are almost equal. These results strongly suggest that the assumed carrier valence band tunneling model for negative biased p^+ type gates is correct.

To investigate the gate oxide reliability, charge-to-breakdown measurements were performed on capacitors annealed for 30 m at 850 $^\circ\text{C}$. In Fig. 4 the Weibull distributions are shown for 50 capacitors under negative gate bias, i.e., electron injection from the gate. A constant current stress with a current density of $J = 5 \text{ mA/cm}^2$ was used. The area of each of the capacitors was $6.4 \times 10^{-3} \text{ cm}^2$. An average Q_{bd} value of 1 C/cm^2 is acceptable considering the relatively large size of the capacitors. The distribution for the GeSi gates shows a slightly higher Q_{bd} which can be attributed to reduced boron incorporation in the 5.6 nm thick gate oxide, caused by the reduced diffusivity of boron in polycrystalline GeSi [6]. For samples annealed at a lower thermal budget we found the Q_{bd} to increase by a factor of approximately three [7]. For these samples the slope of the Weibull distribution of both gate materials is the same. This indicated that the difference between Si and GeSi gates is caused by a difference in boron penetration. It also appears that Ge present at the gate/gateoxide interface does not degrade the oxide quality. For positive gate bias the

average values for Si and GeSi are $Q_{bd}^+ \sim 20 \text{ C/cm}^2$. For substrate injection the Q_{bd} for GeSi gates is again slightly better than for Si gates.

IV. CONCLUSIONS

Tunnel currents and oxide reliability of p^+ doped poly-GeSi gate material have been studied and compared with poly-Si gates. It was found that PMOS capacitors with BF_2^+ doped (Si or GeSi) gates on 5.6 nm thick gate oxide show a larger oxide barrier height for gate injection than for substrate injection. The increase of the oxide barrier is caused by electron tunneling from the valence band and is approximately equal to the bandgap of the gate material. For Si gate material ϕ_B increases from 3.1 eV at positive gate voltages to 4.4 eV at negative voltages. For GeSi gates the increase is smaller, from $\phi_B = 3.1$ to 4.0 eV, because of the smaller valence band edge energy level of GeSi gate material. This means that for BF_2^+ doped poly-Si or polyGeSi gates the onset of conduction is always as good as or better than for n^+ doped gates. Although GeSi gated samples start conducting earlier, they still have good isolating properties for deep submicron CMOS applications. Charge-to-breakdown measurements indicate that the gate oxide breakdown behavior is similar or even better for GeSi than for Si gates. The Ge at SiO_2 interface does not degrade the oxide quality. The effects of boron and fluorine are the same for poly-Si and poly-GeSi gates. Hence the difference in workfunction can be exploited without problems

with the gate oxide reliability or increase on the tunneling currents.

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REFERENCES

- [1] T.-J. King, J. R. Pfister, J. D. Shott, J. P. McVittie, and K. C. Saraswat, "A polycrystalline- $\text{Si}_{1-x}\text{Ge}_x$ -gate CMOS technology," in *IEDM Tech. Dig.*, 1990, pp. 253–256.
- [2] C. Salm, D. T. van Veen, J. Holleman, and P. H. Woerlee, "Electrical characteristics of B^+ and BF_2^+ implanted poly-Si and poly- $\text{Ge}_x\text{Si}_{1-x}$ as gate material for sub $0.25 \mu\text{m}$ applications," in *Proc. ESSDERC'95*, pp. 131–134.
- [3] J.-L. Ogier, R. Degrave, G. Groeseneken, and H. Maes, "On the polarity dependence of oxide breakdown in MOS-devices with n^+ and p^+ polysilicon gate," in *Proc. ESSDERC'96*, pp. 763–766.
- [4] G. M. Paulzen, E. K. H. Hutten, and V. M. H. Meysen, "Low thermal budget 6 nm furnace N_2O -nitrided gate oxides," in *Proc. ESSDERC'95*, pp. 239–242.
- [5] K. F. Schuegraf, C. C. King, and C. Hu, "Impact of polysilicon depletion in thin oxide MOS technology," in *Symp. VLSI Technol., Syst., Applicat.*, 1993, pp. 86–90.
- [6] C. Salm, D. T. van Veen, D. J. Gravesteijn, J. Holleman, and P. H. Woerlee, "Diffusion and electrical properties of boron and arsenic doped poly-Si and poly- $\text{Ge}_x\text{Si}_{1-x}$ ($x \sim 0.3$) as gate material for sub- $0.25 \mu\text{m}$ complementary metal oxide semiconductor applications," *J. Electrochem. Soc.*, vol. 144, no. 10, pp. 3665–3673, 1997.
- [7] Y. V. Ponomarev, C. Salm, J. Schmitz, P. H. Woerlee, and D. J. Gravesteijn, "High-performance deep submicron MOST's with polycrystalline-(Si,Ge) gates," in *Symp. VLSI Technol., Syst., Applicat.*, 1997, pp. 311–315.