Low-Temperature Fabricated TFTs on Polysilicon Stripes

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***Abstract*—This paper presents a novel approach to make high-performance CMOS at low temperatures. Fully functional devices are manufactured using back-end compatible substrate temperatures after the deposition of the amorphous-silicon starting material. The amorphous silicon is pretextured to control the location of grain boundaries. Green-laser annealing is employed for crystallization and dopant activation. A high activation level of As and B impurities is obtained. The main grain boundaries are found at predictable positions, allowing transistor definition away from these boundaries. The realized thin-film transistors (TFTs) exhibit high field-effect carrier mobilities of 405 $cm^2/V \cdot s$ (NMOS) and 128 $cm^2/V \cdot s$ (PMOS). CMOS inverters and fully functional 51-stage ring oscillators were fabricated in this process and characterized. The process can be employed for large-area TFT electronics as well as a functional stack layer in 3-D integration.**

***Index Terms*—Above integrated circuit (IC), grain boundary, laser annealing, polycrystalline silicon, thin-film transistor (TFT), 3-D integration.**

I. Introduction

As INTEGRATED-CIRCUIT (IC) downsizing may soon reach physical and commercial limitations, 3-D integration is gaining attention. One pursued route for 3-D ICs is the stacking of several active layers by subsequent thin-film depositions. This approach demands low thermal budgets [1]–[3] in combination with good-quality semiconductor and dielectric films. Thin-film transistor (TFT) technology offers just that, in particular through laser crystallization of low-temperature deposited amorphous silicon [4]–[9]. One issue with such films is the random position of grain boundaries, resulting in randomly distributed electrical potential barriers, leading to large device-to-device variations.

Recently, several techniques were reported to control the position of grain boundaries in excimer-laser-crystallized silicon films, through air-gap formation [10], two-pass laser crystallization [11], and the introduction of silicon spacers [12] or buried crystallization seeds [13]. Bearing manufacturing cost and yield considerations in mind, it is at this time unclear which is the most effective solution for controlled grain formation.

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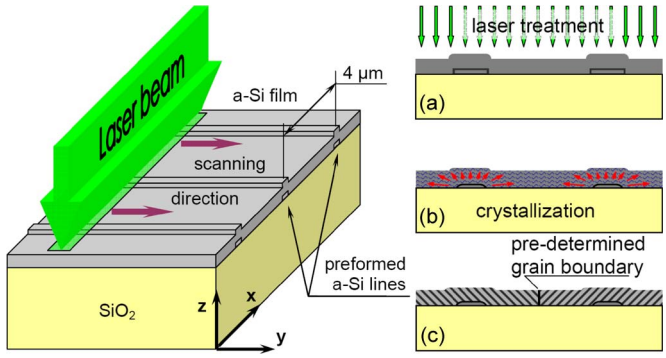

Fig. 1. Crystallization process of a silicon film with preformed lines. (Left) Illustration of the crystallization step. (a) Laser treatment, melting the silicon film, (b) crystallization process—super lateral growth, and (c) crystallized film with predefined grain boundaries.

Following up on the approaches using spacers and seeds, we recently proposed a new approach to control the location of grain boundaries [14], [15], as shown in Fig. 1. An amorphous silicon layer (with typical thickness of 50–100 nm as common in poly-Si TFTs [16]) is deposited over parallel amorphous silicon lines, oriented in the laser-crystallization direction. During laser annealing, a lateral temperature gradient in the molten silicon will result. Recrystallization will start from the coolest (thickest) positions and end in between two lines where the major crystal boundary will form. Thus, long crystals aligned in one direction will be formed.

An important issue is the laser wavelength applied for crystallization. The interlayer oxide must be transparent at this wavelength to prevent its heating to avoid cracks, deformation, and other damage [17]. At the same time, the absorption coefficient for amorphous Si film must be high enough to provide complete melting of the irradiated film.

In the case of the excimer-laser crystallization (308-nm wavelength), the laser beam penetration depth into amorphous silicon and polysilicon extracted from spectroscopic ellipsometer (SE) measurements [18] is < 10 nm, so primarily, a thin top layer of the silicon film is melted and only further heat diffusion provides complete melting of the film. For this reason, we chose for an irradiation at 515-nm wavelength, which has much lower measured absorption coefficients. That ensures a larger penetration depth of $\approx$49 nm for a-Si and near 200 nm for crystallized poly-Si film [18], leading to a more homogeneous melting of silicon layer [17]. This widens the process window for recrystallization in terms of the laser power and pulse duration.

In this paper, the properties of green-laser-crystallized silicon films with preformed a-Si lines are presented and discussed,

such as the obtained crystal structure and sheet resistance. The films are further used to realize n- and p-channel TFTs. The current–voltage characteristics of the transistors, performance of CMOS inverters, and efficiency of TFT channel location control in ring oscillators are shown.

II. Results and Discussion

A. Laser Treatment of a-Si Films

On 100-mm 5–10-$\Omega \cdot$ cm Si wafers thermally oxidized to grow a 0.9-μm SiO_2 layer, a 50-nm-thick a-Si film was deposited by LPCVD (from SiH_4) at 550 °C, in which lines of $\sim$0.5 μm wide at a 4-μm distance were patterned. A second 100-nm a-Si layer was deposited with the same LPCVD process, resulting in an amorphous film with a periodically varied thickness (Fig. 1).

The film was then crystallized using the laser optical system LAVA at INNOVAVENT GmbH, utilizing a green (515-nm) laser beam up to 54-mm length. The laser beam has a uniform top-hat profile along the x-direction and a Gaussian profile along the (scanning) y-direction. The beam intensity profile was measured at the wafer plane using a CCD camera and a microscope. The applied beam length was 8 mm, and the width was 5.8 μm, both full-width half-maximum (FWHM) values. The average energy density in the beam was adjusted by an optical attenuator. The energy density was defined as the total pulse energy divided by the FWHM area of the beam [14].

For the film irradiation, we used the second harmonic of a diode-pumped Yb:YAG thin disk laser (model JenLas ASAMA) irradiating at a repetition rate of 50 kHz. The pulse duration was 206 ns. The scan velocity was 5.68 mm/s, providing a beam overlap of 98%. Silicon film crystallization was investigated at laser energy densities ranging from 0.6 to 1.2 J/cm^2.

During the laser crystallization, the periodically varied thickness locally results in nonmolten lines deeply embedded into the molten silicon. These solid regions influence the temperature gradient in the lateral direction that is perpendicular to the laser scan direction and serve as the crystallization centers for super lateral crystal growth [see Fig. 1(c) and (d)]. The thicker film regions crystallize first, followed by crystallization of the remaining thinner regions. Thereby, the dominant crystal orientation can laterally extend to the grain boundaries, with a possible formation of intragranular ridges and hillocks. AFM measurements show that ridges and hillocks are not significantly apparent in our process [14].

An important parameter for the crystallization process was the choice of line width and line pitch. At 4-μm pitch and 0.5-μm line width, we obtain the largest width grains. If we increase the line pitch above 4 μm, the grains do not extend wide enough perpendicularly to the laser scan direction. If the line width is larger than 0.5 μm, the topography after crystallization is considerable—only thin lines are partly planarized during the crystallization step. A thicker buried silicon line also leads to undesirable topography. The reduction of the line thickness below 50 nm leads to process window narrowing.

To gain continuous super lateral crystal growth starting from the crystallization centers on the bottom of the molten silicon,

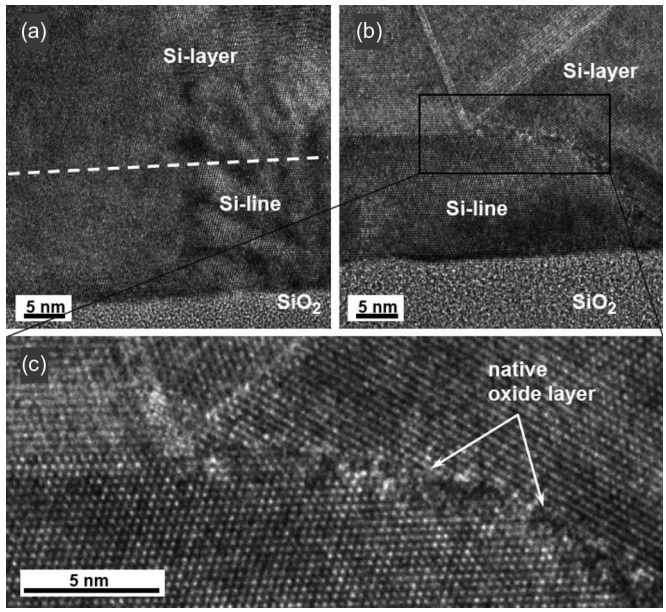

Fig. 2. TEM images of crystallized silicon films: (a) Super lateral crystal growth and (b) fine grain formation on the Si-line and the Si-layer interface [native oxide layer between Si-line and Si-layer is enlarged in (c)]. The dashed line indicates the location of interface between the Si-line and Si-layer.

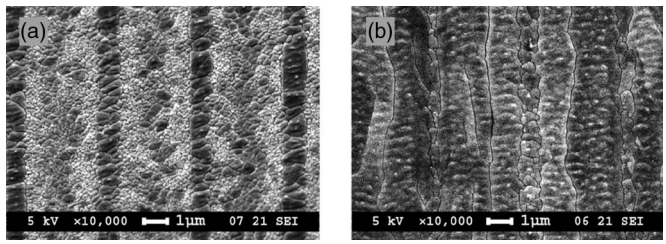

Fig. 3. SEM images (after Wright etch) of a-Si films crystallized with energy densities of (a) 0.6 J/cm^2 and (b) 1.0 J/cm^2 at 98% laser beam overlap.

it is important to have no oxide layer formed between the lines and the upper (second) layer of silicon. This can be achieved by immediate a-Si deposition on a hydrogen-terminated Si surface formed after the last HF dip during stripe patterning. Fig. 2(a) shows the cross section of the crystallized silicon film with the grain propagated from the silicon line into the film lying above. Interruption of the super lateral crystal growth is shown in Fig. 2(b) and (c). Here, the presence of an interfacial layer (i.e., native oxide) on the silicon lines separates the crystallization of the bottom and top layers, resulting in the formation of smaller polysilicon grains.

The crystallinity of the silicon films is visualized by Wright etching as shown in Fig. 3(a) and (b). At sufficiently high laser energy, the material forms long crystalline stripes. This is confirmed by the electron backscatter diffraction (EBSD) analysis (see Fig. 4). The main grain boundaries [marked with black in Fig. 4(a)] in the films crystallized with 1.0 J/cm^2 are oriented mostly parallel to the preformed a-Si lines, i.e., in the laser scanning direction, providing a good control over their location (see Figs. 3(b) and 4). The grain boundaries oriented perpendicular to the laser scanning direction [marked with yellow in Fig. 4(a)] mainly are electrically less active subgrain twin boundaries formed during the lateral growth to release

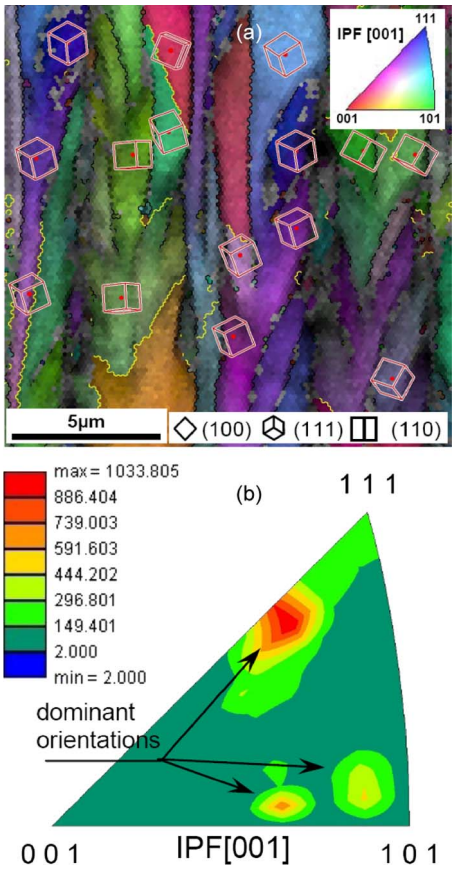

Fig. 4. (a) Crystal orientation map and normal direction inverse pole figure extracted from (b) the orientation map of crystallized silicon films (1.0 J/cm^2 at 98% laser beam overlap; the inset shows the color key indicating the orientation aligned with the surface normal).

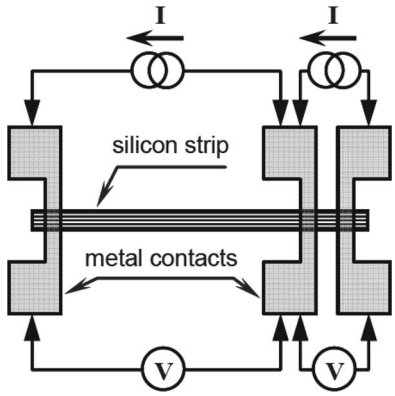

Fig. 5. Measuring configuration for determining $R_{\square}$. The length ratio between the left and right parts of the silicon strips on the same structure was 250 μm/10 μm or 200 μm/20 μm, and the widths were 5, 10, and 15 μm.

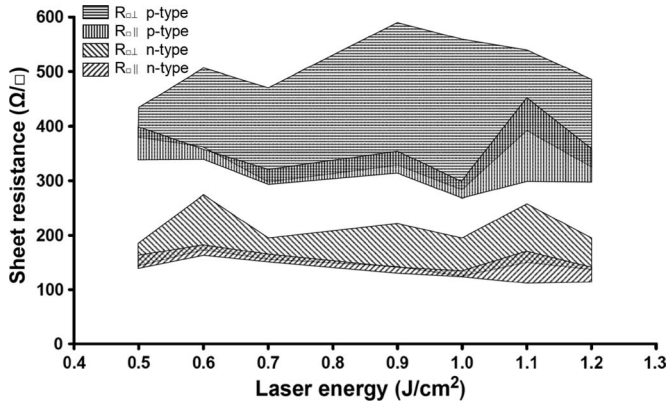

Fig. 6. Sheet resistance spread of crystallized a-Si films versus laser crystallization energy.

thermal stress in a crystallized film [19], [20]. The concept of enlarged crystalline grain formation is therefore approved.

The irradiation with a lower energy (0.6 J/cm^2 at 98% overlap) resulted in insufficient film melting. This leads to a fine-grain structured silicon film [see Fig. 3(a)].

Fig. 4(b) shows the relative prevalence of certain grain orientations with respect to the film surface normal direction, observed by EBSD. The dominant orientation is (112), with fractions of (102) and (142) oriented grains.

It should be noted that the exact process window for laser crystallization may vary upon the layer stack underneath the a-Si film, because the thermal diffusion is different [21]. A silicon heat sink layer can alleviate this problem [22]. The silicon layer thickness is more than the absorption length for the used wavelength, in particular at higher temperatures. Therefore, we expect that interference inside the silicon film can be neglected.

B. Sheet Resistance $R_{\square}$ Measurements

1) Fabrication of Long Diffusion Area Structures: Test structures were designed to verify the impurity activation. Due to the expected anisotropy in electrical behavior, the conventional four-point method for measuring sheet resistance (e.g., van der Pauw or Greek cross) [23] could not be employed. Thus, sheet resistance was measured in both directions using Kelvin-contacted silicon stripes of 300-μm length and 5-, 10-, and 15-μm width (Fig. 5), oriented in the x- and y-directions.

The crystallized silicon films were initially patterned to form stripes. Then, BF_2^+ (1×10^{15} cm^{-2}) and As^+ (4×10^{15} cm^{-2}) ions were implanted at 55 keV to form p- and n-type stripes. Arsenic was chosen instead of phosphorus due to the lower diffusion and smaller implantation depth at the same acceleration voltage. The higher solubility of arsenic allows an implantation of higher dose in comparison with boron.

The dopant activation was done by a laser optical system that is similar to that used for the crystallization. The applied laser energy density was 0.4 J/cm^2. The beam length was 5.16 mm, and the width was 28.4 μm. The pulse duration was 300 ns with a repetition rate of 10.2 kHz, and the scan velocity was 14.5 mm/s, providing a beam overlap of 95%. Under these conditions, the dopant becomes active without silicon remelting.

2) Sheet Resistance $R_{\square}$ of Laser-Crystallized Films: We measured the sheet resistance of the silicon stripes, oriented in both the *parallel* (y-axis) and *perpendicular* (x-axis) current-flow directions with respect to the main grain boundaries. These resistivities, labeled $R_{\square\parallel}$ and $R_{\square\perp}$, respectively, are shown in Fig. 6. Clearly (and as expected), the sheet resistance is lower when current flows parallel to the main grain boundaries. Moreover, the spread of $R_{\square\parallel}$ is significantly lower in comparison to the $R_{\square\perp}$ spread, for both p- and n-type films. In samples

TFT process steps	technique	temperature
a-Si deposition	LPCVD	550 °C
lines patterning	wet etching	R.T.
a-Si deposition	LPCVD	550 °C
Si crystallization	laser crystallization	
Si-film patterning	wet etching	R.T.
S/D doping	ion implantation	R.T.
dopant activation	laser annealing	
SiO_2 gate deposition	ICPECVD	150 °C
contact openings	wet etching	R.T.
metallization	Al sputtering	R.T.
Al patterning	wet etching	R.T.
post metall. anneal	in H_2O/N_2 for 10 min.	400 °C

Fig. 7. Process steps used for the TFT fabrication.

crystallized at 0.7–1.0-J/cm^2 laser energy densities, the parallel sheet resistance of both films has an rms spread below 5% in contrast to the perpendicular rms spread of up to 21%. The figure further indicates that the laser energy dependence is weak, suggesting an appreciable process window.

From the calculated resistivity values ($\rho_{n,\|} = 1.4$ m$\Omega \cdot$ cm for n-type and $\rho_{p,\|} = 3.0$ m$\Omega \cdot$ cm for p-type silicon film), we can derive the concentrations of the electrically activated donor and acceptor atoms, i.e., approximately 8×10^{19} cm^{-3} for boron and 3×10^{20} cm^{-3} for arsenic, near the saturation limit of heavily doped films [24]. This corresponds to an activation level above 80% for both impurities.

C. TFTs

1) TFT Fabrication: Similarly to the long diffusion area test structures, TFTs were fabricated on patterned silicon films primarily crystallized with laser energy densities of 1.0 J/cm^2. The same implantation conditions were used to form p- and n-type regions for the source and drain. Then, the same dopant activation process was applied.

A 100-nm-thick SiO_2 gate dielectric layer was deposited by means of remote inductively coupled plasma-enhanced chemical vapor deposition (ICPECVD) in Ar–N_2O–SiH_4 plasma at 150 °C and pressure of 1 Pa. The gas phase contained 0.08% of SiH_4 and 18% of N_2O—see [25] and [26] for more details. The thickness of the deposited oxides was determined by J. A. Woollam M2000 SE and was confirmed by C–V measurements.

Then, contact openings in the SiO_2 were etched in a buffered hydrofluoric acid solution. The front and back sides were metalized by sputtering a 1-μm-thick Al layer, patterned at the front side (defined by photolithography and wet etched)—providing metal contacts to the source/drain regions and forming the gate electrode. The post metallization anneal was done in H_2O/N_2 ambient for 10 min at 400 °C. The TFT fabrication process is summarized in Fig. 7

Electrical measurements were performed on a Karl Suss MicroTec PM300 Manual Probe Station equipped with a Keithley 4200 SCS.

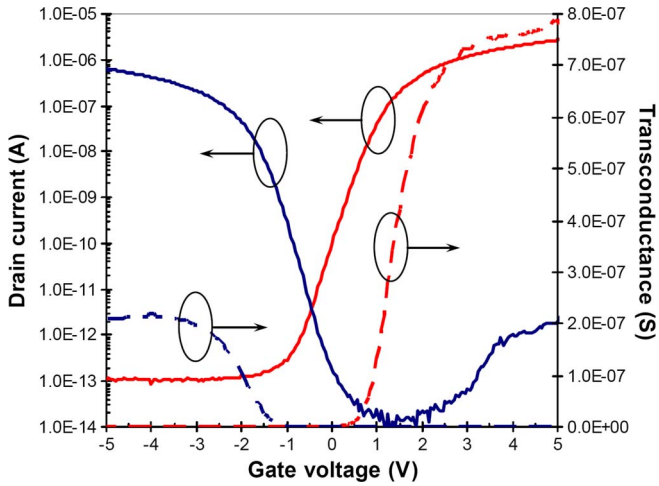

Fig. 8. Transfer characteristics measured for *parallel* n-channel and p-channel TFTs ($W/L = 10\ \mu$m$/20\ \mu$m) at a drain voltage of 0.1 V or -0.1 V. Laser crystallization energy was 1.0 J/cm^2.

TABLE I
TFT PERFORMANCE

Symbol	N-MOS		P-MOS	
	$\|\|$-TFT	$\perp$-TFT	$\|\|$-TFT	$\perp$-TFT
TFT channel sizes (W/L)	10/20	10/20	10/20	10/20
Threshold voltage, V_{th} (V)	1.5	3.6	-2.0	-4.1
On-current, I_{on} (μA)	35.1	6.1	7.6	1.5
Subthreshold slope, S (mV/dec)	308	359	275	383
Field effect mobility, μ_{FE} (cm^2/Vs)	405	145	128	89

2) Electrical Characterization: The field-effect mobility was calculated from transconductance g_m in the linear region at low source–drain voltage (V_{DS}) using the following equation [23]:

$$\mu_{FE} = \frac{L g_m}{W C_{ox} V_{DS}} \tag{1}$$

where C_{ox} is the gate oxide capacitance per unit area, L and W are the channel length and width, respectively, and

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=0.1\,V}. \tag{2}$$

Here, I_D is the drain current and V_{GS} is the gate voltage.

The measurements were done using the Al front gate, with the Si bottom gate (i.e., the substrate) grounded. The device channels were undoped for both p- and n-channel TFTs.

Fig. 8 shows typical transfer characteristics obtained at a drain voltage of -0.1 V for p-channel TFTs and 0.1 V fo r n-channel TFTs. For all the measured TFTs, the channels were realized in both *perpendicular* and *parallel* orientations to the laser scanning direction (or to the main grain boundaries), and the channel sizes (W/L) were 10 μm$/20$ μm.

A correct orientation of transistors with respect to the grain boundaries is essential. The *parallel* TFTs show superior mobility for both N- and PMOS transistors, as listed in Table I. The TFTs with channels oriented *parallel* to the main grain boundaries additionally exhibit a lower subthreshold slope

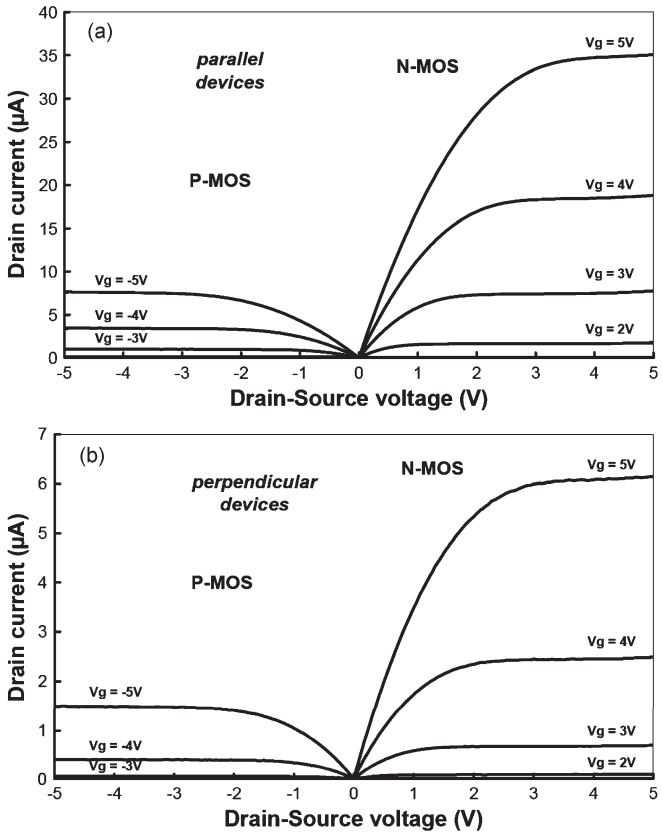

Fig. 9. Output characteristics measured for (a) *parallel* and (b) *perpendicular* n-channel and p-channel TFTs ($W/L = 10\ \mu\text{m}/20\ \mu\text{m}$) at different gate voltages. Laser crystallization energy was 1.0 J/cm^2.

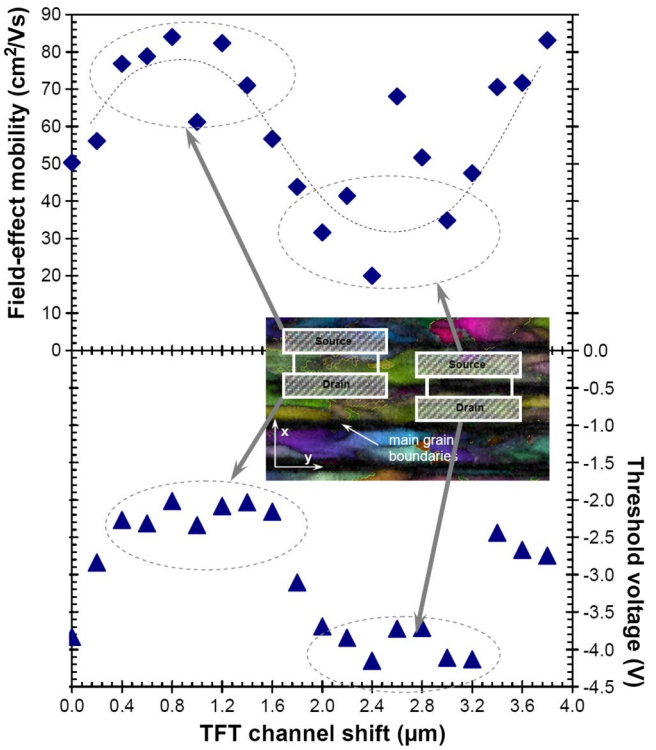

Fig. 10. Location-dependent (a) field-effect mobility of holes ($\mu_{\text{FE},h}$) and (b) threshold voltage measured for *perpendicular* p-channel TFTs ($W/L = 12\ \mu\text{m}/2\ \mu\text{m}$; laser crystallization energy is 1.0 J/cm^2). Between neighboring devices, the TFT channel is shifted with a step $\Delta x = 0.2\ \mu$m in the x-axis direction (see Fig. 1). Dashed lines are drawn to guide the eye.

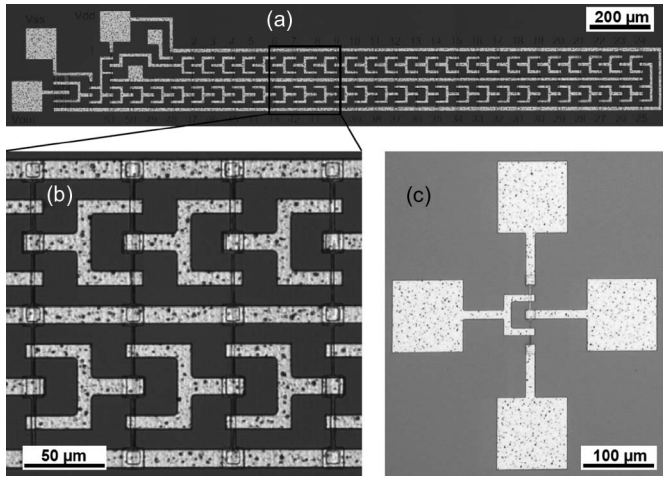

Fig. 11. Optical image of (a) 51-stage ring oscillator [eight stages are zoomed-in in (b)] and (c) CMOS TFT inverter.

(Table I) and little location dependence. Furthermore, the mobility of the present TFTs using ICPECVD SiO_2 is significantly higher than the earlier fabricated TFTs with ALD Al_2O_3 [15]. We attribute this mobility enhancement to the use of a thick high-quality SiO_2 gate dielectric [26] in contrast to the earlier used thin Al_2O_3 [15]. Al_2O_3 has also shown to yield lower mobilities in the case of MOS transistors on monocrystalline Si [27].

The output characteristics (Fig. 9) exhibit typical linear-saturation curves for the drain current at various gate voltages. Thus, as it follows from the transfer and output characteristics, the orthogonal devices show a lower mobility, strongly dependent on the placement of the device with respect to the grain boundaries: An improper placement leads to lower on-currents.

As schematically shown in Fig. 1, laser crystallization with underlying preformed a-Si lines enables the formation of laterally enlarged grains with grain boundaries dominantly located in between the line positions. A series of 20 TFTs with predetermined channel locations (oriented *perpendicular* to the laser scanning direction and to the grain boundaries) was manufactured. The channel sizes (W/L) were 12 μm/2 μm. The channel of each next transistor was shifted in the x-direction for 0.2 μm with respect to the position of the previous transistor in the same series. This gradual channel shift ensures the existence of TFTs with major grain boundaries located in the channel, and devices with much less boundaries or even grain-boundary-free channels. The measured mobility and threshold voltage values (Fig. 10) show a performance enhancement of the TFTs having channels placed in between the major grain boundaries.

D. CMOS Inverters and Ring Oscillators

To perform a dynamic characterization of the TFTs, we designed and fabricated CMOS inverters and 51-stage ring oscillators, as shown in Fig. 11. For a basic CMOS inverter, the channel widths for p- and n-channel TFTs were 3 and 2 μm, respectively, and the channel lengths were 2 μm for both transistor types. To avoid loading down the ring oscillator, an

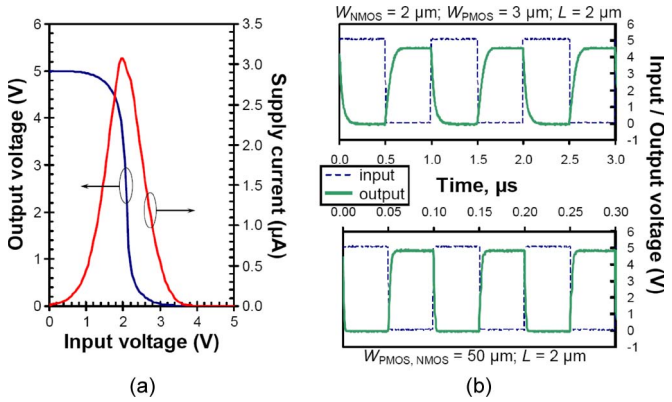

Fig. 12. Transfer characteristics of CMOS TFT inverters: (a) Static and (b) dynamic at $V_{\rm DD} = 5$ V (the TFT channels are oriented *parallel* to the grain boundaries).

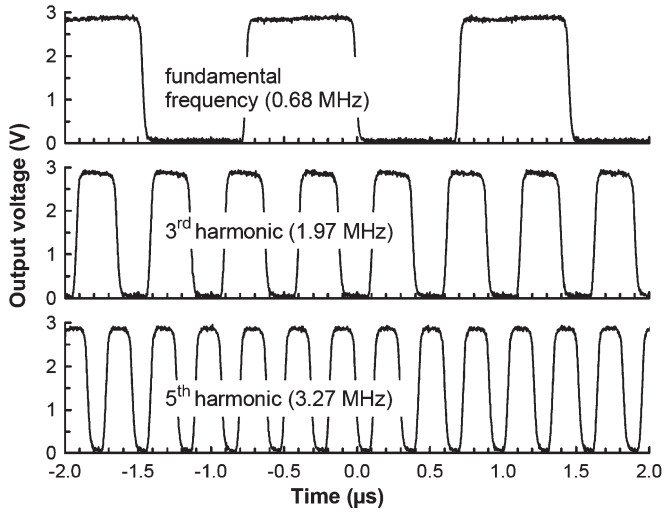

Fig. 13. Three oscillation waveforms measured for the 51-stage CMOS ring oscillator at a supply voltage $V_{\rm DD} = 5$ V ($W_{\rm NMOS} = 2$ μm, $W_{\rm PMOS} = 3$ μm, $L = 2$ μm, and the TFT channels are oriented *parallel* to the grain boundaries).

output buffer stage was designed. It consisted of one basic inverter and an additional inverter stage having P- and NMOS transistors with $W/L = 50$ μm$/2$ μm.

Fig. 12(a) shows the basic inverter transfer characteristics for a supply voltage $(V_{\rm DD})$ of 5 V. The inverter exhibits an abrupt full-range output voltage switch at an input voltage around 2.1 V. The dynamic output characteristics of the basic inverter and the inverter with wider channels $(W_{\rm NMOS,PMOS}/L = 50$ μm$/2$ μm) are compared in Fig. 12(b). The extracted rise and fall times are 103 and 80 μs for the basic inverter, and 3.9 and 1.9 μs for the inverter with wider channels. These values are, however, conservative estimates of the real switching speed, given the large parasitic capacitance present in this measurement.

The ring oscillators exhibit stable oscillations with frequencies in the megahertz range with the TFT channels oriented *parallel* to the grain boundaries. None of the ring oscillators with *perpendicularly* oriented TFTs oscillates. Fig. 13 shows the output of an unloaded 51-stage CMOS ring oscillator. In addition to the fundamental oscillation frequency of 0.68 MHz,

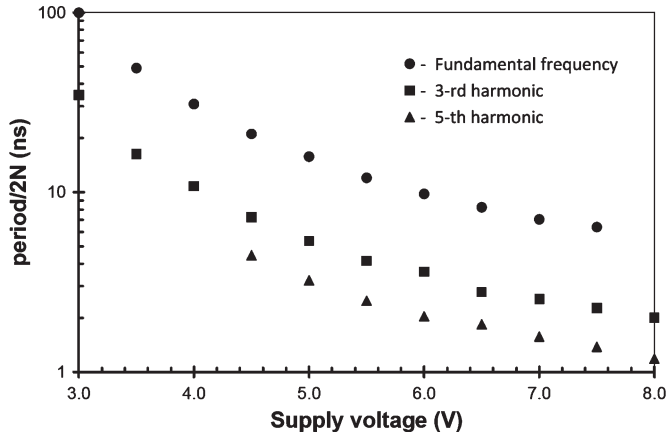

Fig. 14. Dependence of the oscillation period on $V_{\rm DD}$ for different harmonics.

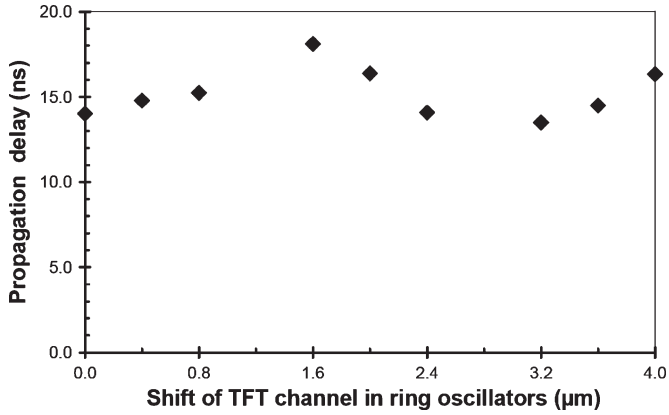

Fig. 15. Location-dependent propagation gate delay determined with the fundamental frequency mode for the ring oscillators with parallel TFT channels ($W_{\rm NMOS} = 2$ μm, $W_{\rm PMOS} = 3$ μm, and $L = 2$ μm).

odd higher harmonics (1.97 and 3.27 MHz) were measured for the same ring oscillator, in line with reports in [28] and [29]. The $V_{\rm DD}$ dependence of the oscillation periods for the three harmonics is shown in Fig. 14. By using the fundamental frequency, the propagation gate delay $t_{\rm pd}$ amounts to 14.4 ns, obtained by the following equation [30]:

$$t_{\rm pd} = \frac{T}{2N} \tag{3}$$

where T is the period of the oscillation and N is the number of stages.

Similar to the experiment with shifted TFTs (see Fig. 10), a series of 11 ring oscillators with predetermined channel locations (oriented *parallel* to the laser scanning direction and to the grain boundaries) was fabricated. Channels of all transistors in every next ring oscillator were shifted perpendicularly to the major grain boundaries for 0.4 μm with respect to the channel positions in the previous ring oscillator of the series. As stated earlier, this shift ensures the existence of oscillators with and without major grain boundaries in the channels.

Although the current flow in all these ring oscillators is parallel to the boundaries, we still observe a deviation in the device performance, leading to a lower propagation gate delay when

fewer boundaries are expected to be present in the channels (Fig. 15). This demonstrates the effectiveness of the device positioning method proposed in this paper.

III. Conclusion

We fabricated high-performance p- and n-channel poly-Si TFTs using pretextured a-Si, green-laser crystallization and activation, and a low-temperature dielectric. The pretexturing leads to large-grain poly-Si films with the grain boundaries mostly oriented along the underlying a-Si lines. The sheet resistance is lower and shows a lower variability for devices oriented *parallel* to the major grain boundaries than for *perpendicularly* oriented devices. Heavily As- and B-doped silicon films exhibit high doping activation level after laser annealing. The TFTs oriented *parallel* to the underlying a-Si lines (and therefore to the grain boundaries) exhibit significantly better electrical performance than the *perpendicularly* oriented devices.

The 51-stage CMOS ring oscillators with *parallel* TFTs were fully operational and showed an improved performance if all TFT channels were positioned in between the major grain boundaries. In contrast, the ring oscillators made of the *perpendicularly* oriented TFTs were not operational.

The described low-temperature fabrication method can be further developed for low-temperature CMOS postprocessing, after replacing the LPCVD step at 550 °C by, e.g., plasma-enhanced CVD of a-Si at temperatures lower than 400 °C. This CMOS process can be employed for large-area TFTs as well as in 3-D electronics due to its low thermal budget.

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References

[1] K. C. Saraswat, S. J. Souri, V. Subramanian, A. R. Joshi, and A. W. Wang, "Novel 3D structures," in *Proc. IEEE Int. SOI Conf.*, 1999, pp. 54–55.

[2] S. Gu, S. V. Dunton, A. J. Walker, S. Nallamothu, E. H. Chen, M. Mahajani, S. B. Herner, V. L. Eckert, S. Hu, M. Konevecki, C. Petti, S. Radigan, U. Raghuram, and M. A. Vyvoda, "Three-dimensional thin-film-transistor silicon-oxide-nitride-oxide-silicon memory cell formed on large grain sized polysilicon films using nuclei induced solid phase crystallization," *J. Vac. Sci. Technol. B*, vol. 23, no. 5, pp. 2184–2188, Sep. 2005.

[3] N. Moussy, P. Gidon, N. Carriere, W. Rabaud, B. Giffard, B. Gluck, D. Thomas, J. Prima, F. Roy, N. Casanova, J. Regolini, J. B. Chevrier, F. Collet, A. S. Ozanne-Gomila, and O. Salasca, "A highly reliable amorphous silicon photosensor for above IC CMOS image sensor," in *IEDM Tech. Dig.*, 2006, pp. 1–3.

[4] A. T. Voutsas, "A new era of crystallization: Advances in polysilicon crystallization and crystal engineering," *Appl. Surf. Sci.*, vol. 208/209, pp. 250–262, Mar. 2003.

[5] S. D. Brotherton, D. J. McCulloch, J. B. Clegg, and J. P. Gowers, "Excimer-laser-annealed poly-Si thin-film transistors," *IEEE Trans. Electron Devices*, vol. 40, no. 2, pp. 407–413, Feb. 1993.

[6] S.-M. Han, M.-C. Lee, M.-Y. Shin, J.-H. Park, and M.-K. Han, "Poly-Si TFT fabricated, 150 °C, ICP-CVD and excimer laser annealing," *Proc. IEEE*, vol. 93, no. 7, pp. 1297–1305, Jul. 2005.

[7] P. Lengsfeld, N. H. Nickel, and W. Fuhs, "Step-by-step excimer laser induced crystallization of a-Si:H," *Appl. Phys. Lett.*, vol. 76, no. 13, pp. 1680–1682, Mar. 2000.

[8] M. Nerding, R. Dassow, S. Christiansen, J. R. Köhler, J. Krinke, J. H. Werner, and H. P. Strunk, "Microstructure of laser-crystallized silicon thin films on glass substrate," *J. Appl. Phys.*, vol. 91, no. 7, pp. 4125–4130, Apr. 2002.

[9] A. Hara, F. Takeuchi, M. Takei, K. Suga, K. Yoshino, M. Chida, Y. Sano, and N. Sasaki, "High-performance polycrystalline silicon thin film transistors on non-alkali glass produced using continuous wave laser lateral crystallization," *Jpn. J. Appl. Phys.*, vol. 41, no. 3B, pp. L311–L313, Mar. 2002.

[10] C.-H. Kim, I.-H. Song, W.-J. Nam, and M.-K. Han, "A poly-Si TFT fabricated by excimer laser recrystallization on floating active structure," *IEEE Electron Device Lett.*, vol. 23, no. 6, pp. 315–317, Jun. 2002.

[11] L. Mariucci, A. Pecora, R. Carluccio, and G. Fortunato, "Advanced excimer laser crystallization techniques," *Thin Solid Films*, vol. 383, no. 1/2, pp. 39–44, Feb. 2001.

[12] T.-K. Chang, C.-W. Lin, C.-C. Tsai, J.-H. Lu, B.-T. Chen, and H.-C. Cheng, "High-performance poly-Si thin film transistors crystallized by excimer laser irradiation with A-Si spacer structure," *Electrochem. Solid-State Lett.*, vol. 8, no. 1, pp. G14–G16, 2005.

[13] P. C. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, "Formation of location-controlled crystalline islands using substrate-embedded seeds in excimer-laser crystallization of silicon films," *Appl. Phys. Lett.*, vol. 79, no. 12, pp. 1819–1821, Sep. 2001.

[14] I. Brunets, J. Holleman, A. Y. Kovalgin, A. A. I. Aarnink, A. Boogaard, P. Oesterlin, and J. Schmitz, "Green laser crystallization of a-Si films using preformed a-Si lines," *ECS Trans.*, vol. 3, no. 8, pp. 185–191, 2006.

[15] I. Brunets, A. Y. Kovalgin, J. Holleman, and J. Schmitz, "Poly-Si stripe TFTs by grain-boundary controlled crystallization of amorphous-Si," in *Proc. ESSDERC*, 2008, pp. 87–90.

[16] Y. Kuo, "Thin-film transistor and ultra-large scale integrated circuit: Competition or collaboration," *Jpn. J. Appl. Phys.*, vol. 47, no. 3, pp. 1845–1852, 2008.

[17] A. Hara, K. Yoshino, F. Takeuchi, and N. Sasaki, "Selective single-crystalline-silicon growth at the pre-defined active region of a thin film transistor on glass by using continuous wave laser irradiation," *Jpn. J. Appl. Phys. Part 1*, vol. 42, no. 1, pp. 23–27, 2003.

[18] I. de Wolf, "Micro-Raman spectroscopy to study local mechanical stress in silicon integrated circuits," *Semicond. Sci. Technol.*, vol. 11, no. 2, pp. 139–154, Feb. 1996.

[19] A. Bary, B. Mercey, G. Poullain, J. L. Chermant, and G. Nouet, "EBIC and conductance measurements in poly- and bicrystalline silicon," *Rev. Phys. Appl.*, vol. 22, no. 7, pp. 597–601, 1987.

[20] S. Christiansen, P. Lengsfeld, J. Krinke, M. Nerding, N. H. Nickel, and H. P. Strunk, "Nature of grain boundaries in laser crystallized polycrystalline silicon thin films," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5348–5354, May 2001.

[21] C. Z. Tan, J. Arndt, and H. S. Xie, "Optical properties of densified silica glasses," *Phys. B*, vol. 252, no. 1/2, pp. 28–33, Jul. 1998.

[22] S. Akiyama, S. Ogawa, M. Yoneda, N. Yoshii, and Y. Terui, "Multilayer CMOS device fabricated on laser recrystallized silicon islands," in *IEDM Tech. Dig.*, 1983, pp. 352–355.

[23] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. New York: Wiley, 2006, pp. 500–501.

[24] T. Kamins, *Polycrystalline Silicon for Integrated Circuits and Displays*, 2nd ed. Norwell, MA: Kluwer, 1998, pp. 230–231.

[25] A. Boogaard, A. Y. Kovalgin, I. Brunets, A. A. I. Aarnink, J. Holleman, R. A. M. Wolters, and J. Schmitz, "Characterization of SiO_2 films deposited at low temperature by means of remote ICPECVD," *Surf. Coat. Technol.*, vol. 201, no. 22/23, pp. 8976–8980, Sep. 2007.

[26] A. Boogaard, A. Y. Kovalgin, and R. A. M. Wolters, "Net negative charge in low-temperature SiO_2 gate dielectric layers," *Microelectron. Eng.*, vol. 86, no. 7–9, pp. 1707–1710, Mar. 2009.

[27] S.-I. Saito, K. Torii, Y. Shimamoto, O. Tonomura, D. Hisamoto, T. Onai, M. Hiratani, and S. Kimura, "Remote-charge-scattering limited mobility in field-effect transistors with SiO_2 and Al_2O_3/SiO_2 gate stacks," *J. Appl. Phys.*, vol. 98, no. 11, pp. 113 706-1–113 706-9, Dec. 2005.

[28] N. Sasaki, "Higher harmonic generation in CMOS/SOS ring oscillators," *IEEE Trans. Electron Devices*, vol. ED-29, no. 2, pp. 280–283, Feb. 1982.

[29] T. W. Houston, "Comments on 'Higher harmonic generation in CMOS/SOS ring oscillators'," *IEEE Trans. Electron Devices*, vol. ED-30, no. 8, pp. 958–959, Aug. 1983.

[30] L. Forbes, "n-channel ion-implanted enhancement/depletion FET circuit and fabrication technology," *IEEE J. Solid State Circuits*, vol. SSC-8, no. 3, pp. 226–230, Jun. 1973.

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