# Strong Efficiency Improvement of SOI-LEDs Through Carrier Confinement

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***Abstract*—Contemporary silicon light-emitting diodes in silicon-on-insulator (SOI) technology suffer from poor efficiency compared to their bulk-silicon counterparts. In this letter, we present a new device structure where the carrier injection takes place through silicon slabs of only a few nanometer thick. Its external quantum efficiency of $1.4 \cdot 10^{-4}$ at room temperature, with a spectrum peaking at 1130 nm, is almost two orders higher than reported thus far on SOI. The structure diminishes the dominant role of nonradiative recombination at the $n^+$ and $p^+$ contacts, by confining the injected carriers in an SOI peninsula. With this approach, a compact infrared light source can be fabricated using standard semiconductor processing steps.**

***Index Terms*—Integrated optics, integrated optoelectronics, light-emitting diodes (LEDs), light sources, luminescent devices, optoelectronic devices, semiconductor devices, silicon-on-insulator (SOI) technology.**

## I. Introduction

RECENT progress in silicon light-emitting diodes (LEDs) has led to reported internal quantum efficiencies around 3%, potentially offering a new integration approach for very large scale integration (VLSI) circuits with optical communication [1]. It was found that high-purity silicon, with low doping levels and low defect density, leads to the highest efficiency at the band-to-band recombination wavelength [2], [3]. However, the silicon LEDs with the highest efficiency emit infrared light from an extended volume within the silicon wafer. This lack of spatial confinement prohibits the formation of compact light-emitting arrays, limits switching speed, and will lead to undesired crosstalk problems in integrated microsystems. One approach to a better confinement of the light emission is to form a silicon LED in silicon-on-insulator (SOI) material. This is attractive, because both VLSI electronics and integrated optics are commonly fabricated on SOI wafers [4]. Yet, the highest reported efficiency of silicon LEDs on SOI is two orders of magnitude lower than in bulk-silicon LEDs [5].

In this letter, we introduce a novel device structure that reduces the nonradiative recombination by confining the carriers in an SOI peninsula. The device exhibits a record-high quantum efficiency for SOI-LEDs, closing in on bulk-silicon efficiency levels. It is manufactured with normal VLSI processing procedures.

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## II. Experimental

The starting material is a 100-mm p-type "Smart-Cut" SOI substrate. The device layer is a 200-nm p-type silicon with a resistivity of 10–100 $\Omega \cdot$ cm. The SOI layer is first etched into islands. Then, through a repeated local oxidation of silicon, in combination with buffered-HF wet-etching and ellipsometric film thickness measurement, we locally create very thin silicon regions (5–25 nm) of 2-$\mu$m wide and 60-$\mu$m long. Oxidation on ultrathin silicon becomes self-limiting [6], [7], enlarging the process window for this approach. On each wafer, four different thin-silicon thicknesses are realized to minimize the impact of wafer-to-wafer process variations. The thickness of the thinned-down SOI layer was verified using a bright-field high-resolution transmission electron microscopy (HRTEM). Example HRTEM images are shown in the inset of Fig. 1(a). The thinned layer thickness varies with $\pm 2$ nm across the wafer, determined by the SOI uniformity.

After growing a 12-nm thermal oxide, highly doped $p^+$ and $n^+$ regions were formed by annealing $5 \times 10^{15}$ cm$^{-2}$ $BF_2^+$ and $As^+$ implants at 800 °C for 30 min. Then, a 300-nm P-doped poly-silicon gate electrode was deposited and patterned over the thinned regions. After opening contact windows, metal contacts were made by sputtering and patterning TiW/Al(Si) interconnect. Fig. 1(a) shows a schematic drawing of the device. Electrical characteristics were measured using a Cascade probe station and an Agilent 4156C parameter analyzer. The integrated electroluminescence (EL) intensity emitted from our devices was recorded by a calibrated Xenics InGaAs near-infrared camera via a microscope with near-infrared objective lenses; the camera can be extended with a Specim spectroscope. The optical setup was calibrated using a halogen lamp, a Ge detector, and a Spectralon Lambertian surface. The calibrated energy measured from the device was then divided by the photon energy to obtain the number of collected photons. Then, the external quantum efficiency is defined as the ratio of the number of collected photons and the number of injected electrons.

## III. Results and Discussion

The basic philosophy behind the device architecture is that a volume of lowly doped monocrystalline silicon can emit infrared light with reasonable efficiency (through phonon-assisted band-to-band recombination), as long as competing nonradiative recombination mechanisms [8] are well

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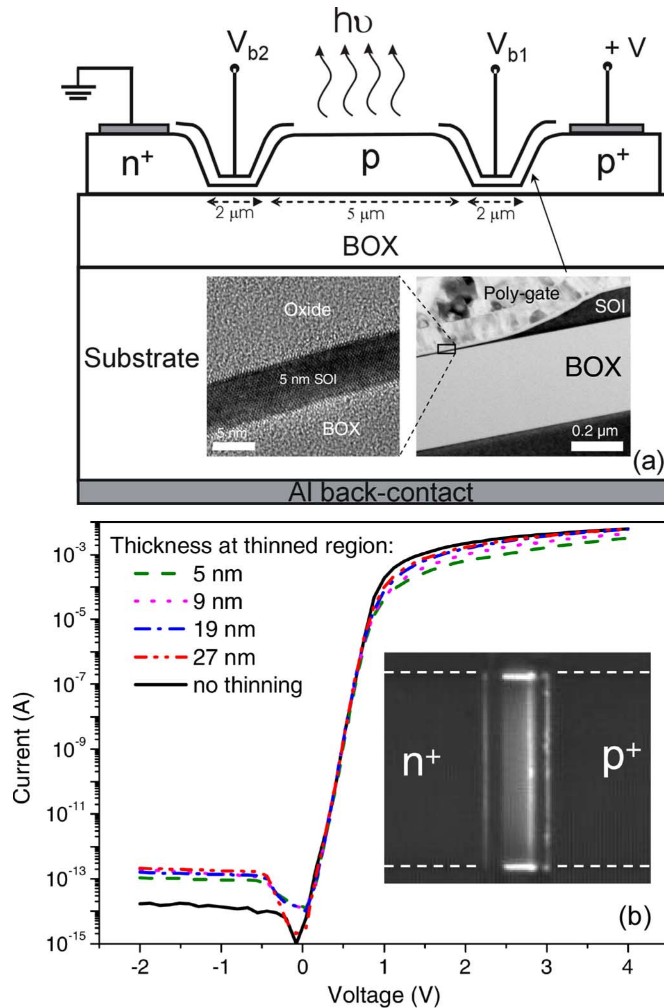


Fig. 1. (a) Schematic cross section of the $p^+/p/n^+$ diode. The infrared emitted light is collected from the front side of the wafer. The distance between the thinned-down regions is 5 $\mu$m; thinned-down regions are 2-$\mu$m wide, and the device length is 60 $\mu$m. The insets show cross-sectional HRTEM images of the thinned-down silicon regions with thickness of 5 nm. (b) $I$–$V$ characteristics of five diodes with the same structure, except the thickness of the thinning-down region. Inset is a top-view infrared image of the device (biased at 1 mA), taken with the InGaAs infrared camera via a 50×-microscope. The dashed lines indicate the boundary of the SOI island. The bright central area is the active region (p-type peninsula); the two outer bright lines are interpreted as wave-guided light escaping from the edge of the two poly-gates. The integrated intensity from the edges amounts to 10%–15% of the total light emission.

suppressed. To this purpose, high-quality Si is chosen (using SmartCut wafers); the silicon layer is enclosed by thermally grown $SiO_2$ with high-quality interfaces; and the doping level is maintained as supplied. Under these circumstances, we expect the recombination at the $p^+$ and $n^+$ contacts [9] as well as the Si-$SiO_2$ interfaces [10] to dominate the nonradiative recombination. If the recombination at the $p^+$ and $n^+$ contacts is effectively suppressed by creating a barrier to this recombination, the highest possible internal efficiency in this geometry is close to 1%, assuming a surface recombination velocity of $s_r =$ 10 cm/s [11].

Current–voltage $(I–V)$ characteristics of devices were measured between the $n^+$ and $p^+$ regions showing diode operation with a slope of 72 mV/decade. Holes and electrons are injected into the central area through the thinned regions. The access resistance of this diode is high and increases with decreasing silicon thickness. By application of a negative voltage $(V_{b1})$ to the poly-gate next to the $p^+$ region and a positive voltage $(V_{b2})$ to the poly-gate next to the $n^+$ region, the carrier density in the thinned silicon layer is enhanced. This leads to a good forward conduction: At $V_{b1} = -1$ V and $V_{b2} = +1$ V, 1 mA flows at ~2-V forward bias. Fig. 1(b) shows the $I$–$V$ characteristics of five diodes with varying thinned-region thickness. The distribution and the spatial location of the emitted light can be seen in a top-view infrared image of the device [inset in Fig. 1(b)].

We compared the electroluminescence of five diodes, that only differ in the thickness of the thinned access silicon film. Their EL spectra with the same intensity peak at ~1130-nm wavelength are recorded in Fig. 2(a). The electroluminescence increases with as much as a factor of 24 when access regions are thinned from 145 to 5 nm, as quantified by the integrated EL intensity in the inset of this figure. This enhancement of electroluminescence, in identical silicon volumes (on the same wafer) but with different access regions, is explained by a confinement of the injected carriers in this volume.

Three effects may contribute to the carrier confinement in the realized structure.

1) By administering the appropriate gate potential, minority carriers experience a potential barrier in this thin film.
2) Injected carriers have difficulty in finding the exit through diffusion, as it is geometrically small.
3) The silicon layer is so thin, that bandgap widening effects may play a role (below ca. 10 nm).

The effect of gate voltages was studied on a diode with 19-nm thinned regions, forward-biasing the diode with 1 mA under two biasing conditions: first, with both poly gates grounded and, second, with gate biases of $V_{b1} = -1$ V and $V_{b2} = +1$ V. The latter condition creates a high electron density in the thin silicon region connected to the $n^+$ contact and a high hole density in the thin film adjacent to the $p^+$ contact. Not only does this reduce the diode's external resistance but holes, injected into the p-type silicon, now encounter a potential barrier on their way to the $n^+$ region, and similar for electrons, vice versa. We observe a factor 3 higher integrated electroluminescence under the biased condition.

Thinning down the access regions has a much stronger effect [inset of Fig. 2(a)]. A monotonous increase of EL is observed, while the quantum-size effect is known to be significant only when the silicon layer thickness is below 10 nm [13], [14]. The electroluminescence is inversely proportional to the access region thickness in the full range. This is evident that the effect has a purely geometrical origin. The external quantum efficiency of the device at room temperature under a 1-mA forward current reaches $1.4 \cdot 10^{-4}$ for the device with the thinnest SOI layers (5 nm). The light output–current $(L–I)$ characteristics of those diodes at room temperature are shown in Fig. 2(b). Note that the surface of this device did not receive any special treatment to maximize the outcoupling of light [1].

The temperature dependence of the integrated EL intensity of the fabricated devices was investigated in the range of 253–473 K. An increase in the integrated EL intensity with the temperature was observed for devices with and without thinning when the gates are floating. This trend is in line with the bulk-silicon LED behavior [3], [12], [15]. However, an

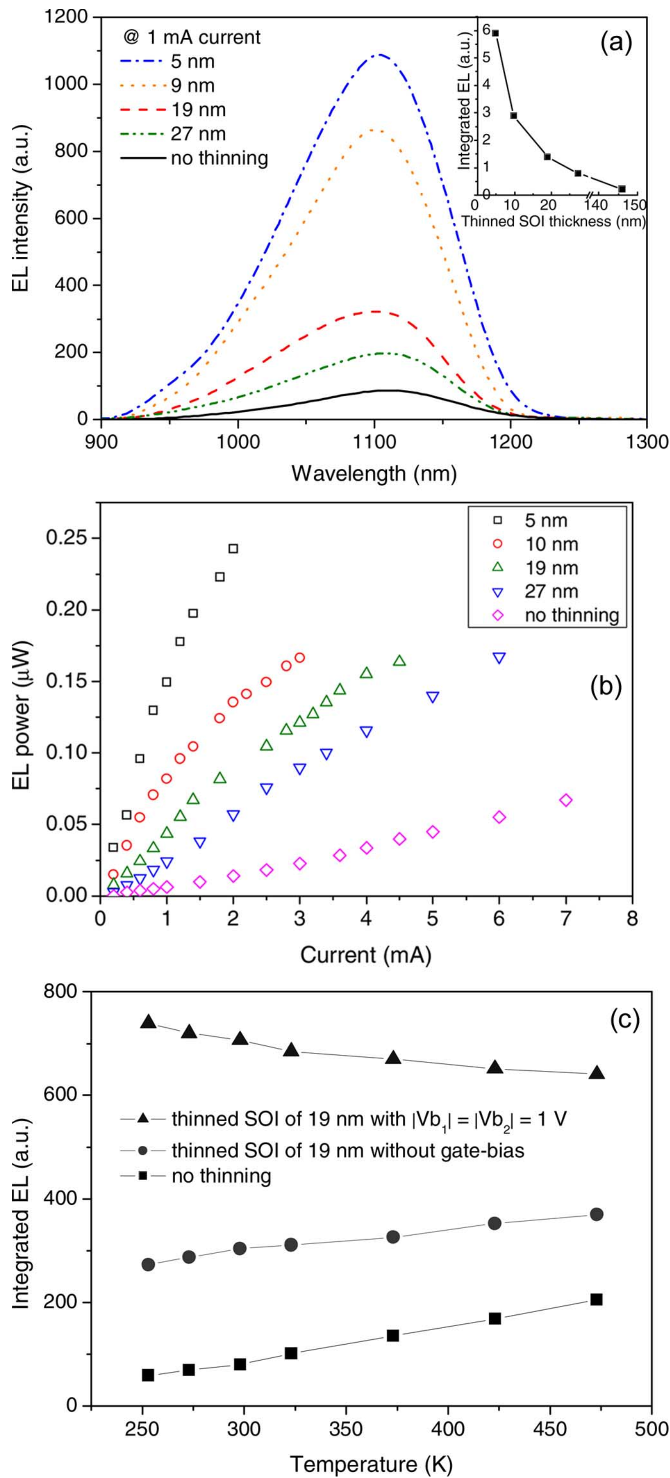


Fig. 2. Light emission properties of the fabricated SOI-LEDs. (a) Emission spectra of five devices with varying access region thickness. Inset: Integrated electroluminescence as a function of access silicon thickness. (b) $L$–$I$ characteristics of five diodes at room temperature at gate biases of $V_{b1} = -1$ V and $V_{b2} = +1$ V. (c) Integrated electroluminescence as a function of device temperature for diodes with and without thinned access regions; and varying the gate biasing.

opposite temperature dependence was seen when biasing the poly-gates, as shown in Fig. 2(c). In confined-carrier systems, the confinement is normally reduced with increasing temperature. In our device, this happens through the increase of the minority carrier concentration in the thin regions at fixed gate potential. This qualitatively explains the weak thermal quenching. The found temperature dependence behavior indicates that our devices work efficiently at around room temperature and above, allowing the utilization of this emission process in integrated microsystems.

## IV. Conclusion

A compact Si LED realized on SOI is presented. Its operation is based on phonon-assisted band-to-band recombination in high-quality silicon. Using thinned-down gated silicon access regions, the quantum efficiency is shown to improve with almost two orders of magnitude. The device exhibits a record of electroluminescence efficiency for SOI-LEDs. Compared to bulk-silicon LEDs, it has the advantage of a laterally and vertically well-defined light emission spot and, possibly, a higher switching speed.

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