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Seedless electroplating on patterned silicon

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Abstract
Nickel thin films have been electrodeposited without the use of an additional seed layer, on highly doped silicon wafers. These substrates conduct sufficiently well to allow deposition using a peripherical electrical contact on the wafer. Films 2 μm thick have been deposited using a nickel sulfamate bath on both n+- and p+-type silicon wafers, where a series of trenches with different widths had been previously etched by plasma etching. A new, reliable and simple procedure based on the removal of the native oxide layer is presented which allows uniform plating of patterned substrates.

1. Introduction

The relatively inexpensive equipment together with the possibility of obtaining excellent via/trench filling properties [1] is the major advantage of electrodeposition over other methods of thin film production. However, electrodeposition has one feature that can be a major disadvantage, namely the need for a conducting substrate or a conducting seed layer previously sputtered or evaporated on top of the substrate. The possibility of electroplating directly on semiconducting silicon substrates relieves the need for this seed layer making the process simpler. This has direct consequences in microelectromechanical systems (MEMS). For example, in three-dimensional engineering, a (highly doped) silicon wafer can be processed using conventional micromachining techniques such as KOH wet chemical etching and SF_6/C_4F_8-based dry plasma etching. Subsequently, the silicon structure can be uniformly coated with nickel, without any further deposition steps. This process leaves the silicon device completely covered with a nickel film, making it more corrosion resistant in harsh environments or when in contact with aggressive fluids.

Although electroplating is typically carried out on a metal seed layer, deposition on silicon is not new and it has been reported a few times for different metals and metal alloys [2, 3]. In the following sections, a new procedure to electroplate nickel directly onto highly doped silicon wafers will be presented. These wafers have high aspect ratio structures and the electrical contact to them is made by a circular flexible contact on top, at the edge of the wafer, instead of a backplate.

2. Experimental setup

2.1. Description of the system

A conventional 8 l sulfamate bath[1], containing 300 g l^{-1} of nickel sulfamate together with nickel chloride and boric acid, is used for the electroplating of nickel. The solution is agitated, continuously filtered and kept at a temperature around 55 °C during plating. The anode is an insoluble Ti mesh coated with Pt, and the cathode is the wafer that should be electroplated. In this cathode, electrical contact is made to the wafer by a peripherical contact. An additional anode probe can be inserted in the electrolyte to apply a potential difference between the wafer and the bath (figure 1).

For micromechanical devices, it is very important to obtain films with low stress values and low roughness. Both properties depend on operating variables such as temperature and current density. Stress and roughness values have been optimized for microelectromechanical system (MEMS) applications with respect to bath parameters using 4in silicon wafers with a conducting layer on top. This conducting layer was made by evaporating a 10 nm thick Cr layer and a 100 nm thick Au layer. After evaporation the wafer is scanned in two perpendicular directions with a surface profilometer in order to get the deflection of the wafer prior to nickel deposition. A 9 μm thick nickel film is electroplated and the wafer is scanned again. The deflection difference is then related to the stress using Stoney's equation [4]. This experiment was repeated for current densities (J) from 2 to 7 A dm^{-2} at

[1] ECSI Fibrotools, model IKO, Electrochemical Systems Inc., 96 Ford Road Denville, NJ 07834, USA (www.fibrotools.com).

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Table 1. Bath optimization for MEMS. Stress is given in MPa and the roughness is given by the appearance of the wafer, varying from +++ very shiny to - - - very dull.

	2 A dm^{-2}	3 A dm^{-2}	4 A dm^{-2}	5 A dm^{-2}	6 A dm^{-2}	7 A dm^{-2}
40 °C	−50/+	−40/o	−20/-	0/- -	20/- -	50/- - -
45 °C	−30/++	−50/+++	−60/+	−30/+	−10/-	10/-
55 °C	10/+	0/++	−10/+++	−10/+++	−10/++	−10/++
60 °C	20/o	20/o	10/o	0/+	0/++	−10/++

Table 2. Values of the resistivity (ρ), the sheet resistance ($R_\square = \rho/t$) and the wafer 'through' resistance ($R_\perp = \rho t/A$, with $A = 0.66$ dm^2 in our case) as a function of thickness (t) and material.

	p	n	p$^+$	n$^+$	Au	Cr	Au/Cr/p	SiO_2
t (μm)	525	525	475	525	0.1	0.01	–	10^{-3}
ρ ($\Omega\cdot\mu$m)	50 000[a]	50 000[a]	150[a]	200[a]	0.022[b]	0.13[b]	–	10^{18} [b]
$R_\square$ (Ω)	95	95	0.3	0.4	0.22	13	0.2	10^{21}
$R_\perp$ (Ω)	0.004	0.004	1.1×10^{-5}	1.6×10^{-5}	≈0	≈0	0.004	10^6

[a] Okmetic Oyj.

[b] CRC Handbook of Chemistry and Physics.

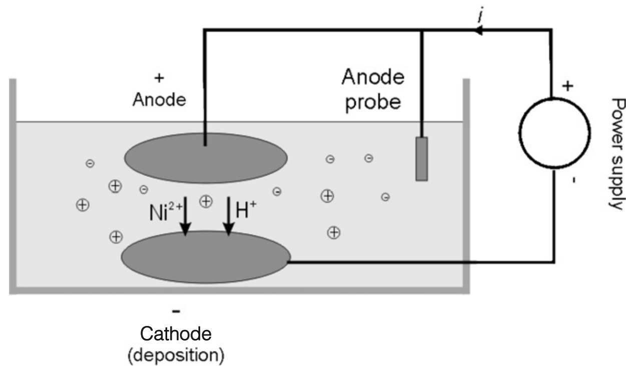

Figure 1. Schematic representation of the setup for nickel electroplating.

40 °C, 45 °C, 55 °C and 60 °C. The pH value of the solution was maintained at values between 4 and 4.5. The results are shown in table 1.

From the results, it can be concluded that on chromium–gold seed layers and for a bath pH value between 4 and 4.5, the best results are obtained for a plating current density between 4 and 5 A dm^{-2} and a bath temperature of 55 °C. These optimized parameters have been used during all experiments for seedless plating of nickel on silicon wafers.

2.2. Theoretical considerations

Electroplating relies on making electrical contact from a power supply to an ionic solution through an anode and a cathode (wafer). For the experiments described in this paper, the electrical contact to the wafer is made through contacts along the circumference on the wafer (peripheral contact), see figure 2. In order to avoid significant resistance to the current and to provide a uniform current distribution, the sheet resistance ($R_\square$) should be low, typically under 0.5 Ω per square [5]. In the case of a wafer with a 0.01 μm Cr adhesion layer and a 0.1 μm thick Au conducting layer on top, this resistance is about 0.2 Ω per square (table 2). Without this conducting layer, normally doped silicon wafers (p- or n-type) show a much higher resistance by about two orders of magnitude. Highly doped silicon wafers (p+- or n+-type) have a resistance comparable to that of a normal wafer with a conducting layer. This means that only highly doped Si wafers can conduct sufficiently well to allow electrodeposition in the same way as wafers with a conductive seed layer on top. However, when the contact to the cathode is made by a backplate electrode (figure 2(*b*)), the resistance through the wafer, $R_\perp$, is the important parameter. From table 2, it can be concluded that in this configuration, also normally doped wafers could be plated without a seed layer.

In practice, another factor has to be taken into account when plating without a seed layer. An oxide layer, SiO_2 layer, of about 1 nm thickness is present on silicon wafers as received from the supplier. This so-called native oxide forms on every bare silicon surface exposed to air. Although very thin, it has a very high resistance to the current (table 2), which can be enough to avoid electrical contact between the electrode and the wafer, making it impossible to proceed with electroplating.

Therefore, removing the native oxide layer from the surface of the wafers and avoiding getting it again is a key issue during our experiments. The procedure is not trivial because the removal of the native oxide using, for example, HF solutions results in hydrophobic surfaces. These surfaces are indeed conducting sufficiently, but repel water and water-based solutions such as the nickel sulfamate electrolyte. This can be a problem that has to be resolved for successful plating of patterned wafers as will be discussed in section 4.3.

3. Bare Si wafers

The experiments were carried out with four types of (1 0 0)- and (1 1 1)-oriented silicon wafers: p/boron, n/phosphorus, p+/boron and n+/antimony. The wafers were cleaned using HNO_3 to remove organic contaminants and then etched in 1% HF, to remove the native oxide and inorganic particles from the wafer surface. It is known from the literature [6] that silicon surfaces etched in dilute HF solutions are highly resistant to oxidation in air due to the termination with hydrogen.

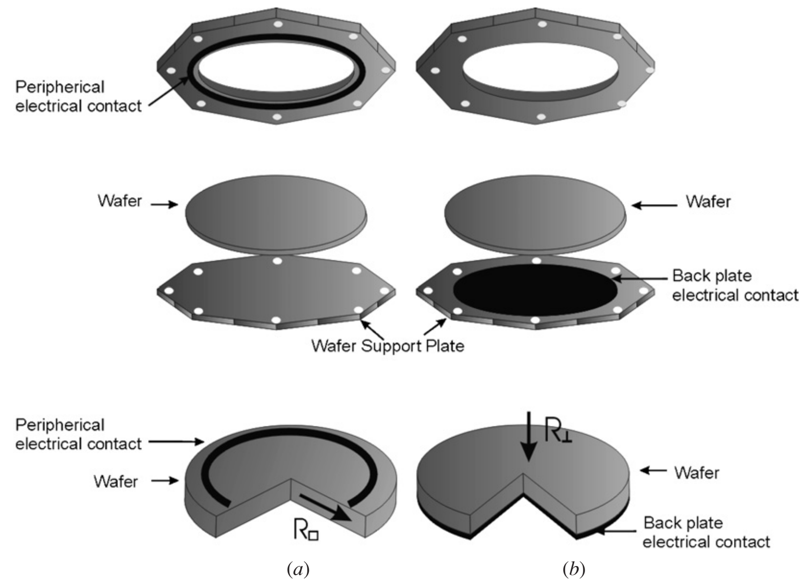

Figure 2. Schematic drawing of the wafer holder with (*a*) peripherical electrical contact or (*b*) a backplate contact with respectively the effective resistances $R_{\square}$ and $R_{\perp}$.

After this the wafers were rinsed just for a few seconds with deionized water using a shower head in order to remove any acid left and then spin dried.

While the oxide growth on HF-treated Si surfaces proceeds extremely slowly in air, it was observed that just a few seconds in the electrolyte at 55 °C were enough to hinder the growth of nickel. In order to minimize oxidation reactions between the substrate and the constituents of the electrolyte, the power supply was switched on with a second anode probe inserted in the bath, prior to the immersion of the wafer (figure 1). Wafers have been electroplated at 55 °C for 3 min with a current density of 4 A dm^{-2}. This will lead to an expected thickness of 2 μm.

Following this procedure, successful results are obtained for the highly doped wafers (n+- and p+-types), n- and p-type wafers remain unplated. In our setup, the contact to the silicon wafers of the plating power supply is applied at the perimeter of the wafers only, on the surface to be plated. Using this configuration, the effective resistance is determined by $R_{\square}$ (as can be seen from figure 2) which is directly proportional to the resistivity (ρ). Most probably due to their much higher resistivity, the n- and p-type wafers are not plated. Although very inconvenient when plating normally doped wafers, our configuration for the electrical contact has a major advantage in the case of 3D plating. When a structure has to be encapsulated with nickel the use of a backplate electrode would impede any plating at the backside of the wafer. In the case of a peripherical contact the backside may be free and may be plated too.

4. Patterned Si wafers

An important issue during MEMS processing is the ability to plate and fill high aspect ratio structures conformally, enabling a void free nickel filled trench. Conformal plating is an even growth from all surfaces resulting in a deposit of equal thickness at all points. When a seed layer is used, an insulating photoresist structure is made on top of the wafer, which is then electroplated. In this case, the structures to be plated have nonconducting sidewalls and the trenches are filled evenly from the bottom up to the desired height. Electroplating occurs then only on those areas that are not covered by the mask. After deposition the masking material can subsequently be removed. In the experiments described in this paper, highly doped Si wafers are patterned after which the entire wafer surface is plated. In this case there is no mask, and everything is conducting, including the walls of the trenches. This leads to a different plating mechanism.

In order to optimize this trench filling mechanism, highly doped wafers were processed using the procedure as described in the previous section. The results led to an adapted procedure. Although the results improved, this adapted procedure was not yet satisfying and a final procedure was introduced.

4.1. Initial procedure

The trench pattern used in our experiments was defined by optical lithography using a Karl Süss mask aligner. The p+-type (1 0 0) oriented silicon wafers from Okmetic Oyj were dehydrated for 10 min on a hotplate at 120 °C. After spin-coating with the adhesion promoter HMDS and a 3.5 μm thick positive resist layer (Olin 908-35), they were exposed for 12 s to 9 mW cm^{-2} UV light. After exposure, the resist layer was developed in Olin OPD 4262. The wafers were then plasma etched using C_4F_8/SF_6 steps (BOSCH etching) forming vertical trenches[2] [7].

After standard HNO_3 cleaning to remove the photoresist, the wafers were ashed in oxygen atmosphere for 30 min at 800 °C to remove the fluorocarbon film which is deposited during the plasma etching process on the walls of the trenches. The wafers were immersed for 5 min in 50% HF solution

[2] Adixen Micro Machining Systems (www.adixen.com), Alcatel Vacuum Technology, Annecy Cedex, France.

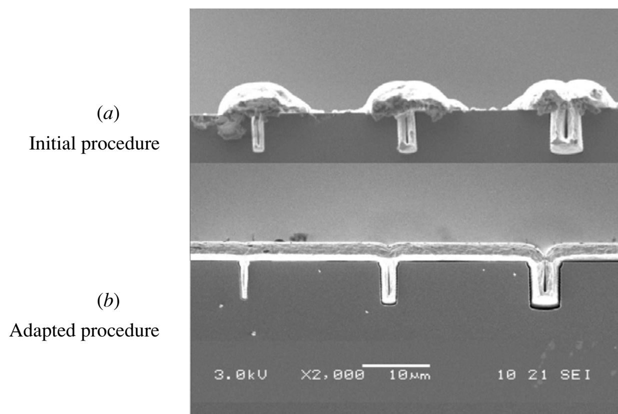

Figure 3. Cross section of a p+ silicon wafer with 7 μm deep trenches and electroplated nickel on top.

to remove the oxide film created during ashing and to lift the carbon residue from the oxide surface. Just prior to nickel plating the wafers were dipped in 1% HF, rinsed with a shower head and spin dried. Wafers following this initial procedure showed clear preferential areas to plate: the walls and bottom of the trenches (figure 3(*a*)). We suppose that contact with water after the HF dip is the cause.

4.2. Adapted procedure

In order to avoid any contact of the surface of the wafer with water, it was decided to immerse the wafers in ethanol directly after the 1% HF dip and to spin them dry afterwards. This new step in the processing led to uniform coverage of the structures (figure 3(*b*)).

At this stage it was also decided to eliminate the 50% HF step. To remove the oxide layer, 1% HF solution for 5 min was found to be sufficient.

It is not yet fully clear what is causing the preferential growth of nickel in the trenches when water is used and why using ethanol this problem is not found.

4.3. Final procedure

A consequence of removing the oxide layer with a HF solution is that wafers become hydrophobic, i.e. the wafer surface tends to avoid contact with water. However, the electroplating solution is water-based and therefore the silicon wafers tend to avoid contact with the nickel sulfamate, leading to trapped air bubbles in the structures. Especially, the high aspect ratio smaller structures show this problem, resulting in bubble-shaped areas that are hardly plated or not at all plated (figure 4(*a*)). As the bubble-shaped areas were always to be found on the same side of the trenches all over the wafer, it was concluded that air was trapped during immersion of the wafer in the electrolyte.

This inherent problem can be solved by spraying the wafers with ethanol just before introducing them into the plating bath. Although the wafers are hydrophobic, they are completely wetted with ethanol. In this way, air bubbles are avoided leading to successful plating of all structures (figure 4(*b*)). A big advantage of this wetting method is that due to the temperature of the bath, the ethanol is expected to evaporate, leaving no traces in the bath solution as would be the case with conventional wetting agents. Moreover, using conventional wetting agents, the wafers are typically conditioned for a few minutes inside the solution prior to starting the current supply. This procedure would be fatal for hydrogen-terminated silicon because the bath is oxidizing the silicon for zero current.

The final procedure of direct nickel plating on highly doped silicon is then as follows:

- photolithography,
- deep trench plasma etching[3],
- HNO_3 cleaning,
- ashing at 800 °C in oxygen[4],
- 1% HF dip for 5 min,
- ethanol dip for 5 min[5],
- spin dry,
- mount wafer on plating holder,
- potential is applied using the additional anode probe,
- spray wafer with ethanol,
- immerse wafer in electrolyte,
- plate with nickel.

5. Buried channels

Using this final procedure, trenches have been used as the basis for the fabrication of microchannels buried in n+ Si wafers [8] (figure 5). The wafer is covered first with photoresist and patterned by lithography and directional etching. Trenches are conformally coated with a polymer which is removed at the bottom of the trench. The structure is isotropically etched in the bulk of the substrate. After stripping the coating the structure is filled with nickel. Depending on the thickness of the nickel film and the dimensions, the trenches may be completely sealed.

Three different wafers were prepared using different etch times: 1, 3 and 9 min, which led to depths of around 6, 13 and 23 μm, respectively, for the 2 μm wide trench. The etch depth does not increase linearly with time due to the so-called RIE lag effect, i.e., for increasing aspect ratio (depth/width ratio) the etch rate slows down [9]. The samples were coated with nominally 2 μm of nickel (figure 6). In order to observe the cross section of the trenches the wafers are introduced into liquid nitrogen for a moment and then broken along one of the crystal lines. In the close-ups it can be observed that the growth of the nickel layer is still in its early stage for the deepest trench. There, the 3D nickel island growth can be clearly noted. For the other two depths, the islands have already coalesced forming a continuous film. The nucleation and growth of electroplated nickel follows the Volmer–Weber model [10].

During electroplating of high aspect ratio structures with different widths, the deposition rate decreases with increasing depth. This is probably due to the combination of two effects: diffusion and electric field effects. For deep narrow trenches

[3] This plasma etching can be BOSCH or cryogenic.
[4] Only needed in the case of BOSCH etching.
[5] IPA can also be used when the resist should not be removed.

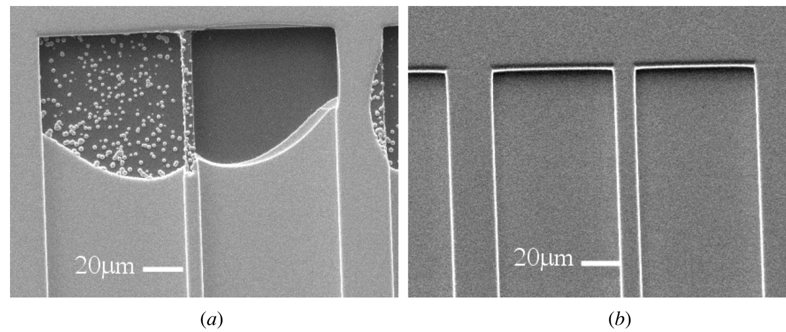

Figure 4. Top view of a silicon trench on an n+ wafer, covered with 2 μm nickel film. (*a*) Adapted procedure: in the left trench an air bubble was trapped and released after some time, and in the right one the bubble stayed all the time, inhibiting plating. (*b*) Result after improved wetting conditions using the final procedure.

Figure 5. Buried channels fabrication scheme.

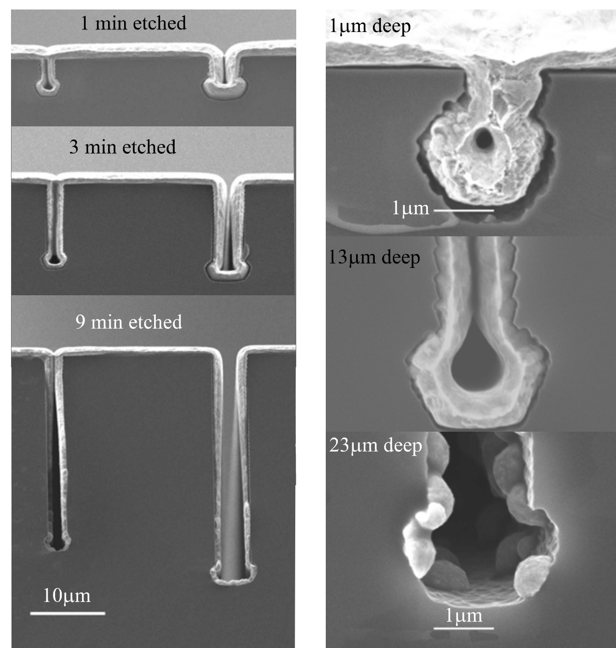

Figure 6. Cross sections of the nickel electroplated buried channels with a film thickness of about 2 μm. On the left, 2 μm and 4 μm wide trenches are shown for different etching times. On the right, close-ups of the 2 μm trenches show the difference in growth at the bottom as a function of their depth.

mass transfer takes place via diffusion, which means that the nickel ions move from a higher to a lower concentration inside the trench. If the supply of nickel ions is hampered, a concentration distribution inside the trench can be expected. On the other hand, due to the trenches the electric field will also be disturbed. It is expected that the plating solution is sufficiently conducting to ensure an equipotential condition inside the trench. Due to the decreasing ionic concentration the thickness of the outer Helmholtz plane [11] will increase and, thus, the electric field will decrease down the trench. A thorough study of these effects is necessary to reveal the dominant cause.

The use of reversed pulsed plating [12] could be the solution to obtain high aspect ratio trenches filled evenly from the bottom without voids. In pulse reversal plating, positive as well as negative (anodic) dc current pulses separated by periods of zero current are applied to the wafer. This way, nickel is deposited during the forward pulse current. The nickel content inside the trench is replenished during the zero current by diffusion. During the reversed pulse etching of nickel takes place, especially at the corner sites. For our system this means that specifically that at the edges of the trench the nickel is removed at a higher rate than at the bottom. This way closing of the trench can be avoided and conformal coverage can be

achieved. Some experimental work should be done in order to verify this method.

6. Conclusion

Electroplated nickel films have been successfully deposited on highly doped silicon wafers using a peripherical electrical contact. A method to obtain conformal deposition in deep structures has been presented, where all the efforts are put in removing the native oxide layer and avoiding getting it again. Both applying the plating potential with an additional anode probe before immersion in the electrolyte and the use of ethanol instead of water after an HF dip, are found to be crucial and result in uniform filling. The problem of air bubbles being trapped in the trenches as the wafer is introduced into the solution has been solved using ethanol, this time as a surfactant.

The procedure presented here is a simple method to electroplate highly doped wafers which leads to full coverage of patterned wafers, with for example trenches. For deep and narrow structures, such as buried channels, it was found that at the bottom, the nickel layer is thinner than on the top. Future studies are necessary to clarify the causes of this effect.

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