Guest Editorial

THIS special issue consists of papers which have been presented at the 23rd European Solid-State Circuits Conference, held September 16–18, 1997 in Southampton, U.K. Three hundred sixteen people attended this ESSCIRC conference, which has a strong focus on integrated circuit design, including sensor interfaces, various analog functions, communication circuits, mixed-signal systems, memories and digital circuit design. The papers were selected following the recommendations of the audience, the chairmen, and the program committee.

The first group of papers deals with sensor interfaces which is the starting point of many signal processing chains. In the first paper, by Huang and Oberle, a passive telemetry IC for biomedical applications is described. This very low power BiCMOS data acquisition system includes an RF-DC converter and voltage regulator. Tuthill describes a temperature sensor in 0.6- μm CMOS technology. The circuit uses switched current and switched capacitor techniques and includes a 10-bit ADC for digital outputs.

The second group consists of two papers dealing with LF analog circuit design. In the paper by Duisters and Dijkmans, a CMOS opamp for audio applications is presented. In this circuit the local supply voltage is boosted to make rail-to-rail input possible. The advantage of this technique is the resulting low distortion level of the opamp in noninverting gain configurations. Den Besten and Nauta describe, in their paper, a fully integrated 5-V-to-3.3-V supply voltage regulator for applications in digital IC's. The circuit requires no external components and special precautions have been taken to allow 5 V in the 3.3-V CMOS process.

The third group of papers deals with analog switched capacitor and continuous-time filters. In the paper by Quinn, a high-accuracy switched capacitor bandpass filter for SECAM TV video applications is described. The recursive bandpass filter is based on a charge redistribution technique and dissipates only 4 mW in 5-V CMOS. Another switched capacitor filter is presented by Vazquez *et al.* This paper focuses on design for testability and the unified on- and off-line testing approach presented is proven to be useful for opamp-based analog circuits in general. Punzenberger and Enz present a paper on an analog continuous-time log-domain filter. The BiCMOS filter can be tuned over three decades, up to 10 MHz, and is power efficient at low supply voltages.

The next three papers deal with oscillators and PLL's. Vaucher and Kasperkovitz present a wide-band tuning system for fully integrated satellite receivers. The wide loop bandwidth of the bipolar circuit enables use of noisy integrated VCO's for reception of satellite digital signals. A two-chip ISM band frequency synthesizer is described by Filiol *et al.* This high-resolution frequency synthesizer is controlled by a fourth-order digital sigma-delta modulator. A compact digital

filter which makes use of sigma-delta quantized tap coefficients is used for GMSK pulse shaping for data transmission. Marie and Belin have presented a single-chip flat panel display controller that features a new clock regenerator architecture. It is fabricated in 1.0- μm BiCMOS.

In the area of RF-analog, two papers are presented. The first one by Cathelin *et al.* presents a low-power voltage-tolerant miniaturized radio receiver to be imbedded in a wristwatch. The circuit decodes the time from as far as 3000 km from the transmitter. The second paper, by Huang *et al.*, describes the effect of technology down-scaling on several RF CMOS functions. Quarter-micron CMOS appears to be the threshold where robust designs can be realized with current consumption competitive to bipolar implementations.

Matching of transistor behavior is critical to the functioning of many analog circuits. The paper by Tenbroek *et al.* is dedicated to this effect in SOI technology where matching properties are strongly influenced by localized internal and coupled heating.

Three circuits for communication, with various approaches and bandwidth but comparable technologies, have been selected from ESSCIRC'97. In the first one, Belot *et al.* have implemented a complete transceiver complying with ATM, SDH/SONET specifications in 3.3-V BiCMOS, featuring automatic power adaptation. The emphasis is put on the advantages of BiCMOS versus CMOS. Casier *et al.* describes an ISDN line driver in 3.3-V CMOS technology. A novel current control circuit is implemented which reduces the variation of the quiescent current and thus facilitates the driver's compensation. Hossack *et al.* present a compander (compressor-expander) for noise reduction in cellular telephone, implemented in 3.0-V CMOS. The use of sigma-delta modulators yields a simple and elegant implementation.

Delta-sigma is also used for an high-speed high-resolution analogue-to-digital converter designed by Marques *et al.* in a low-cost 5-V μm CMOS technology. Yet another analogue interface is presented by Redman-White *et al.* as a front-end for a TV teletext system. The chip includes the front-end and a DSP and is fabricated in a 3.3-V CMOS technology with rail-to-rail circuitry to compensate for the low voltage.

The two next papers are about low-power low-voltage digital signal processing circuits. The first one, by Borgatti *et al.*, extracts features for a remote speech recognition system and is imbedded in a portable appliance. The second one is a FIR filter implemented in standard cells for the read channels of hard-disk. This brief paper concentrates on power, floor plan, and arithmetic problems.

Memories are represented by a brief and three full papers, covering an analogue storage cell, a multilevel storage cell, a dynamic memory cell for large planes, and finally, a static memory cell for low power and speed. Ehler *et al.* address the problem of dense long-term analog storage in standard (no floating gate) CMOS process. For multilevel memories,

Montanari *et al.* describe a simple and efficient level identifying circuit based on shorter distance to current references. The problem of noise in large submicron dynamic RAMS is studied by Kim *et al.* Topological solutions are brought up aimed at compensate or cancel the noises. In GaAs circuits, quiescent current prevents the use of large caches. A low static current memory cell is presented by Bernal and is intended for microprocessors with embedded memory.

Last but not least, there is a full paper on quasi-adiabatic switching for very low power consumption by Mateo and Rubio.

ESSCIRC'97 was an interesting conference on various topics of circuit design. We hope that with this special issue, all who could not attend the conference have access to this selection of excellent papers. The next European Solid-State Circuits Conference (ESSCIRC'98) will be held in The Hague, The Netherlands, September 22–24, 1998.

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Alain Guyot received the Ph.D. degree from the Institute National Polytechnique, Grenoble, France, in 1975.

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Bram Nauta (S'89–M'91) was born in Hengelo, The Netherlands, in 1964. In 1987, he received the M.Sc. degree (*cum laude*) in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies.

In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, The Netherlands, where he worked on high-speed AD converters. From 1994, he led a research group in the same department, working on analog key modules. This included amplifiers, filters, PLL's, voltage regulators, line drivers, reference circuits, substrate interference, etc., mainly in CMOS technology. In 1998 he returned to the University of Twente as Professor heading the Department of IC Design within the Department of Electrical Engineering. He also heads the IC Design Group in the MESA Research Institute. His Ph.D. thesis was published as a book, titled *Analog CMOS Filters for Very High Frequencies* (Boston, MA: Kluwer, 1993). He holds eight patents in circuit design.

Dr. Nauta received the "Shell Study Tour Award" for his Ph.D. work. In 1997, he became Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING.