Photoelectric Effects in $\text{Ta}_2\text{O}_5\text{--SiO}_2\text{--Si}$ Structures

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Abstract

Investigating the behaviour of ISFETs with a $\text{Ta}_2\text{O}_5\text{--SiO}_2$ dielectric it has been observed that their long-term stability is strongly influenced by previous exposures to daylight. A Ta_2O_5 layer, as prepared for ISFET application, will become conductive by exposure to optical radiation. This conduction is due to bulk traps with a depth of 1.6–3.2 eV. It is shown that a low temperature anneal step in the presence of an Al layer on top of the Ta_2O_5 layer may eliminate these traps and reduce the associated threshold voltage instability.

1. Introduction

ISFETs with a $\text{Ta}_2\text{O}_5\text{--SiO}_2$ dielectric often exhibit a worse long-term stability than the reported value of 0.1 mV/day [1]. It has been found that the device characteristics strongly depend on the experimental conditions before and during measurements. The samples under investigation for instance showed a 40 mV threshold voltage shift over a period of 10–15 h, after immersion in a pH solution, preceded by dry storage at laboratory conditions.

A variety of experiments has shown that a phenomenon which disturbs the long-term stability of electrolyte- $\text{Ta}_2\text{O}_5\text{--SiO}_2\text{--Si}$ samples is their sensitivity to light. Therefore the photoelectric effects in these structures have been investigated.

2. Device Fabrication

Different samples have been realized and compared with respect to their drift behaviour, namely MTOS (metal- $\text{Ta}_2\text{O}_5\text{--SiO}_2\text{--Si}$), ETOS (electrolyte- $\text{Ta}_2\text{O}_5\text{--SiO}_2\text{--Si}$), MOS (metal- $\text{SiO}_2\text{--Si}$) and EOS (electrolyte- $\text{SiO}_2\text{--Si}$) structures.

The MTOS devices are n-type FETs in a p-type $\langle 100 \rangle$ 10 Ω cm silicon wafer, and fabricated by means of an NMOS process. After thermal growth of 80 nm gate oxide a shallow ion implantation step is performed for threshold voltage

adjustment to -1 V, followed by a 30 min anneal at 900 °C in dry N_2 . Then 50 nm Ta is deposited by e-gun evaporation with a rate of about 15 nm/min. The Ta layer is patterned and then oxidized at 500 °C in dry O_2 during 200 min, yielding a 100 nm thick Ta_2O_5 layer with a relative dielectric constant of 33. Realizing that the relative dielectric constant of SiO_2 is 3.9, this means that the capacitance per unit area C_i of the Ta_2O_5 layer is $(33/100)/(3.9/80) = 6.8$ times larger than the capacitance C_0 of the SiO_2 layer. Finally a 1 μm thick layer of Al is deposited for metallization, patterned and annealed at 450 °C in dry N_2 during 30 min.

ETOS structures are realized in the same way, except that in that case the Al metal gate is also etched away during the patterning of this layer. MOS and EOS structures are realized in similar ways to the MTOS and ETOS structures. Only the Ta deposition, patterning and oxidation step are in that case omitted.

3. Initial Experimental Results

The samples have been connected to an amplifier of the source-drain follower type. Using such an amplifier, the current from drain to source/bulk and the drain-source voltage are kept constant. A saturated calomel electrode, connected to ground, is used as the reference electrode. The amplifier then adjusts the source voltage to satisfy the predetermined bias conditions. It can be shown that this means that any change δV_t of threshold voltage is accompanied by a change $\delta V_s = -\delta V_t$ of the source voltage. Using this amplifier the pH sensitivity of ETOS samples appeared to be about 56 mV/pH in the whole range pH = 2–12, which is in good agreement with the reported value of 59 mV/pH [1].

To investigate the photoelectric effects in ETOS samples in more detail, first of all the influence of light on the performance of ETOS devices, as connected to the source-drain follower, has been determined. The samples are immersed in a pH buffer solution, which is placed in a dark and

temperature stabilized container. Then they are intermittently exposed to light from a Schott KL1500 cold-light source. The response of the source voltage can be seen from Fig. 1.

Considering this Figure, two different effects seem to be present. When light is switched on a rapid increase of the source voltage can be seen, followed by an exponential change during several minutes. It can also be observed that the polarity of this second change depends on the ISFET bias conditions. Using $V_{ds} = 0.1$ V and $I_{ds} = 0.1$ mA the source voltage increases as shown in curve A, while for $V_{ds} = 1$ V and $I_{ds} = 0.1$ mA the source voltage decreases as shown in curve B. After switching off the light a rapid decrease of the source voltage can be seen, followed by a very slow recovery of the original source voltage.

The rapid increase of the source voltage after switching on the light, and the corresponding decrease after switching it off is mainly caused by the generation of a photocurrent through the reverse-biased drain–bulk diode, and for a smaller part by a change of the threshold voltage due to the generation of electron–hole pairs in the channel.

The other exponential, source voltage shift, is much slower and seems to be due to another bias dependent mechanism in the samples. A change of the bias conditions means a change of the electric field in the insulators. Therefore it can be concluded that this effect depends on the applied electric field during exposure to light.

The validity of this conclusion has been checked by bias–stress experiments, as shown in Fig. 2. Samples are first connected to a drain–source follower. After measuring the source voltage the sample is connected to a stress voltage V_{str} between silicon on one side and reference electrode on the other side. Then the light source is switched on for several minutes. Afterwards the sample is again connected to the drain–source

Fig. 1. Response of the source voltage of ETOS samples to optical radiation as a function of time, as measured by a source–drain follower for different bias conditions. Curve A: $V_{ds} = 0.1$ V and $I_d = 0.1$ mA, curve B: $V_{ds} = 1$ V and $I_d = 0.1$ mA.

Fig. 2. Experimental set-up for bias–stress measurements.

follower. Then within several minutes the applied source voltage is measured again. To avoid dielectric breakdown only positive stress voltages were applied.

In Fig. 3 the source voltage has been plotted as a function of stress voltage V_{str} , related to the value V_s^0 , measured after applying zero stress voltage. It should be noted that source voltage shift and stress voltage are almost linearly related to each other, and that the observed behaviour is reversible.

Performing however the same experiments with EOS samples, no significant source voltage shift has been observed. Several mechanisms may be responsible for the observed behaviour of ETOS samples, namely

- (a) degradation of electron mobility in the silicon
- (b) generation/recombination of SiO_2 –Si interface states
- (c) electrical polarization in the insulators
- (d) charge injection in the insulators

Fig. 3. Measured source voltage of ETOS samples as a function of applied stress voltage, after exposure to optical radiation.

Due to the observed linear relation between source voltage shift and applied stress voltage, as well as the fact that EOS samples do not exhibit such effects as ETOS samples do, it can be concluded that only an effect in the insulator (polarization or charge injection) can be responsible for the observed phenomena.

Realizing that the slope of the curve in Fig. 3 is 0.12, which value corresponds rather well with the ratio $C_0/C_i = 1/6.8$, it can be concluded that the source voltage shift is due to storage and removal of charge at the Ta_2O_5 - SiO_2 interface through a Ta_2O_5 layer, which is (semi)conductive while exposed to optical radiation.

In order to explain this it is assumed that the original threshold voltage, measured after applying zero stress voltage to the sample, corresponds to zero electric field in the Ta_2O_5 and potential V_i and charge Q_i at the Ta_2O_5 - SiO_2 interface. If now a stress voltage V_{str} is applied to the silicon while the Ta_2O_5 layer is conductive due to optical radiation, a current is flowing through it until the electric field in this layer is again zero. The potential at the Ta_2O_5 - SiO_2 interface is then again equal to V_i , but the charge at the Ta_2O_5 - SiO_2 interface has been increased to $Q_i - C_0 \cdot V_{\text{str}}$. Connecting the sample to the source-drain follower, the corresponding shift in the measured source voltage is $-(C_0/C_i) \cdot V_{\text{str}}$.

4. Photoconduction in Ta_2O_5 Layers

Many different methods for the preparation of Ta_2O_5 layers have been considered, and for some of these layers photoconduction has been observed [2-4]. In Al_2O_3 and Si_3N_4 layers similar effects have been observed [5, 6].

It is generally agreed that photoconduction in insulators like Ta_2O_5 , Al_2O_3 and Si_3N_4 is caused by photoionization of initially neutral traps, located between valence band and conduction band, and accompanied injection of electrons in the conduction band. The trap depth may however be different, depending on the preparation method. For Ta_2O_5 samples prepared by different recipes, values from 2.1 to 3.9 eV have been found for the trap depth [2-4]. To investigate whether the presence of these traps and their depth is determined by the fabrication method of the Ta_2O_5 layers only, or also by the presence of a surrounding electrolyte, some other samples have been fabricated and measured.

Of MTOS samples, realized as described in Section 2, the $1\text{ }\mu\text{m}$ thick Al gate was etched, except for a $10\text{ }\mu\text{m}$ wide edge around the gate. Then a 10 nm thick layer of Al, which has a negligible absorption for visible light, was de-

posited on the gate region. These samples have been indicated as M_1TOS samples.

The measured source voltage for these samples is given in Fig. 4. Note the different scale as compared to Fig. 3.

In a second experiment the 10 nm thick Al of the M_1TOS samples was removed by wet etching, yielding again chemical sensitive devices, indicated as ETOS* samples. The pH response of these samples appeared to be 55 mV/pH . However, on performing bias stress experiments with these samples a behaviour was observed that is similar to that of an M_1TOS structure, as drawn in Fig. 4.

Finally it has been determined that for ETOS* and M_1TOS samples the measured source voltage shift is not due to optical radiation, because the same curve as drawn in Fig. 4 has been obtained for bias-stress measurements performed on samples in a dark environment.

Comparing the results of Figs. 3 and 4 it can be concluded that the threshold voltage shift in ETOS samples is about 30 times larger than in ETOS* and M_1TOS samples, and thus is of quite different origin.

The light source radiation is in the visible range, with a photon energy of 1.6 – 3.2 eV . This means that the trap depth in ETOS samples is less than 3.2 eV , and in M_1TOS and ETOS* samples is more than 3.2 eV . Due to the similar behaviour of ETOS* and M_1TOS samples the lower trap depth in ETOS samples is not caused by ions in the contacting electrolyte. Therefore it can be concluded that the trap depth is influenced by the preparation method. As mentioned in Section 2 ETOS samples are realized in almost the same way as MTOS samples. The only difference is that during the Al anneal, the gate region of MTOS samples is covered with Al and the gate region of

Fig. 4. Measured source voltage of M_1TOS samples as a function of applied stress voltage, after exposure to optical radiation.

ETOS samples is not. Due to the fact that ETOS* samples are made by etching the Al gate of originally MTOS samples, the preparation method of ETOS and ETOS* samples is also different.

It seems that the application of a low temperature treatment in N_2 in the presence of an Al layer on top of the Ta_2O_5 can anneal traps with a depth less than about 3.2 eV in this layer. This conclusion is in agreement with the observed dependence of trap depth in a range 2.1–3.9 eV on the preparation method [2–4]. Similar effects have been observed in MOS structures with respect to states at the Si– SiO_2 interface [7], and in Al_2O_3 – SiO_2 ISFETs for the long-term drift [8].

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