Improved Device Performance by Multistep or Carbon Co-Implants

Reinoud Liefting, Rutger C. M. Wijburg, Jonathan S. Custer, Hans Wallinga, *Member, IEEE,* and Frans W. Saris

***Abstract*—High-energy ion implantation is used for forming the collector in vertical bipolar transistors in a BiCMOS process. Secondary defects, remaining after annealing the implant damage, give rise to an increased leakage current and to collector-emitter shorts. These shorts reduce the transistor yield. The use of multiple step implants or the introduction of a C gettering layer are demonstrated to avoid dislocation formation. Experimental results show that these schemes subsequently lower the leakage current and dramatically increase device yield. The presence of C can cause increased collector/substrate leakage, indicating that the C profile needs to be optimized with respect to the doping profiles.**

I. Introduction

HIGH-energy ion implantation is a convenient processing step that offers a high degree of reproducibility. Moreover it enables formation of retrograde n- or p-wells after the high temperature field oxidation step [1], [2]. After the LOCOS step is done, the tub can be implanted in a self-aligned way, which makes the need for area-consuming stopper implants superfluous. Due to a reduced lateral diffusion of the dopants, high-energy ion implantation results in an increased packing density compared with processes using conventional buried layers [3].

Numerous technologies and devices have been realized using high-energy ion implantation. In CMOS processes, the high-energy implanted retrograde well offers a reduced susceptibility to latch-up [4]. In bipolar technology, it can be used to fabricate a pedestal collector to improve the frequency behavior [5] or to simplify processing [3], [6]. Other applications of high-energy ion implantation include the realization of vertically integrated DRAM cells [7] or very fast EEPROM cells using a buried injector [8].

One of the critical problems with high-energy implants is the formation of dislocations during annealing [6], [9], [10]. These dislocations form only if a critical amount of implant damage

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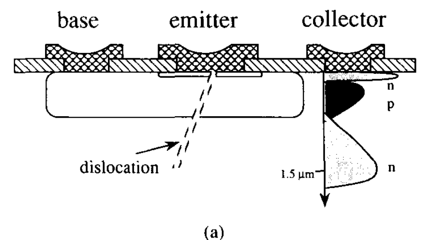
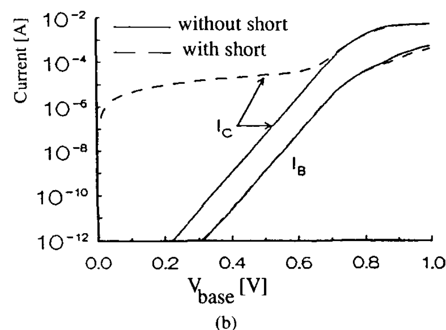


(a)



(b)

Fig. 1. (a) Schematic of a vertical transistor formed by high-energy ion implantation. The collector implant gives rise to dislocation formation during annealing, which can result in collector-emitter shorts. (b) These shorts give rise to excess collector currents, as is illustrated in the Gummel plot.

has been exceeded [11]. This issue applies particularly to the fabrication of collector regions, because the implanted dose must be sufficiently high to obtain a low collector resistance, which gives rise to high damage levels. If the dislocations intersect a junction, an increased leakage current can result. Furthermore, when both the collector/base and the emitter/base junctions are connected via a dislocation, collector-emitter (*c*-*e*) shorts may arise by enhanced diffusion of (emitter) dopants along the dislocations [Fig. 1(a)]. This results in a parasitic resistance behavior in the transistor characteristics, as is shown in the Gummel plot of Fig. 1(b). In general, these *c*- *e* shorts are an important yield problem in bipolar device manufacturing. Although some improvement has been reported by performing extended anneal treatments [6], no structural solution for this problem has been found until now.

Dislocations are not observed if a subcritical amount of damage is generated by a low dose ($1 \times 10^{13} P/\text{cm}^2$) collector implant [11] and no yield problems result [12]. However, a P dose of $\sim 4 \times 10^{13}/\text{cm}^2$ is needed for an acceptable collector resistance [3], but this dose gives rise to dislocation formation [11] and, subsequently, *c*-*e* shorts [12]. In this paper, two

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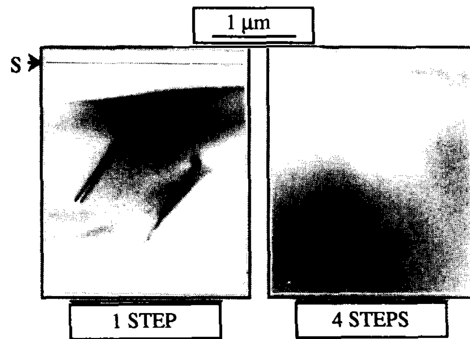

Fig. 2. XTEM analysis of Si implanted with 1 MeV $1.1 \times 10^{14}/\mathrm{cm}^2$ P in one- or four-steps. An anneal at 900°C for 15 min was performed after each implant step.

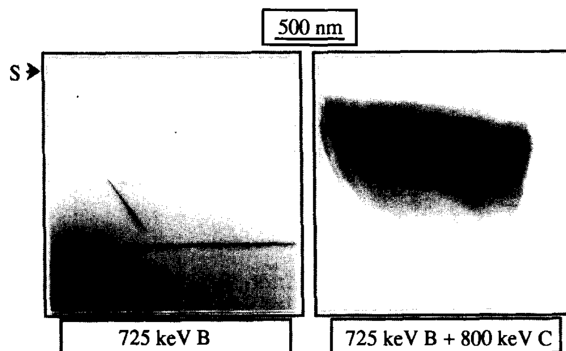

Fig. 3. XTEM analysis of Si implanted with 725 keV $1 \times 10^{14}/\mathrm{cm}^2$ B without and with an extra 800 keV $5 \times 10^{14}/\mathrm{cm}^2$ C implant. An anneal at 900°C for 15 min was performed after the implants.

methods are applied to prevent dislocation formation for the higher P dose. The principle of the two methods is explained in the following. In the first method, an implant is performed in multiple steps. Fig. 2 shows that annealing a $1.1 \times 10^{14}/\mathrm{cm}^2$ 1 MeV P implant gives rise to dislocation formation with a density of $\sim 5 \times 10^8/\mathrm{cm}^2$. However, if this implant is performed in four steps of $2.8 \times 10^{13}/\mathrm{cm}^2$, where each step generates a sub-critical amount of damage and is followed by a 900°C, 15 min anneal, no dislocations are observed [11], [13], [14].

In the second method, C is implanted in the damage region. To demonstrate this method, Fig. 3 shows that annealing a $1 \times 10^{14}/\mathrm{cm}^2$ 725 keV B single implant results in the formation of dislocations, while these dislocations are avoided if a $5 \times 10^{14}/\mathrm{cm}^2$ 800 keV C is also implanted. It is thought that C acts as a sink for Si interstitials, thereby avoiding these interstitials to agglomerate and form dislocations [15]–[17]. This principle has also been shown for the combined 1.5 MeV P and 1.15 MeV C implants used in this work [15].

This paper describes how these two methods are used to avoid dislocation formation for the $4 \times 10^{13} P/\mathrm{cm}^2$ 1.5 MeV collector implant in a BiCMOS process. For the multiple step sequence, $2 \times (2 \times 10^{13} P/\mathrm{cm}^2)$ is implanted, and for the introduction of a C layer, $\sim$1.15 MeV C is implanted to doses of 2 and $5 \times 10^{14}/\mathrm{cm}^2$. Electrical measurements on bipolar devices in which the two methods for avoiding dislocation formation have been applied, are presented.

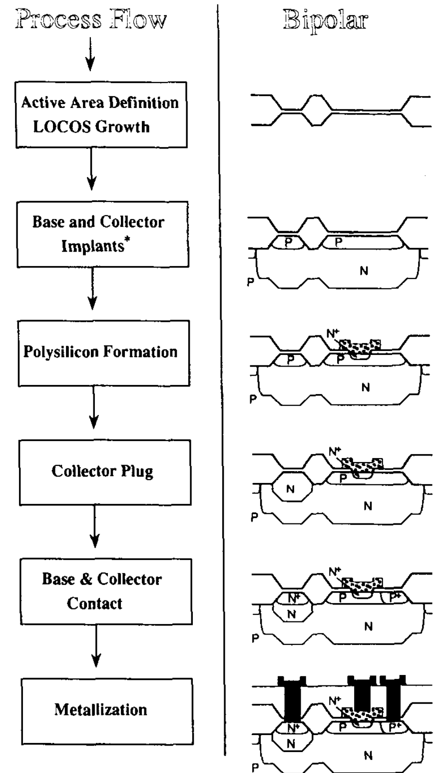

Fig. 4. Process flow for forming the bipolar device structures.

II. Sample Preparation

For the full BiCMOS device fabrication, three wafers (3-in, 20 mΩcm, p-type) with a 4 μm thick epitaxial layer (10 Ωcm, p-type) were used. Fig. 4 summarizes process conditions. After growing the field oxide, the tubs for the CMOS devices were implanted. The collector and base of the bipolar devices were formed after fabrication of the CMOS gates. The base was implanted with $1 \times 10^{13}/\mathrm{cm}^2$ 40 keV B. The collector implant, $4 \times 10^{13}/\mathrm{cm}^2$ 1.5 MeV P, was done aligned to the 0.6 μm LOCOS oxide, while the LOCOS was covered with a resist layer. The collector of wafer 1 was implanted in two steps of $2 \times 10^{13} P/\mathrm{cm}^2$, with each step followed by a 900°C anneal for 15 min in N_2-ambient. For wafers 2 and 3, after a single $4 \times 10^{13} P/\mathrm{cm}^2$ implant, parts of the wafers were co-implanted with 1.15 MeV C to doses of 2 and $5 \times 10^{14}/\mathrm{cm}^2$, respectively. These wafers were subsequently annealed at 900°C for 15 min in N_2-ambient. Table I specifies the collector implant procedures for the three wafers. After annealing, the emitter window was opened in the 25 nm thick screening oxide and a polysilicon emitter was made.

The transistor doping profile co-implanted with $2 \times 10^{14} C/\mathrm{cm}^2$, as simulated with SUPREM III, is presented in Fig. 5. The measured projected range of the C implant is

TABLE I
IMPLANTS FOR COLLECTOR REGION

	Wafer 1	Wafer 2	Wafer 3
collector implant	$2 \times (2 \times 10^{13}\,P/\mathrm{cm}^2)$	$4 \times 10^{13}\,P/\mathrm{cm}^2$	$4 \times 10^{13}\,P/\mathrm{cm}^2$
Carbon co-implant (part of the wafer)	—	$2 \times 10^{14}\,C/\mathrm{cm}^2$	$5 \times 10^{14}\,C/\mathrm{cm}^2$
anneal	2 × (900°C/15 min)	900°C/15 min	900°C/15 min

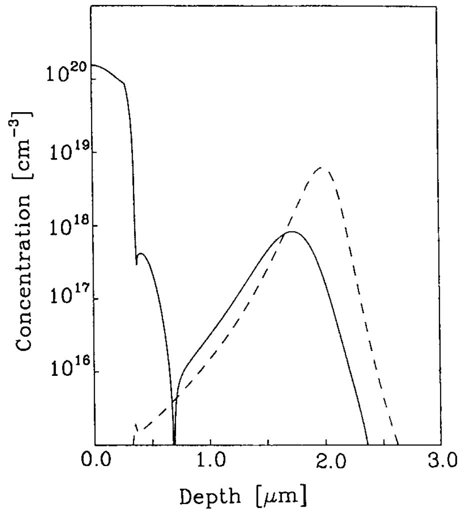

Fig. 5. Doping profile (drawn line) of bipolar transistor co-implanted with $2 \times 10^{14}\,C/\mathrm{cm}^2$ (broken line), as simulated with SUPREM III.

0.2 μm deeper than the P implant, which has been shown to be most effective for suppression of dislocation formation for the 1.5 MeV P implant [15].

III. ELECTRICAL MEASUREMENTS

Bipolar device measurements were performed on transistors of wafers 2 and 3 which were made by the standard process (no C implanted). Some of the Gummel plots for these "standard" transistors showed excessive collector current densities at low base-emitter voltages (Fig. 6). This is attributed to the presence of c-e shorts. The yield of these standard transistors as a function of emitter area is presented in Fig. 7. For cells with an emitter area of $10^4\,\mu\mathrm{m}^2$, 65% of the emitters are shorted, decreasing to 20% for an area of 1200 $\mu\mathrm{m}^2$. The larger the area, the higher the probability that at least one dislocation crosses both the base/emitter and collector/base junction. In a first order approximation, the yield is an exponential function of the emitter area, with a "fatal" defect density per unit area of $1.25 \times 10^4/\mathrm{cm}^2$ [18]. This density of defects is in agreement with results found earlier for MeV implanted collector regions, where the dislocation density near the surface was investigated with a Secco-type defect etch [6], [9]. Hence, the c-e shorts are likely caused by dislocations running from the collector to the surface region. However, the "fatal" defect density of $1.25 \times 10^4/\mathrm{cm}^2$ is more than four orders of magnitude smaller than dislocation densities observed for medium dose MeV P implants (see, e.g., Fig. 2). Hence, only one out of 10^4

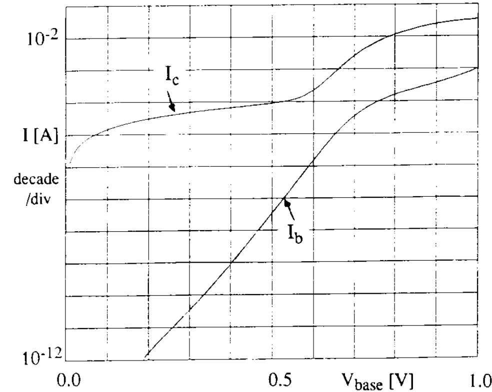

Fig. 6. Gummel plot of transistor with standard collector ($10^4\,\mu\mathrm{m}^2$ emitter). The excessive collector current at low base-emitter voltages is attributed to the presence of c-e shorts.

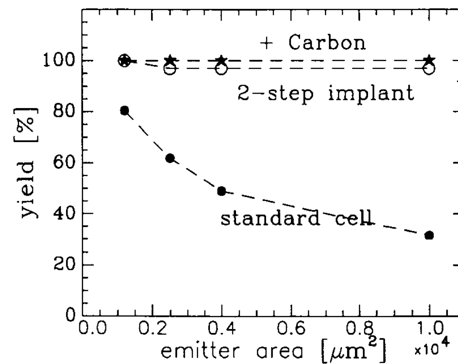

Fig. 7. Yield of bipolar transistors with standard, two-step implanted and C co-implanted collectors, as a function of emitter area.

dislocations is fatal, in agreement with results obtained for keV-implanted bipolar transistors [19].

Electrical measurements were also performed on transistors with two-step implanted collectors and on transistors with C co-implanted collectors. The yield of these transistors as a function of emitter area is presented in Fig. 7. For the multistep implants, only 3% of the transistors with large emitter areas showed the presence of shorts. The smallest emitters ($1200\,\mu\mathrm{m}^2$) exhibited no shorts at all. Thus an enormous improvement in yield is obtained compared to the results for the standard bipolar transistors. For the collectors co-implanted with C, the results were even better. There, none of the transistors showed the excess collector current behavior, independent of emitter area or C-dose (Fig. 7). A typical example of a Gummel plot, where shorts were avoided by either the two-step implant or the C co-implant, is presented in Fig. 8. The transistor exhibited good characteristics over more than eight decades with a common emitter current gain (h_{fe}) of ≈ 80.

In addition to fatal shorts, dislocations can also affect junction characteristics such as leakage currents. An ideal defect-free diode has reverse I–V characteristics which can be fitted with a power law $I \propto V^n$ with $n \approx 0.5$ [18]–[20]. For

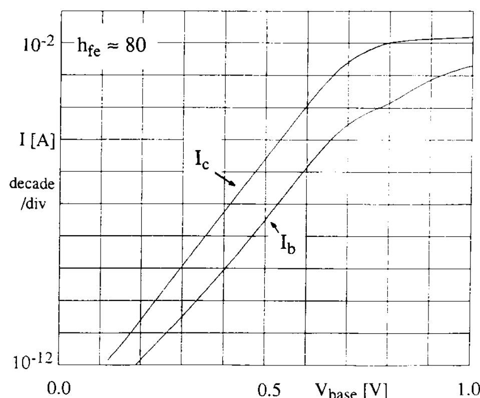

Fig. 8. Gummel plot of transistors with two-step implanted or C co-implanted collector ($10^4\,\mu m^2$ emitter).

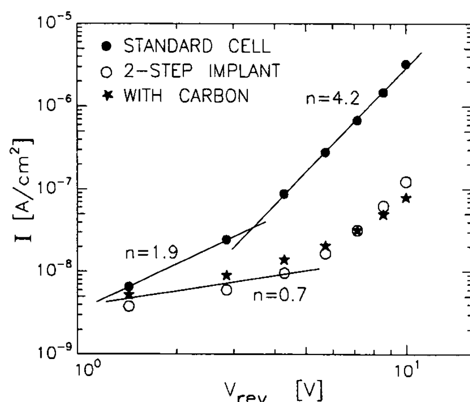

Fig. 9. Reverse I–V characteristics of the collector/base junction. $I \propto V^n$, where $n \approx 0.5$ for an ideal junction and $2 < n < 4$ for a junction containing dislocations.

the I–V characteristics of the standard separate collector/base diodes (no emitter formed), n was ~1.9 for lower and ~4.2 for higher voltages (Fig. 9). This is normally observed for junctions containing dislocations [19]–[21]. (The dislocations in the depletion region establish efficient breakdown regions, which give rise to the higher voltage dependence [19].) In contrast, for both the two-step and C co-implanted diodes, the leakage current densities are one order of magnitude lower at 5 V reverse bias. However, n is only ~0.7 even for lower voltages, indicating an improved, but still not ideal leakage behavior. There are several possible explanations for this non-ideal behavior, including Zener breakdown [19]. In addition, the two-step implanted diodes have undergone an additional mask/implant/anneal sequence, which could adversely affect device performance.

Although the reverse I–V characteristics of the collector/base junction in the C co-implanted transistors are acceptable, it is known that C-related defects can lead to increased leakage currents [22]. Because the C-profile overlaps the P implant, there will be C-related defects in the collector region, primarily near the collector/substrate junction, see Fig. 4. This may influence the collector sheet resistivity

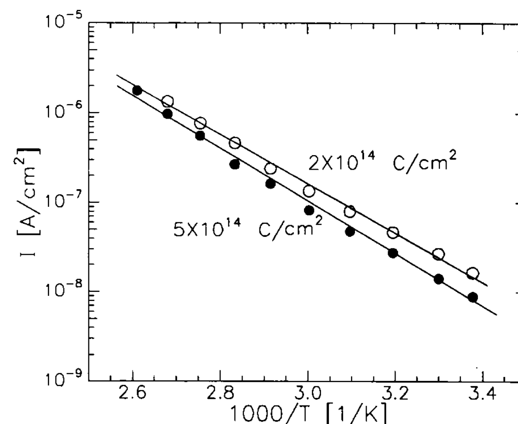

Fig. 10. Leakage current density as a function of $1/T$ for collector/base junctions implanted with 1.15 MeV C, measured at reverse bias of 2.85 V. Activation energies between 0.55 and 0.60 eV are extracted (drawn lines).

and the leakage currents of the collector/base as well as the collector/substrate junction. The sheet resistivity of the standard collector is $356\,\Omega/\Box$, while higher values of 544 and $630\,\Omega/\Box$ are measured for the 2 and $5\times10^{14}/\mathrm{cm}^2$ C implanted structures, respectively. The C-related defects probably lower the mobility of the carriers, increasing the resistivity of the collector. No changes in sheet resistivity of the base were observed.

The C-related defects may also introduce states in the bandgap which enhance carrier generation/recombination. The position of these states can be determined by temperature dependent leakage current measurements [22], shown in Fig. 10 for C implanted diodes. The leakage in the C-implanted collector/base junctions increases with temperature and can be fitted with an activation energy between 0.55 and 0.60 eV for both C doses. This activation energy indicates that deep traps in the depletion region are generated by the implants. Such deep traps have been observed for MeV C implanted silicon [22], although activation energies of ~0.6 eV also have been found for junctions containing dislocations [19]. The lowest leakage is observed for the highest C dose, which is attributed to the stronger gettering of point defects and impurities from the depletion region. The leakage current density at 25°C is only $\sim 10\,\mathrm{nA/cm^2}$, which is a good result.

Fig. 11 shows the temperature dependent leakage current density of the collector/substrate junction for C implanted diodes. The current density here is on the order of 100 mA/cm^2, seven orders of magnitude higher than for the collector/base junction. This is attributed to the high concentration of C-related defects positioned near the collector/substrate junction. A small decrease in leakage current density for increasing measuring temperature is observed, see also Wang *et al.* [23].

IV. Discussion and Conclusions

High-energy ion implantation was used for creating the collector in vertical bipolar transistors, but dislocations formed during annealing and severely influenced device performance.

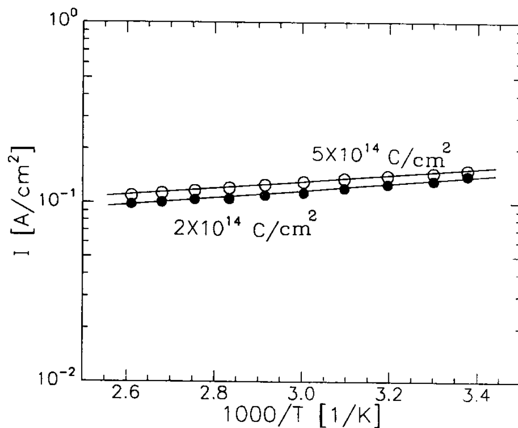

Fig. 11. Leakage current density as a function of $1/T$ for collector/substrate junctions implanted with 1.15 MeV C, measured at reverse bias of 2.85 V. Leakage is decreasing for increasing temperature.

The collector/base junction showed an increase in leakage current when the junction was intersected by dislocations. If the base/emitter and collector/base junctions were intersected, c- e shorts arose probably as a result of enhanced diffusion of the emitter dopant along a dislocation. These shorts reduced the yield of transistors with a $10^4\,\mu\mathrm{m}^2$ emitter area to less than 35%. For thinner base widths than used in this work, the number of dislocations in standard devices which would run from the emitter to the collector should increase, causing an even lower yield. Therefore, dislocation engineering by multistep or C co-implants would be even more important.

Two methods were applied in this paper to suppress dislocation formation for the collector implant. In the first scheme, the collector was formed in two implant and anneal steps, and in the second scheme, extra carbon to doses of 2 and $5 \times 10^{14}/\mathrm{cm}^2$ was implanted in the collector region prior to annealing. For both methods, dislocation formation was avoided and the leakage current in the collector/base junction decreased. Also, for the transistors with two-step implanted collectors, only one out of 30 transistors showed an excessive collector current at low base-emitter voltage. For the C co-implanted collectors, none of the transistors were shorted. However, for the C implanted junctions, C -related defects introduced deep traps in the bandgap which gave rise to an increase in leakage current especially at the collector/substrate junction, because the concentration of defects is highest near this junction.

The optimum collector dose is $\sim 4 \times 10^{13} P/\mathrm{cm}^2$ [3]. For the multistep method, only two-steps are needed in total for implanting this dose. This means that only one additional series of masking/implant/anneal steps has to be performed. The extra masking step is necessary since the LOCOS oxide is not thick enough to stop the P ions. If doses much higher than $4 \times 10^{13} P/\mathrm{cm}^2$ are required, the multi step procedure would involve too many extra implant and anneal steps.

Dislocation formation for P doses as high as $1 \times 10^{15}/\mathrm{cm}^2$ can be avoided by co-implanting C [15]. In this case, only one extra implant step has to be carried out. The C layer is known to efficiently getter point defects and metallic impurities from the near surface region, thereby improving the quality of the active regions of the device [17], [22]–[25]. However, the C-related defects should not influence the leakage of either of the junctions too much. This may be reached by lowering the C dose to the minimum value needed for suppressing dislocation formation for the P implant. Also, the C can be implanted at a somewhat lower energy such that it is positioned in between the collector/base and the collector/substrate junctions, or at a much higher energy so that it is below the collector/substrate junction. However, it should be investigated if dislocation formation is then still avoided.

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References

[1] R. D. Rung, C. J. Dell'Oca, and L. G. Walker, "A retrograde p-well for higher density CMOS," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 1115–1119, 1981.

[2] J. Y. Chen, "Quadruple-well CMOS for VLSI technology," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 910–919, 1984.

[3] R. C. M. Wijburg, G. J. Hemink, J. Middelhoek, and H. Wallinga, "A high-energy ion implanted BiCMOS process with compatible EPROM structures," in *Proc. ESSDERC*, 1990, pp. 515–519.

[4] F. S. Lai, L. K. Wang, Y. Taur, J. Y. Sun, K. E. Petrillo, S. K. Chicotka, E. J. Petrillo, M. R. Polcari, T. J. Bucelot, and D. S. Zicherman, "A highly latchup-immune 1-μm CMOS technology fabricated with 1-MeV ion implantation and self-aligned TiSi2," *IEEE Trans. Electron Devices*, vol. ED-33, p. 1308, 1986.

[5] J. F. Ziegler, B. L. Crowder, and W. J. Kleinfelder, "Experimental evaluation of high-energy ion implantation for possible fabrication of a transistor pedestal collector," *IBM J. Res. Dev.*, vol. 15, pp. 452–456, 1971.

[6] H. J. Böhm, L. Bernewitz, W. R. Böhm, and R. Köpl, "Megaelectronvolt phosphorous implantation for bipolar devices," *IEEE Trans. Electron Devices*, vol. 35, pp. 1616–1619, 1988.

[7] A. Mouthaan and M. Vertregt, "A vertically integrated dynamic RAM-cell: buried bit line memory with floating transfer layer," *Solid State Electron.*, vol. 29, pp. 1289–1294, 1986.

[8] R. C. M. Wijburg, G. J. Hemink, J. Middelhoek, H. Wallinga, and A. Mouthaan, "VIPMOS: A novel buried injector structure for EPROM applications," *IEEE Trans. Electron Devices*, vol. 38, pp. 111–120, 1991.

[9] M. Takahashi, S. Konaka, and A. Kajiyama, "MeV-energy As^+ implantation into Si: Extended-defect reduction and planar n-p-n transistor fabrication," *J. Appl. Phys.*, vol. 54, pp. 6041–6043, 1983.

[10] M. Tamura, "Damage formation and annealing of ion implantation in Si," *Mat. Sci. Rep.*, vol. 6, pp. 141–214, 1991.

[11] R. J. Schreutelkamp, J. S. Custer, J. R. Liefting, W. X. Lu, and F. W. Saris, "Preamorphization damage in ion implanted silicon," *Mat. Sci. Rep.*, vol. 6, pp. 275–366, 1991.

[12] F. W. Ragay, "High-energy ion implantation for bipolar transistor fabrication," Ph.D. dissertation, University of Twente, The Netherlands, 1991.

[13] J. R. Liefting, V. Raineri, J. S. Custer, R. J. Schreutelkamp, and F. W. Saris, "Avoiding dislocation formation for B, P, and As implants," *Mat. Res. Soc. Symp. Proc.*, vol. 235, in press.

[14] R. J. Schreutelkamp, J. R. Liefting, J. S. Custer, and F. W. Saris, "Avoiding preamorphization damage for high mass implants," *Appl. Phys. Lett.*, 58, pp. 2827–2829, 1991.

[15] M. Tamura, T. Ando, and K. Ohyu, "MeV-ion-induced damage in Si and its annealing," *Nucl. Instr. Meth. B.*, vol. 59/60, pp. 572–583, 1991.

[16] J. R. Liefting, J. S. Custer, R. J. Schreutelkamp, and F. W. Saris, "*C* implanation for suppression of dislocation formation," *Mat. Res. Soc. Symp. Proc.*, vol. 235, in press.

[17] H. Wong, J. Lou, N. W. Cheung, E. P. Kvam, K. M. Yu, D. A. Olson, and J. Washburn, "Cross-section transmission electron microscopy study of carbon-implanted layers in silicon," *Appl. Phys. Lett.*, vol. 57, pp. 798–800, 1989.

[18] S. M. Sze, *Semiconductor Devices: Physics and Technology.* New York: Wiley, 1985.
[19] P. Ashburn, C. Bull, K. H. Nicholas, and G. R. Booker, "Effects of dislocations in silicon transistors with implanted bases," *Solid State Electron.*, vol. 20, pp. 731–740, 1977.
[20] K. V. Ravi, *Imperfections and Impurities in Semiconductor Silicon.* New York: Wiley, 1981.
[21] C. Bull, P. Ashburn, G. R. Booker, and K. H. Nicholas, "Effects of dislocations in silicon transistors with implanted emitters," *Solid State Electron.*, vol. 22, pp. 95–104, 1979.
[22] H. Wong, N. W. Cheung, and S. S. Wong, "Electronic defects in silicon induced by MeV carbon and oxygen implantations," *Nucl. Instr. Meth.*, vol. B37/38, pp. 970–974, 1989.
[23] A. C. M. Wang and S. Kakihana, "Leakage and hfe degradation in microwave bipolar transistors," *IEEE Trans. Electron Devices*, vol. ED-21, pp. 667–674, 1974.
[24] W. Skorupa, R. Kögler, K. Schmalz, and H. Bartsch, "Proximity gettering by MeV-implantation of carbon: microstructure and carrier lifetime measurements," *Nucl. Instr. Meth.*, vol. B55, p. 224, 1991.
[25] K. Tsukamoto, S. Komori, T. Kuroi, and Y. Akasaka, "High-energy ion implantation for ULSI," *Nucl. Instr. Meth.*, vol. B59/60, p. 584, 1991.

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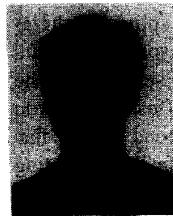

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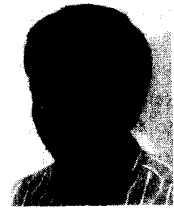

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