Embedded 5 V-to-3.3 V Voltage Regulator for Supplying Digital IC's in 3.3 V CMOS Technology

Gerrit W. den Besten and Bram Nauta, *Member, IEEE*

***Abstract*—A fully integrated 5 V-to-3.3 V supply voltage regulator for application in digital IC's has been designed in a 3.3 V 0.5 μm CMOS process. The regulator is able to deliver peak current transients of 300 mA, while the output voltage remains within a margin of 10% around the nominal value. The circuit draws a static quiescent current of 750 μA during normal operation, and includes a power-down mode with only 10 μA current consumption. The die area is 1 mm^2, and can be scaled proportional to the maximum peak current. Special precautions have been taken to allow 5 V in the 3.3 V process.**

***Index Terms*—CMOS integrated circuits, digital supply, fully integrated solution, low drop, power-down, replica control, series regulator, supply voltage compatibility.**

I. Introduction

In the recent past, many digital IC's were fabricated in CMOS technology with 5 V supply voltage. This has led to a large number of systems with a 5 V supply on the PCB's. Meanwhile, CMOS technology has developed further, and the maximal allowable supply voltage of the digital IC's has dropped to 3.3 V for 0.5 and 0.35 μm technologies, and will drop to even lower values in the newer technologies. Since IC manufacturers want to use modern CMOS processes for cost reduction, a supply voltage compatibility problem results.

An intermediate solution is an integrated supply voltage regulator in the low voltage IC, which converts the external 5 V to an internal 3.3 V. If, in this case, the IO signals of the IC are kept at the 5 V level, and if the integrated regulator does not require extra pins, the PCB designer can use the IC as if it were a classical 5 V product. The extra chip area needed for the regulator pays off against the increased packing density of the modern technology that can be used.

Fig. 1 shows the circuitry needed to allow 5 V operation in 3.3 V technology. The external 5 V (V_{DDD}) is connected to the integrated supply voltage regulator and the I/O cells. The digital core operates at 3.3 V generated by the regulator. The I/O cells convert the 3.3 V logic swing to 5 V swing *and vice versa*. For being compatible with existing 5 V IC's, there is not always an IC pin available for external decoupling of the internal 3.3 V supply. Therefore, the regulator itself must be able to deliver a stable and accurate internal supply voltage, without using an external capacitor. This is difficult to realize since the digital core circuitry draws large and steep supply current peaks. Both the external 5 V and internal 3.3 V supply voltages have the normal $\pm$10% tolerance.

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The authors are with Philips Research Laboratories Eindhoven, 5656 AA, The Netherlands.

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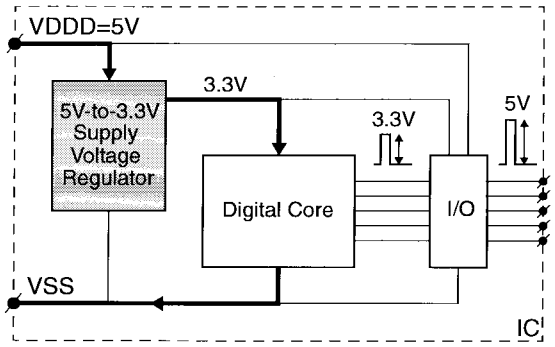


Fig. 1. Typical IC application of the regulator.

Since the supply voltage regulator needs to be fully integrated, no high-efficient dc–dc converters which need external inductors and/or capacitors can be used. This regulator must therefore be of the series regulator type, so it will be dissipating power. This does not have to be a problem since the old 5 V technology IC would also have had a larger power dissipation due to the larger internal voltage swings and parasitic capacitors. The total power dissipation of a 3.3 V core plus supply voltage regulator is less than the same function in 5 V technology. The external supply voltage is the same while the current is reduced.

As a transition of the PCB to 3.3 V supply voltage operation is expected, the integrated regulator must be designed in such a way that the external supply voltage can be anywhere in the range of 3.3–5 V. The PCB designer can use the same IC for a 5 V as well as for a 3.3 V system. This allows a smooth transition from 5 to 3.3 V.

Summarizing, the regulator to be designed must be fully integrated, being able to deliver steep current transients and having an absolute accuracy of $\pm$10%. Also, the external V_{DDD} must be anywhere in the 3.3–5 V range, and the circuit must be small and have a small standby current. In addition, the circuit must have a power-down mode in which the current consumption is reduced to several microamperes.

A. Existing Techniques

Previously published embedded regulator circuits were found to be less suited for this application. These circuits, mostly designed for voltage reduction in RAM IC's, can be divided into three types, each with its specific problems. The basic diagrams of these types are shown in Fig. 2.

Fig. 2(a) [1]–[3] shows the first type where the output device is a PMOS transistor. The output is current driven. The gate

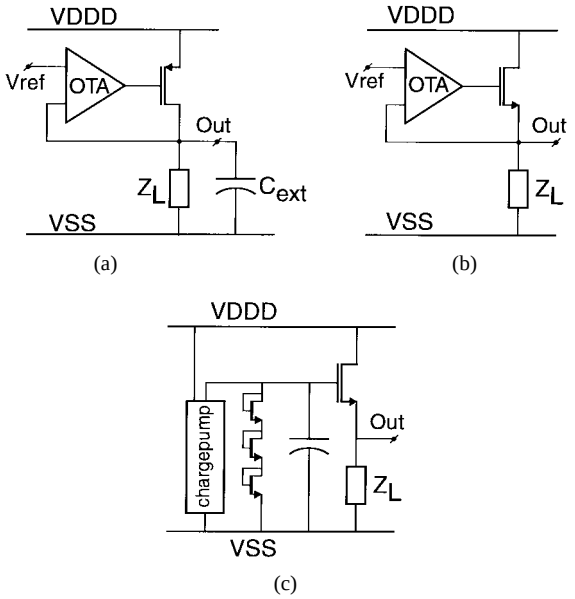


Fig. 2. Conventional regulator structures: (a) PMOS with OTA feedback [1]–[3], (b) NMOS with OTA feedback [3], [4], and (c) NMOS with charge-pump control [5].

of the PMOS is controlled by a feedback loop with OTA. The output impedance will increase with frequency due to the roll-off of the control loop gain. This makes a large (external) capacitor C_{ext} necessary to enforce a low output impedance for high frequencies. The control loop is at least second order due to another pole at the PMOS gate besides the badly defined pole at the output of the regulator. Therefore, the loop generally suffers from stability problems.

Fig. 2(b) shows the second type [3], [4] with an NMOS output device instead of a PMOS. This circuit has fewer stability problems, and does not require a large output capacitor due to the inherently low-ohmic output impedance of the source-follower structure. The disadvantage of this type is that the output voltage is at least one gate–source voltage below the external supply voltage, which implies that it cannot have a low dropout voltage.

The third type in Fig. 2(c) [5] does not have a feedback loop. The gate of the NMOS output device is driven by a charge pump, and its voltage is determined by a simple reference. The gate voltage can exceed the supply, and therefore this type of regulator can have a low dropout voltage. However, the resulting output voltage is rather inaccurate. Furthermore, high voltages easily appear in the charge pump which operates at V_{DDD}, resulting in possible reliability problems.

The fully integrated series regulator described in this paper can operate at supply voltages up to 5.5 V, and overcomes the above-described problems. The next section will describe the circuit. Then, some experimental results are discussed, and some conclusions are given.

II. New Regulator

Fig. 3(a) shows the basic diagram of the regulator. It consists of an NMOS $M1$ in a source-follower configuration, a gate decoupling capacitor $C1$, a bias resistor $R1$, and a control part. The control part behaves like a charge pump, and slowly

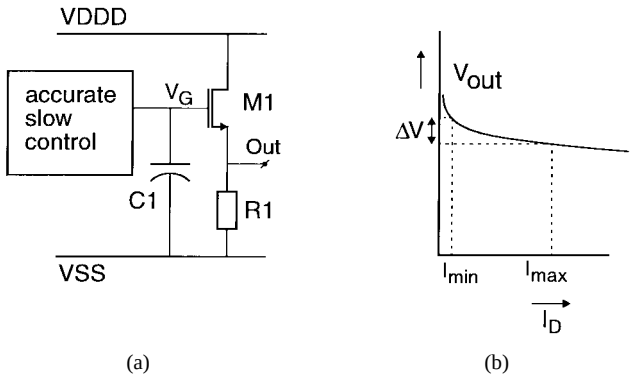


Fig. 3. NMOS output stage.

controls the charge on $C1$. This circuit is described in the next sections. In order to understand the method of control of the gate, first the operation of such an output stage is discussed.

A. Output Stage

The output structure of Fig. 3(a) is chosen because it implies an inherently low output impedance for all frequencies. It also ensures a good PSRR because the NMOS behaves like a cascode device for the internal supply. The large capacitor $C1$ is necessary to reduce the capacitive coupling from the output to the gate voltage V_G at higher frequencies through the gate–source capacitance of output transistor $M1$. The slow but accurate control drives the gate to the right dc voltage. Fast control has no relevance here because load current variations will always be faster than a control loop could handle. For this reason, the output voltage varies slightly with the load current. Actually, the voltage is tracing a part of the transistor I_d–V_{gs} characteristic as shown in Fig. 3(b). If the drain current of $M1$ increases from $I_{\min}$ to $I_{\max}$, the output voltage drops with a voltage equal to ΔV.

The demand on the accuracy of the output voltage of the regulator is $\pm 10\%$, i.e., ± 300 mV $= 600$ mV. The actual accuracy is determined by two parts: 1) the accuracy of the control part, and 2) the output voltage variation due to output current variation. Here, the accuracy demands are split as follows: maximal 200 mV for the control part and maximal 400 mV for the signal-dependent part, under worst case conditions. The latter 400 mV is the sum of the V_{gs} variation of $M1$ (determined by the W/L ratio of $M1$), and the V_G variation due to the coupling from output voltage through C_{gs} of $M1$.

The circuit part consisting of $C1$ and $M1$ consumes most of the die area of the complete voltage regulator. One can either spend a lot of area on $C1$ or on $M1$. If $C1$ is made very large, then the ripple on V_G will be small; the V_{gs} variation may then be 400 mV, and $M1$ need not to be too large. On the other hand, if $C1$ is made small, then the V_G variation will be large. This means that there is less left for V_{gs} variation, and thus $M1$ becomes large. The optimization has been done numerically, which led to an optimal ratio between capacitor and transistor area.

For 200 μA bias current $(I_{\min})$, 100 mA peak load current $(I_{\max})$, and 400 mV dynamic voltage variation at 140°C, this

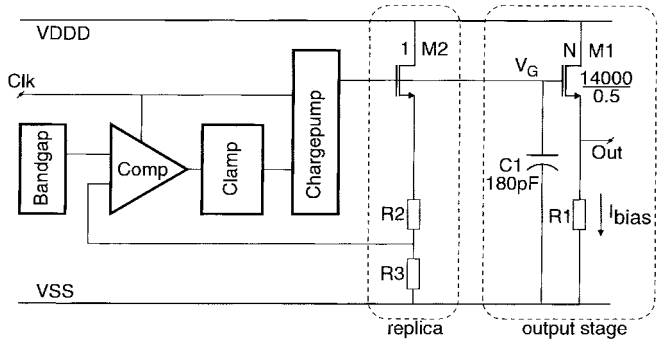


Fig. 4. Basic regulator diagram.

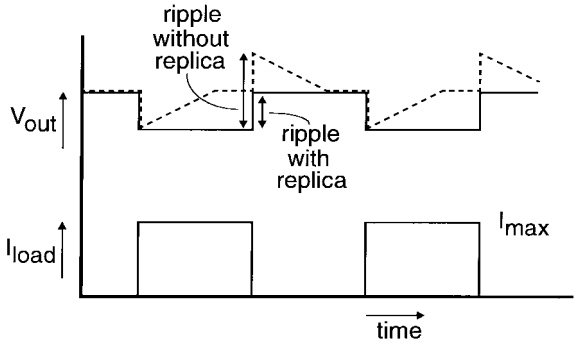


Fig. 5. Influence of replica feedback. With replica, the ripple in $V_{\rm out}$ is reduced by a factor 2.

results in a W/L of 14 000 μm/0.5 μm for the NMOS and 180 pF for $C1$, which is implemented in gate oxide. Although there is a high voltage (maximum 4.5 V) across the oxide, this was allowed in the 3.3 V process because the drain–source voltage of the transistor used to implement $C1$ equals zero, and the dimensions are well above process minimum, so no hot electrons will appear. Transistor $M1$ has minimum L, and is biased close to weak inversion for maximizing g_m/I, which implies a small voltage variation for quite a large current ratio. The typical large-signal output resistance for these dimensions is about 3 Ω.

The circuit has been designed to handle the maximum specified peak load currents. Peak load currents in digital circuits can be much larger than the average current. The ratio depends a.o. on clock frequency and the presence of internal decoupling of the 3.3 V supplies. Decoupling the internal 3.3 V is advantageous for reducing EM radiation of the IC, and for reducing substrate bounce. Also, the area needed for the supply voltage regulator will be smaller in that case. The stability of the regulator is independent of the internal supply decoupling.

Absolute values of $M1$ and $C1$ depend on the peak load current to be expected. If N times more current is needed, $C1$ and $M1$ become a factor N larger. Since the area of the regulator is dominated by $M1$ and $C1$, its area is proportional to the expected peak load current.

B. Regulator Circuit

Fig. 4 shows a 100 mA output stage in combination with the implementation of the accurate gate control loop. The required gate voltage V_G for the output stage can be larger than V_{DDD}, especially when V_{DDD} becomes smaller than 4.5 V. Therefore, this gate must be driven by a charge pump. High stress voltages in this charge pump—which is a capacitive voltage doubler—can be avoided if its input (supply) voltage is kept about a factor 2 lower than its output voltage.

This concept of a charge pump driving the gate has the advantage that, due to the fact that the input of the charge pump is at a much lower voltage level, the rest of the regulator circuitry can operate at a lower, process-tolerated voltage. This lower internal voltage has to be generated from the external V_{DDD}, and is chosen to be 3.3 V. It can easily be generated by making a copy of the regulator output voltage with an extra NMOS transistor with the gate connected to V_G. A special start-up circuit is required for precharging V_G in order to initialize circuit operation.

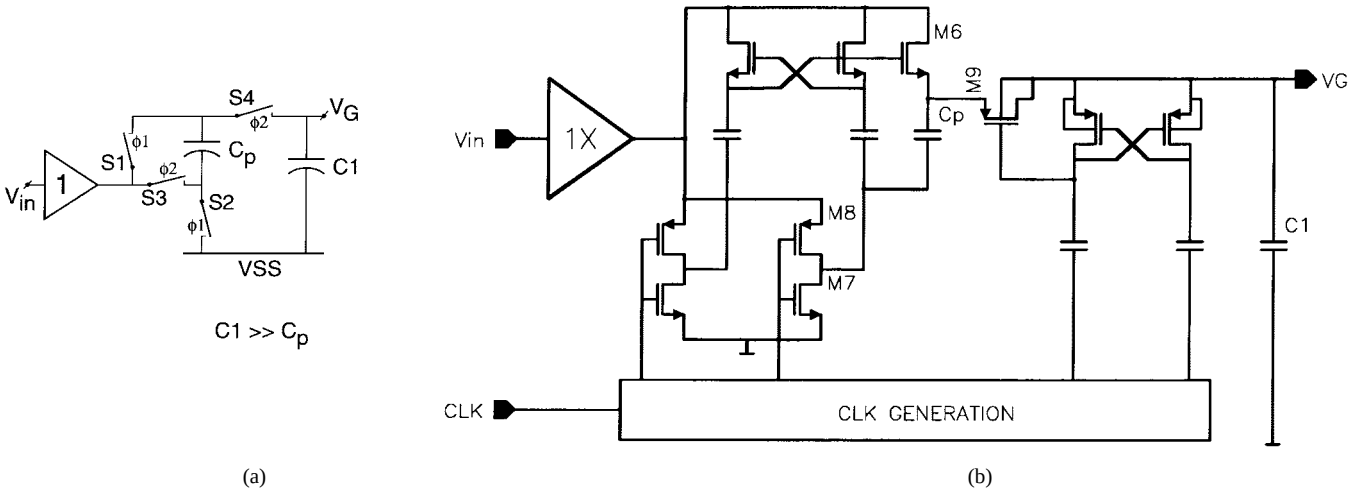
The control loop consists of a bandgap reference, a comparator, a clamp circuit, a charge pump, and a replica circuit for feedback as also shown in Fig. 4. An on-chip free-running oscillator delivers the required clock signal. A bandgap reference is necessary to obtain the required static accuracy. The operation of the control loop can be understood as follows. The resistive division in the replica branch ($M2$, $R2$, $R3$) scales down the nominal copy of the output voltage. The resulting feedback voltage equals the bandgap reference voltage of 1.21 V if and only if the nominal regulator output voltage is correct. The comparator can decide, from the input signals, whether the gate voltage must increase or decrease, which is done via the clamp circuit with the bidirectional charge pump. The clamp circuit generates the input voltage for the charge pump. The charge pump acts as a voltage doubler, and its input voltage is somewhat higher or somewhat lower than half the gate voltage V_G.

Thanks to the charge-pump approach, this regulator with source-follower output has a low dropout voltage of only a few hundred millivolts. V_{DDD} can have any value between 5.5 V and just above 3.3 V for correct output voltages. V_{DDD} can even be lower than 3.3 V, although the output voltage will always be slightly lower than V_{DDD}.

C. Replica Feedback

Instead of sensing the output voltage directly, a replica branch is used for feedback which guarantees stability independent of the load. This is an advantage since the exact load is not known. The influence of process variations and temperature at dc settings is cancelled due to the matched structure of the replica. In the layout, the replica transistor is located at the center of the output power transistor array. Matching—including thermal effects—is now optimal.

The replica ensures that the output is controlled toward the correct nominal dc setting, and implies that the loop is not influenced by load current variations. This is illustrated in Fig. 5. For the given load current pattern, the ripple with direct feedback is twice as much as for the implementation with replica. Without replica, it would be impossible to achieve $\pm$10% output accuracy together with an acceptable quiescent



(a) (b)

Fig. 6. (a) Charge pump for gate control and (b) transistor diagram of charge pump.

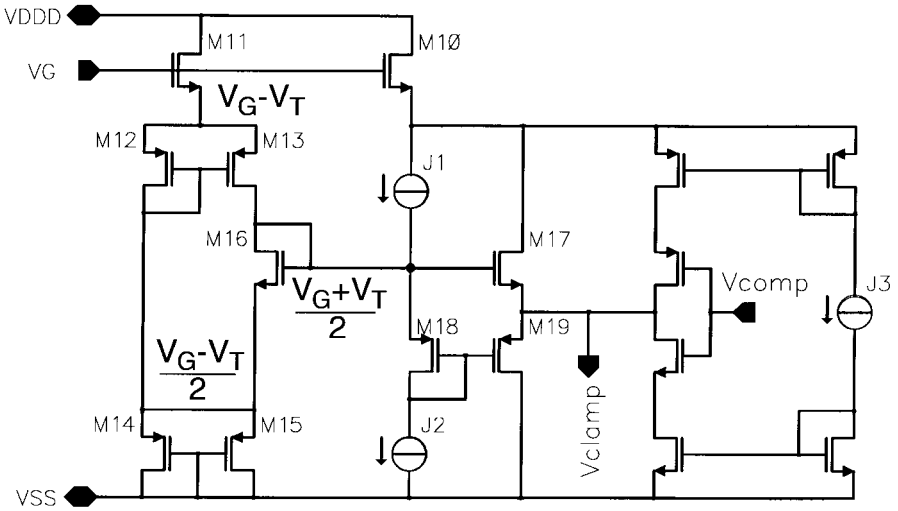


Fig. 7. Clamp circuit. The input voltage $V_{\rm comp}$ has a large swing, while the output voltage $V_{\rm clamp}$ has a defined swing: approximately $V_T/2$ higher or lower than $V_G/2$.

current, due to the limited achievable g_m/I of the output stage transistor.

D. Charge Pump

The operation of the bidirectional charge pump [6] circuit can be explained by using a basic capacitive voltage doubler circuit as shown in Fig. 6(a). A voltage buffer in front of it ensures that the preceding clamp circuit is not loaded. The decoupling capacitor $C1$ of the output stage is much larger than pumping capacitor C_p. Two nonoverlapping clocks ϕ_1 and ϕ_2 are driving the switches. During clock phase 1, the input voltage $V_{\rm in}$ is put on capacitor C_p. During clock phase 2, capacitor C_p is charged or discharged until the voltage across C_p is $V_G - V_{\rm in}$, which means that a charge transport of $(V_G - 2^*V_{\rm in})^*C_p$ has taken place from or to buffer capacitor $C1$. For an input voltage $V_{\rm in}$ of $V_G/2$, the charge pump is in equilibrium, and does not transport any charge.

Because the charge pump is connected to the high gate voltage, stress easily occurs in this circuit. Safe operation has been guaranteed by keeping the input voltage close to $V_G/2$. This is realized by the clamp circuit which generates a voltage $V_G/2 \pm V_T/2$. This voltage clamping implies that the charge pump transfers well-defined charge packages of $Q = C_p{}^*V_T$ to or from buffer capacitor $C1$. This results in voltage steps of $C_p/C_1{}^*V_T$ at node V_G.

The transistor implementation of the charge pump is shown in Fig. 6(b). Switches $S1$–$S4$ are, respectively, implemented by MOS transistors $M6$–$M9$. $S4$ implemented with PMOS $M9$ is driven at the high gate voltage level V_G with low voltage level clock signals using a capacitive level shifter.

E. Clamp

The clamp circuit as shown in Fig. 7 delivers an output voltage which is approximately $V_T/2$ higher or lower than $V_G/2$, just as required for the charge pump. The two possible output voltages are generated by transistors $M11$–$M16$, where $M11$ and $M16$ have a large W/L and the others have a small W/L. The high or low output level of the comparator at node $V_{\rm comp}$ causes a current to flow through either $M17$ or $M19$. Due to the matched transistors pairs $M16$–$M17$ and

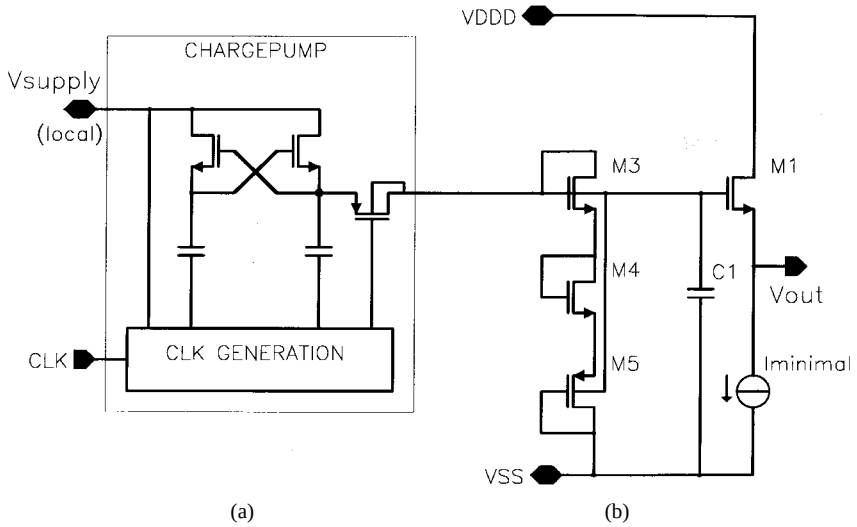


Fig. 8. Circuit to control V_G during power-down: (a) charge pump and (b) diode stack and output stage.

$M18$–$M19$, the output voltage is either a copy of the source or the gate voltage of $M16$. These are just the two required output voltage levels. The process parameter V_T is used as a reference because it is quite well defined and easy to use. This circuit also shows an example of local supply voltage reduction with source followers $M10$ and $M11$. Safe operation of the circuitry below $M10$ and $M11$ is possible with a 5 V supply.

F. Power-Down Mode

In normal operation, the regulator draws a quiescent current, dominated by the bias current of the output transistor $M1$. This current is 200 μA for a peak load current of 100 mA. In many applications, the digital part of the IC can be set to power-down mode in which the supply current is reduced to a leakage level of several microamperes. Besides the main control loop, the regulator therefore contains a powerdown loop which consumes much less power. In the power-down mode, the main control loop is almost completely switched off, the bias current in the output stage is reduced to a minimum level, and the clock frequency and other bias currents are decreased in order to save power. Using handshakes, the control is smooth and safely taken over by the less accurate power-down loop [5], shown in Fig. 8. This loop only consists of a charge pump and a stacked diode voltage reference ($M3$–$M5$). A low-power oscillator and some additional biasing deliver the required reference signals. The output voltage of the regulator in the power-down mode is in the range 2.0–3.6 V, which is accurate enough to maintain safe operation and to keep, for instance, memory contents correct. Current consumption in power-down is typically 10 μA.

G. Start-Up Circuit

Fig. 9 shows the start-up circuit which is necessary for precharging V_G. It also generates the local internal supply voltage for some circuit blocks of the regulator control loop. Consider the situation when V_G is approximately zero. Current source $J1$ initiates a current through $M27$, $M24$, $M28$, and $J3$, thereby increasing node voltage V_{GX}. Due to transistor

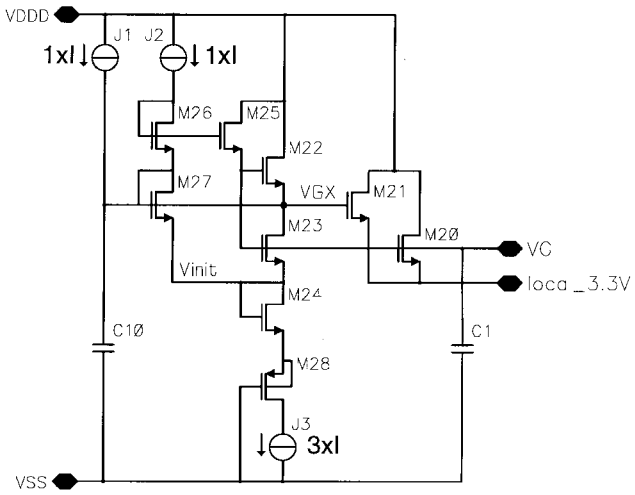


Fig. 9. Start-up circuit.

$M21$, the local supply voltage becomes almost equal to V_{init}. Simultaneously, current source $J2$ together with $M25$ and $M26$ pulls up node V_G toward V_{GX}. This is enough to guarantee proper operation of the control loop circuitry. After V_G has increased somewhat due to this control loop, $M23$, $M24$, $M28$, and $J3$ tend to conduct more current than $J1$ and $J2$ can deliver. This causes a decrease of node voltage V_{GX}, until the surplus of sink current is flowing through $M22$. At that time, voltage V_{GX} has become close to V_{init}, and both $M21$ and $M25$ are switched off. The internal supply voltage is now determined by source follower $M20$. This completes the start-up procedure. Note that the diode stack $M23$, $M24$, $M28$ is similar to the diode stack used for the power-down loop, except for a different connection of the back gate which causes a slightly different threshold. This ensures that the start-up circuit cannot become active during normal power-down operation.

H. Complete Regulator

As mentioned before, the area needed for $M1$ and $C1$ is proportional to the required peak load current. In order to

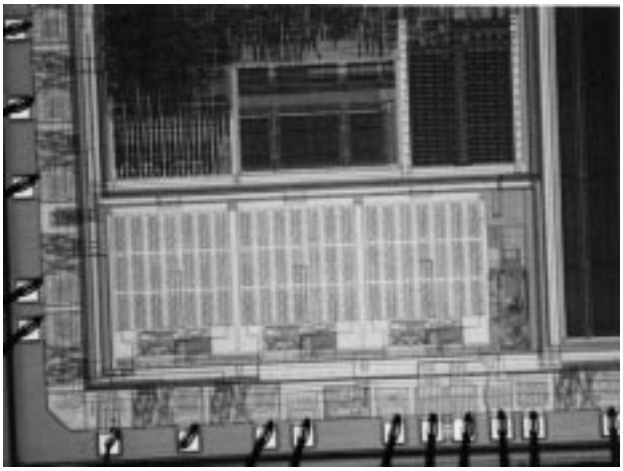


Fig. 10. Photograph of the regulator. The circuit is applied in a 16 bit microcontroller in 0.5 μm CMOS technology.

facilitate application of the regulator in different IC's, the regulator is implemented in modules for 100 mA peak load current each. A complete regulator can consist of several modules in parallel, depending on the totally required peak load current for an application. In case of overload, the output voltage will drop only slightly due to the source-follower output structure. Every module has its own main control loop, except for the bandgap reference and oscillator. This ensures a loop behavior independent of the number of modules. The modules together have only one common power-down loop for power-saving reasons, which is implemented together with the bandgap, oscillator, start-up circuit, additional biasing, and control circuitry in a single common module.

The implementation of a 5 V circuit in 3.3 V CMOS technology requires several measures against hot-electron effects to avoid stress effects for V_{DDD} up to 5.5 V. These include: overvoltage protection with cascodes, voltage division by series connection, voltage clamping, locally generated lower supplies (see, for example, $M10$ and $M11$ in Fig. 7), and temporary reduction of critical voltages in case of changing operation mode.

A 300 mA peak-current regulator consisting of three modules of 100 mA each has been designed for a 16 bit microcontroller application [7] in 0.5 μm CMOS technology. The die area of this regulator is 1 mm^2, which is mainly determined by $M1$ and $C1$. A chip photograph of the embedded regulator is shown in Fig. 10. The three modules of 100 mA each can be well distinguished. On the right-hand side, the common control unit is located.

III. Experimental Results

Fig. 11 shows the measured regulator dc output voltage $V_{\rm out}$ versus external supply V_{DDD} for different dc load currents at room temperature. The output voltage is 3.3 V $\pm$ 10% if $V_{DDD} > 3.3$ V. For lower V_{DDD} values, the output voltage follows V_{DDD}. Also, it can be seen that in the normal operation range, the output voltage drops out 300 mV if the current is increased from 0 to 300 mA. This voltage variation, is as expected, approximately proportional

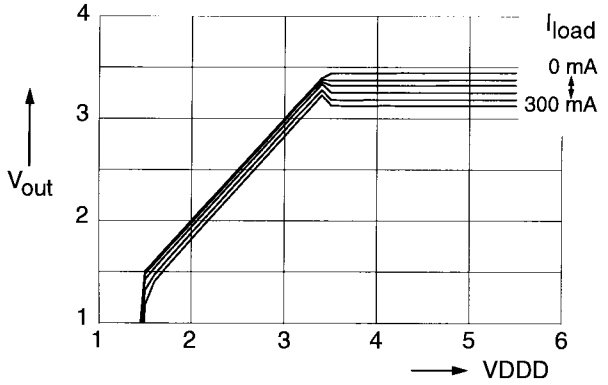


Fig. 11. Measured regulator dc output voltage $V_{\rm out}$ versus external supply V_{DDD} for different load currents.

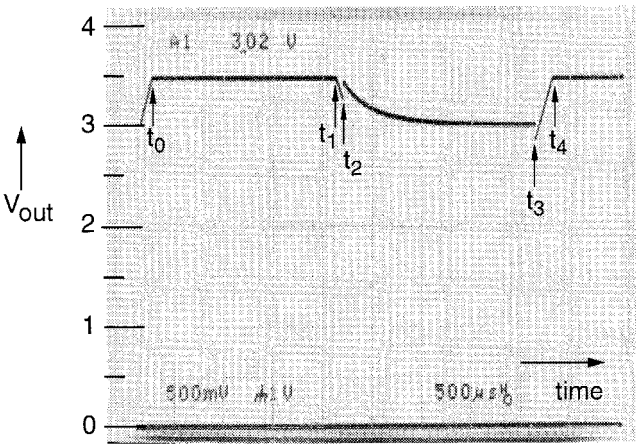


Fig. 12. Illustration of how the circuit can be switched between normal mode and power-down mode. The output voltage is plotted versus time. $t = t_1$: switch to power-down mode, $t = t_3$: switch back to normal mode.

to absolute temperature. The static accuracy was found to be correct and independent of temperature. Measurements of the bandgap voltage (typically 1.21 V) showed a standard deviation of 0.8% due to process variation and a negligible temperature coefficient.

Fig. 12 illustrates how the circuit can be switched between normal mode and power-down mode. Here, the output voltage is plotted versus time (on a large scale). At $t = t_0$, the regulator operates in normal mode, and the output current is small, so the output voltage is rather high: 3.45 V. At $t = t_1$, the circuit is switched to power-down. First, the gate voltage V_G is lowered by the main charge pump, and after that, at $t = t_2$, the bias current $I_{\rm min} = 200\ \mu$A through each output transistor $M1$ is strongly reduced. The result is that the output voltage increases sharply. Now, V_G converges slowly to its new value determined by the power-down charge pump and stacked diode reference. The output voltage follows V_G. In power-down mode, the regulator has a nominal output voltage about 3.0 V, and consumes only 10 μA supply current. At $t = t_3$, the circuit is switched to normal mode again. The 200 μA bias current $I_{\rm min}$ through the transistors $M1$ is switched on, and consequently, the output voltage drops. Also, the main control loop starts pumping V_G to its right value. At $t = t_4$, the circuit is in its normal mode.

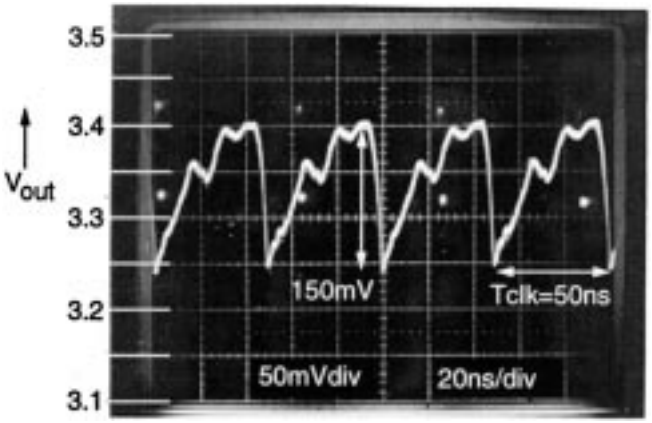


Fig. 13. Measured internal supply voltage transients of the 16 bit microcontroller operating at 20 MHz.

TABLE I
PERFORMANCE SUMMARY

	Min.	Nom.	Max.	Unit
External Supply Vddd	3.3	5.0	5.5	[V]
V_{out} (power-up)	3.0	3.3	3.6	[V]
V_{out} (power-down)	2.0	3.0	3.6	[V]
I_{load}	0		300	[mA]
Iddd-quiescent (power-up)		750		[μA]
Iddd-quiescent (power-down)		10		[μA]
Start-up time from zero		300		[μs]
Recovery time from PD		150		[μs]
V_{ripple} for constant load		12		[mV]
Area 300mA Regulator		1.0		[mm^2]
Process	3.3V-CMOS,0.5μm,3AL,1PS			

The measured internal supply voltage of the 16 bit microcontroller IC operating at 20 MHz clock frequency is shown in Fig. 13. The ripple on the supply voltage is 150 mV, which is less than the designed 300 mV. Apparently, the microcontroller has a lower peak current than the estimated 300 mA. The period of the ripple in the internal supply voltage corresponds to the clock period of the microcontroller. It can be seen that the supply voltage remains easily within the 3.3 V $\pm$ 10% limits.

Table I gives a summary of the experimental data.

IV. CONCLUSIONS

An embedded 5 to 3.3 V supply regulator for digital IC's in 3.3 V, 0.5 μm CMOS technology has been designed. The circuit is able to deliver the steep supply-current transients for digital circuits while the output voltage remains within $\pm$10% accuracy. The circuit needs no large (external) capacitor across the internal 3.3 V. The circuit has a small die area: 1 mm^2 for 300 mA peak current. The output voltage remains correct for an external supply voltage down to 3.3 V. The replica technique used guarantees stability independent of the load, and significantly reduces the voltage ripple at the output. In power-down mode, the current consumption is reduced to 10 μA. The implementation of the regulator contains several measures against hot electron effects to ensure safe operation for V_{DDD} up to 5.5 V.

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Gerrit W. den Besten was born in Hei-en Boeicop, The Netherlands, in 1971. He received the M.S. degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1994 on the subject of clock generation and phase-locked loops.

In the same year, he joined Philips Research Laboratories, Eindhoven. His research interests are in the field of analog key modules.

Bram Nauta (S'89–M'91), for a photograph and biography, see this issue, p. 936.